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TSMC98-726 To the Honorable Commissioner of Patents and Trademarks: Please 1 Name of conveying party(ies):	inal documents or copy thereof.	
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MENG-CHANG LIU, JYH-FENG LIN, MING-SHU YEN, SU-YING SU, FU-YING CHIU AND CHIEN-HUNG LIN	Name: Taiwan Semiconductor Manufacturing Company	
Additional name(s) or conveying party(ies) attached? Yes X No		
	Street Address:	
3. Nature of conveyance X Assignment Merger Security Agreement Change of Name	121 Park Ave. 3 Science-Based Industrial Park City: Hsin-Chu Zip: Country: Taiwan, R.O.C.	
other		
Execution Date: 6/14/99	Additional name(s) & address(es) attached? Yes X No	
4. Application number(s) or patent number(s):		
If this document is being filed together with a new application A. Patent Application No(s)	n, the execution date of the application is: 6/14/99 B. Patent No.(s) 09/373636	
Additional numbers attache	d? Yes X No	
5. Name and address of party to whom correspondence concerning document should be mailed: Name: GEORGE O. SAILE	6. Total no. of applications and patents involved:: 1	
Internal Address:	7. Total fee (37 CFR 3.41): \$ 40.00	
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In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration,		
ASSIGNOR:		
MENG - CHANG LIU Type or print name of ASSIGNOR No. 49, Charnq - Rong Rd.,	JYH-FENG LIN Type or print name of ASSIGNOR No. >> 8, Lm-Seng Rd., Kuang-Fu	
Address Taiwan	country. Han-lien country Town	
No. 49, Charng-Rong Rd., Address Chiayi , Taiwan Republic of China Nationality	Republic of China Nationality	
MING-SHU YEN Type or print name of ASSIGNOR No 15-5, 57 allow, 271 lane, War-ling mod Address Hain-Chu, Tailman		
Republic of Chipman		
ASSIGNEE: Taiwan Semiconductor Manufacturing Co. Ltd. 121 Park Ave. 3 Science-Based Industrial Park Hsin-Chu, Taiwan, R.O.C. Taiwan, R.O.C. Nationality		
and the successors, assigns and legal representatives of the ASSIGNEE (complete one of the following)		
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A Method For Making Improved Polysilicon FET Gate Electrodes Having Composite Sidewall Spacers Using A Trapezoidal-Shaped Insulating Layer For More Reliable Integratated Circuits

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ASSIGNOR:		
	Ac 36. Luzz, Peichen, Peikan, Yulin, Tain	
Pepublic of China		
CHIEN-HUNG LIN Type or print name of ASSIGNOR FF-1, NO. 50, University Address Ham-Chu, Taiwan K. O. C. Nationality	$\mathcal{R} \mathcal{D}_{\cdot}$	
ASSIGNEE: Taiwan Semiconductor Manufacturing Control 121 Park Ave. 3 Science-Based Industrial Park Hsin-Chu, Taiwan, R.O.C. Taiwan, R.O.C. Nationality	o. Ltd.	
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(complete	one of the following)	
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in and to any and all improvements which are disclosed in the invention entitled:		
A Method For Making Improved Polysilicon FET Gate Electrodes Having Composite Sidewall Spacers Using A Trapezoidal-Shaped Insulating Layer For More Reliable Integratated Circuits		

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and which is found in

(a) U.S. patent application executed on eve	en date herewith
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June 14, 1999 (Date	e of signing)
WARNING Date of signing must be the same as the date of	
If ASSIGNOR is a legal entity complete the following in	Meng-Chang Liu Signature of Assignor(s) Jxh-Feng Lin Su-Ying Su Ming-Inn Yen Fu-Tim Chin Chieffy information
	Type or print the name of the above person authorized to sign or behalf of ASSIGNOR
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	the assignment is notarized or legalized then it will only be prima facie evidence (35 USC
261). Use next page if notarization is desired.	Notarization of Legalization Page Added.

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