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ASSIGNMENT SHEET

To: Honorable Commissioner of Patents and Trademarks:

Please record the attached original document(s) or copy thereof.

1. Name of conveying party(ies)
   a) United Semiconductor Corp.

2. Name and address of receiving party(ies):
   a) Name: United Microelectronics Corp.
   Address: No. 3, Li-Hsin Rd. 2
   Science-Based Industrial Park
   Hsinchu, Taiwan
   R.O.C.

3. Nature of conveyance

☒	Assignment	☐	Merger
☐	Security Agreement	☐	Change of Name
☐	Other _____	☐	License Agreement

Execution Date: December 30, 1999

4. Application Number(s) or Patent Number(s): See Appendix A

The title of the (new) application is:

See Appendix A

5. Please send all correspondence concerning this (these) documents to:

HICKMAN STEPHENS COLEMAN & HUGHES, LLP
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6. Total number of applications and patents involved: 316

7. Total fee (37 CFR 3.41): $12,640.00

☒ Enclosed
☐ Authorized to be charged to Deposit Account No. 50-0384
(Order No. JCIPG000)

8. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Date: January 18, 2000

Paul L. Hickman
Registration No. 28,516

02/23/2000 DWGUYEN 00000252 08868752
01 FC:581 12640.00 OP

Attorney Docket No. JCIPG000

(Revised 01/96)

Appendix A

Title	Filing/Issue Date	Serial/Patent No.
METHOD OF FORMING FLUOROSILICATE GLASS (FSG) LAYERS WITH MOISTURE-RESISTANT CAPABILITY	1997/6/5	08/868,752
METHOD OF REMOVING SILICON CARBIDE FROM DAMAGED SILICON SUBSTRARE	1997/6/12	08/873,925
SHALLOW TRENCH ISOLATION FOR SEMICONDUCTOR DEVICES	1997/8/27	08/924,432
METHOD OF REDUCING CROSS CONTAMINATION IN ION IMPLANTORS	1997/11/7	08/965,783
METHOD AND CONTROLLING SYSTEM FOR PREVENTING THE SCRATCHING OF WAFER BACKS BY THE FETCH ARM OF A STEPPER MACHINE	1997/12/16	08/991,187
METHOD FOR FORMING ETOX CELL USING SELF-ALIGNED SOURCE ETCHING PROCESS	1997/12/18	08/992,884
ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1997/12/24	08/998,000
IMPROVED METHOD OF ETCHING	1997/12/29	08/998,769
FABRICATING METHOD FOR FIELD OXIDE ISOLATION DEVICE	1997/12/29	08/999,135
METHOD FOR IMPROVING DIFFERENTIAL ETCHING RATE OF A METALLIC LAYER	1997/12/30	09/000,966
METHOD OF MANUFACTURING SHALLOW TRENCH ISOLATION	1998/1/20	09/008,858
METHOD FOR PREVENTING THE FORMATION OF RECESSES IN BOROPHOSPHOSILICATE GLASS	1998/2/13	09/023,235
METHOD FOR FABRICATING CAPACITOR	1998/2/13	09/023,879
METHOD OF FABRICATING FLASH MEMORY CELL	1998/2/17	09/024,163
FLASH MEMORY CELL	1998/2/17	09/024,782
MANUFACTURING METHOD FOR A THIN FILM WITH AN ANTI-REFLECTION ROUGH SURFACE	1998/3/2	09/033,113
METHOD OF FABRICATING A SPLIT GATE FLASH MEMORY DEVICE	1998/3/2	09/033,376
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1998/3/18	09/040,912
METHOD OF FORMING A SELF-ALIGNED CONTACT IN SEMICONDUCTOR FABRICATIONS	1998/3/23	09/046,059
METHOD OF NITRIDE-SEALED OXIDE –BUFFERED LOCAL OXIDATION OF SILICON	1998/3/26	09/048,697
METHOD OF GROW SELF-ALIGNED SILICON ON A POLY-GATE, SOURCE AND DRAIN REGION	1998/3/26	09/048,924
METHOD FOR MANUFACTURING DRAM CAPACITOR	1998/4/3	09/054,836
METHOD OF FABRICATING STORAGE CAPACITOR FOR DYNAMIC RANDOM ACCESS MEMORY	1998/4/3	09/054,837
METHOD FOR MANUFACTURING DRAM CAPACITOR	1998/4/10	09/058,579
NON-FURNACE CURING PROCESS OS LOW K KIELECTRIC MATERIAL WITH IMPLANT TREATMENT FOR THERMAL	1998/4/14	09/059,684

Title	Filing/Issue Date	Serial/Patent No.
STABILITY LOW K AND RIA POISON IMPROREMENT		
INVERCE-π CAPACITOR WITH RUGGED-POLY SARFACE	1998/4/4	09/059,686
METHOD FOR MANUFACTURING CAPACITOR'S LOWER ELECTRODE	1998/4/17	09/061,658
ETCHING MACHINE HAVING LOWER ELECTRODE BIAS VOLTAGE SOURCE	1998/4/17	09/062,116
METHOD FOR FORMING METALLIC LAYER	1998/4/21	09/063,672
METHOD OF FABRICATING DUAL CYLINDRICAL CAPACITOR	1998/4/24	09/066,196
DUAL CYLINDRICAL CAPACITOR	1998/4/24	09/066,197
METHOD OF PLANARIZING DIELECTRIC LAYER	1998/4/27	09/067,548
METHOD OF FABRICATING STACK CAPACITOR	1998/4/30	09/070,374
STACK CAPACITOR	1998/4/30	09/070,375
METHOD OF FORMING SHALLOW TRENCH ISOLATION	1998/5/6	09/073,708
METHOD OF MANUFACTURING SELF-ALIGNED SILICIDE	1998/5/8	09/075,420
METHOD OF FABRICATING SPLIT-GATE SOURCE SIDE INJECTION FLASH MEMORY ARRAY	1998/5/12	09/076,672
FABRICATING METHOD OF NON-VOLATILE FLASH MEMORY DEVICE	1998/5/12	09/076,676
METHOD OF FABRICATING BIT LINE	1998/5/21	09/082,660
METHOD OF FABRICATING A CAPACITOR OVER A BIT LINE OF A DRAM	1998/6/2	09/089,245
METHOD FOR FABRICATING A CAPACITOR IN A DYNAMIC RANDOM ACCESS MEMORY	1998/6/24	09/103,957
THE NOVEL MEASUREMENT METHOD OF KIND (HUMP) EFFECT IN EFFECT IN SECONDARY APPROACH	1998/6/30	09/106,745
THE METHOD OF KIND EFFECT WITH CHANNEL WIDTH MODULATIN IN EXTRAPOLATION	1998/6/30	09/106,752
TOOL FOR INSPECTING BROKEN WAFER EDGES	1998/6/9	09/107,164
METHOD OF FORMING A VIA	1998/7/10	09/113,471
STRUCTURE OF BURIED BIT LINE	1998/7/10	09/113,844
PREHEATING METHOD FOR HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION	1998/7/17	09/118,054
METHOD FOR FABRICATING A VIA	1998/8/11	09/132,384
METHOD OF FABRICATING DOUBLE DOPED SOURCE REGION	1998/3/2	09/133,148
METHOD OF REDUCING THE REFLECTIVITY AND SWING EFFECT OF WAFER SURFACES IN A PHOTOLITHOGRAPHIC PROCESS	1998/8/19	09/136,566
METHOD OF FABRICATING CAPACITOR	1998/8/20	09/137,028
METHOD OF FABRICATING FLASH ELECTRICALLY-ERASABLE AND PROGRAMMABLE READ-ONLY MEMORY (EEPROM) DEVICE	1998/8/24	09/138,757

Title	Filing/Issue Date	Serial/Patent No.
METHOD FOR ETCHING (AS AMENDED)	1998/8/24	09/138,758
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1998/8/25	09/140,114
ARCHITECTURE OF POLY FUSES	1998/9/9	09/149,929
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/9/14	09/152,360
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/9/14	09/152,450
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/10/1	09/164,288
HIGH VOLTAGE DEVICE	1998/10/1	09/164,690
SETUP FOR REMOVING SLURRY FROM A POLISHING PAD	1998/10/14	09/172,280
METHOD OF COATING AMORPHOUS SILICON FILM	1998/10/30	09/183,061
METHOD OF FABRICATING HIGH VOLTAGE SEMICONDUCTOR DEVICE	1998/10/30	09/183,062
CHEMICAL MECHANICAL POLISHING METHOD	1998/11/4	09/185,808
METHOD OF FABRICATING AN INTEL TYPE FLASH ERASABLE PROGRAMMABLE READ ONLY MEMORY CELL	1998/11/4	09/185,941
METHOD FOR FABRICATING A NON-VOLATILE MEMORY DEVICE	1998/11/4	09/186,129
METHOD OF REMOVING RESIDUE ON A BONDING PAD	1998/11/5	09/186,531
METHOD OF FABRICATING A FLASH MEMORY CELL	1998/11/5	09/186,743
METHOD OF MENDING EROSION OF BONDING PAD	1998/11/5	09/186,744
FLASH MEMORY STRUCTURE AND METHOD OF MANUFACTURE	1998/11/5	09/186,748
ANTI-LEAKAGE APPARATUS	1998/11/6	09/186,999
METHOD FOR FABRICATING A PASSIVATION LAYER	1998/11/6	09/187,958
STRUCTURE OF A FLASH MEMORY	1998/11/13	09/191,326
METHOD OF FORMING HEMISPHERICAL GRAIN POLYSILICON OVER LOWER ELECTRODE CAPACITOR	1998/11/13	09/191,327
METHOD OF MANUFACTURING FLASH MEMORY CELLS	1998/11/13	09/191,798
EEPROM CELL STRUCTURE	1998/11/13	09/191,933
METHOD FOR ANALYZING A CONSEQUENT EFFECT OF A FABRICATION MACHINE CLUSTER	1998/11/25	09/200,330
METHOD OF FABRICATING A DRAM CAPACITOR	1998/12/4	09/206,109
METHOD FOR FABRICATING A TRANSISTOR	1998/12/4	09/206,111
METHOD OF FABRICATING BIT LINES BY DAMASCENE	1998/12/4	09/206,112
METHOD OF FORMING A SHALLOW TRENCH ISOLATION	1998/12/4	09/206,182
FLASH MEMORY STRUCTURE	1998/12/17	09/213,344
METHOD OF MANUFACTURING A FLASH MEMORY STRUCTURE	1998/12/17	09/213,345
METHOD OF FABRICATING METAL OXIDE	1998/12/17	09/213,599

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Title	Filing/Issue Date	Serial/Patent No.
SEMICONDUCTOR		
METHOD OF FABRICATING A FLASH MEMORY	1998/12/17	09/213,600
METHOD OF FORMING A SHALLOW TRENCH ISOLATION	1998/12/17	09/213,700
METHOD OF FABRICATING A DYNAMIC RANDOM ACCESS MEMORY CAPACITOR	1998/12/17	09/213,783
METHOD FOR BOTTOM ELECTRODE OF CAPACITOR	1998/12/17	09/213,934
METHOD OF FABRICATING AN ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT	1998/12/17	09/215,599
DYANMIC RANDOM ACCESS MEMORY CAPACITOR	1998/12/17	09/215,619
METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION STRUCTURE	1998/12/30	09/223,200
METHOD FOR FABRICATING A METAL VIA	1998/12/30	09/223,328
METHOD FOR FORMING VIA HOLE	1998/12/30	09/223,330
SPIN-ON-GLASS PLANARIZATION	1998/12/30	09/223,334
METHOD OF FABRICATING FLASH ERASABLE PROGRAMMABLE READ ONLY MEMORY	1998/12/30	09/223,337
PLANARIATION PROCESS	1998/12/30	09/223,398
METHOD FOR FORMING FLASH MEMORY CELL	1998/12/30	09/223,613
A METHOD FOR FORMING A VIA	1999/1/8	09/227,347
METHOD FOR FORMING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/8	09/227,379
ETCHING PROCESS	1999/1/8	09/227,627
SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/8	09/227,660
METHOD FOR FABRICATING A FLASH MEMORY	1999/1/8	09/227,680
METHOD FOR FABRICATING A FLASH MEMORY	1999/1/8	09/227,974
METHOD FOR FORMING A VIA	1999/1/8	09/227,975
FLASH MEMORY STRUCTURE	1999/1/22	09/235,261
METHOD OF FORMING SHALLOW TRENCH ISOLATION	1999/1/22	09/235,268
METHOD OF FORMING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/25	09/236,951
METHOD OF MANUFACTURING SHALLOW TRENCH ISOLATION	1999/1/25	09/236,955
METHOD OF COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR	1999/1/25	09/236,962
SELF-ALIGNED SILICIDE PROCESS	1999/1/25	09/237,211
METHOD FOR FABRICATING FLASH MEMORY	1999/1/25	09/237,295
METHOD OF REMOVING CARBON CONTAMINATION ON SEMICONDUCTOR SUBSTRATE	1999/2/1	09/241,338
METHOD FOR MANUFACTURING A CYLINDRICAL CAPACITOR	1999/2/1	09/241,522
TRIPLE WELL STRUCTURE	1999/2/1	09/241,524

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Title	Filing/Issue Date	Serial/Patent No.
SURFACE TREATMENT FOR BONDING PAD	1999/2/1	09/241,525
METHOD FOR FORMING HEMISPHERICAL SILICON GRAINS ON DESIGNATED AREAS OF SILICON LAYER	1999/2/1	09/241,526
METHOD FOR FABRICATING CONTACT HOLE	1999/2/1	09/241,527
METHOD FOR REMOVING POLY DEFECT	1999/2/1	09/241,528
METHOD FOR FABRICATING A FLASH MEMORY	1999/2/1	09/241,544
DAMASCENE PROCESS	1999/2/1	09/241,742
ETCHING METHOD FOR DOPED POLYSILICON LAYER	1999/2/1	09/241,757
METHOD OF FORMING A FLASH MEMORY DEVICE	1999/2/1	09/241,759
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/2/1	09/241,760
METHOD FOR FORMING SHALLOW TRENCH ISOLATION	1999/2/1	09/241,789
METHOD OF REDUCING SALICIDE LATERAL GROWTH	1999/2/1	09/241,792
SELF-ALIGNED CONTACT PROCESS	1999/2/1	09/241,793
METHOD FOR FABRICATING SHALLOW TRENCH ISOLATION STRUCTURE	1999/2/1	09/241,977
METHOD FOR FORMING HEMISPHERICAL GRAINED SILICON STRUCTURE	1999/2/8	09/246,226
SHALLOW TRENCH ISOLATION	1999/2/8	09/246,278
METHOD FOR REMOVING PHOTORESIST	1999/2/8	09/246,737
METHOD OF MANUFACTURING PASSIVATION LAYER	1999/2/8	09/246,755
METHOD FOR FORMING SALICIDE LAYERS	1999/2/8	09/246,762
METHOD FOR FORMING INTER-METAL DIELECTRICS	1999/2/16	09/249,882
METHOD OF FABRICATING SELF-ALIGNED SILICIDE	1999/2/16	09/250,618
METHOD OF MANUFACTURING CAPACITOR FOR MIXED-MODE CIRCUIT DEVICE	1999/2/16	09/250,628
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1999/2/16	09/250,749
METHOD OF MANUFACTURING BIT LINE	1999/2/16	09/252,600
METHOD FOR FABRICATING SELF-ALIGNED METAL PLUG	1999/3/1	09/260,628
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/3/2	09/261,094
METHOD OF FABRICATING A GATE STRUCTURE OF SEMICONDUCTOR DEVICE	1999/3/2	09/261,096
METHOD OF CHEMICAL-MECHANICAL POLISHING	1999/3/2	09/261,098
METHOD OF MANUFACTURING FLASH MEMORY	1999/3/11	09/267,760
METHOD OF FABRICATING BARRIER LAYER	1999/3/11	09/267,875
METHOD OF MANUFACTURING LINER INSULATING LAYER	1999/3/11	09/267,883
METHOD FOR FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/3/11	09/267,884

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Title	Filing/Issue Date	Serial/Patent No.
METHOD FOR MONITORING DOSAGE/FOCUS/LEVELING	1999/3/16	09/270,278
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORIES	1999/3/16	09/270.027
METHOD FOR CLEANING A CHEMICAL VAPOR DEPOSITION CHAMBER	1999/3/18	09/272,013
METHOD OF FABRICATING FLASH MEMORY	1999/3/19	09/273,067
METHOD OF FABRICATING A DUAL DAMASCENE STRCUTURE	1999/3/23	09/274,603
IN AN INTEGRATED CIRCUIT		
SEMICONDUCTOR DEVICE WITH AN ANTI-DOPED REGION	1999/3/29	09/280,297
METHOD FOR FABRICATING A SELF-ALIGNED SILICIDE	1999/3/29	09/280,626
METHOD OF FABRICATING DUAL DAMASCENE STRUCTURE	1999/3/29	09/280,892
METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH AN ANTI-DOPED REGION	1999/3/29	09/282,018
METHOD OF FABRICATING SILICIDE LAYER ON GATE ELECTRODE	1999/4/5	09/286,004
METHOD OF MANUFACTURING INTERCONNECT	1999/4/5	09/286,005
METHOD OF FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/4/5	09/286,018
METHOD OF MANUFACTURING BOTTOM ELECTRODE	1999/4/5	09/286,021
METHOD OF MANUFACTURING FLASH MEMORY	1999/4/5	09/286,139
METHOD FOR IN-SITU REMOVING PHOTORESIST AND SIDEWALL POLYMER	1999/4/5	09/286,219
METHOD FOR MANUFACTURING SHALLOW TRENCH	1999/4/5	09/286,231
ISOLATION STRUCTURE		
METHOD OF FABRICATING SILICIDE LAYER	1999/4/5	09/286,687
METHOD FOR FABRICATING A FLASH MEMORY	1999/4/16	09/292,870
METHOD OF FABRICATING ANTI-REFLECTION LAYER	1999/4/16	09/292,871
SELF-ALIGNED METAL SILICIDE	1999/4/16	09/293,419
METHOD OF MANUFACTURING INTERCONNECT	1999/4/16	09/293,420
FULLY SELF-ALIGNED METHOD FOR FABRICATING TRANSISTOR AND MEMORY	1999/4/16	09/293,430
METHOD FOR FORMING A STACKED GATE	1999/4/16	09/293,434
METHOD OF FABRICATING SELF-ALIGNED METAL SILICIDE	1999/4/16	09/293,826
METHOD OF FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/4/19	09/294,541
METHOD OF MANUFACTURING BOTTOM ELECTRODE	1999/4/20	09/295,067
OF CAPACITOR		
METHOD OF OPTICAL PROXIMITY CORRECTION	1999/4/23	09/298,324
METHOD FOR FABRICATING A HYBRID ISOLATION	1999/4/26	09/299,719

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Title	Filing/Issue Date	Serial/Patent No.
STRUCTURE		
METHOD FOR FABRICATING CAPACITOR	1999/5/6	09/306,093
METHOD OF MANUFACTURING METAL-OXIDE SEMICONDUCTOR TRANSISTOR	1999/5/6	09/306,094
FLASH MEMORY	1999/5/6	09/306,119
METHOD OF MANUFACTURING INTERCONNECT	1999/5/6	09/306,130
EQUIPMENT AND METHOD FOR MORNITORING A WAFER SURFACE	1999/5/6	09/306,166
ELECTROSTATIC DISCHARGE PROTECTIVE CIRCUIT	1999/5/6	09/306,243
METHOD OF FABRICATING FLASH MEMORY	1999/5/6	09/306,348
TRANSISTOR STRUCTURE OF ESD PROTECTION DEVICE	1999/5/7	09/307,319
METHOD OF FABRICATING DUAL DAMASCENE	1999/5/10	09/309,186
METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR	1999/5/17	09/313,166
METHOD FOR FORMING GATE TERMINAL	1999/5/17	09/313,167
METHOD FOR FORMING CONDUCTIVE LINE	1999/5/17	09/313,510
METHOD OF FABRICATING FLASH MEMORY	1999/5/17	09/313,511
METHOD FOR FABRICATING PASSIVATION LAYER	1999/5/17	09/313,516
METHOD OF FABRICATING SEMICONDUCTOR DEVICE	1999/5/21	09/315,797
TEST KEY ARCHITECTURE	1999/5/21	09/316,196
METHOD FOR FABRICATING INTER-METAL DIELECTRIC LAYER	1999/5/21	09/316,475
STRUCTURE OF ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/5/21	09/316,584
METHOD OF FABRICATING PASSIVATION LAYER IN LIQUID CRYSTAL DISPLAY	1999/5/21	09/316,585
METHOD OF FABRICATING STORAGE NODE	1999/5/24	09/316,979
METHOD OF FABRICATING CAPACITOR	1999/5/27	09/322,051
METHOD OF FABRICATING METAL PLUG	1999/5/27	09/322,054
METHOD FOR FABRICATING FIELD EMISSION DISPLAY CATHODE	1999/5/27	09/322,055
METHOD FOR IMPROVING STABILITY OF ANTI-COATING LAYER	1999/6/4	09/325,365
METAL ETCHING PROCESS	1999/6/4	09/326,380
METHOD AND STRUCTURE FOR MEASURING A RELATIVE POSITIONAL DEVIATION OF A RETICLE PATTERN	1999/6/4	09/326,392
METHOD OF FABRICATING PASSIVATION OF GATE ELECTRODE	1999/6/8	09/328,056
METHOD FOR FABRICATING A GATE CONDUCTIVE STRUCTURE	1999/6/9	09/328,850
METHOD FOR FABRICATING SILICON-ON-INSULATOR STRUCTURE WITH SHALLOW TRENCH ISOLATION	1999/6/9	09/328,851

Title	Filing/Issue Date	Serial/Patent No.
STRUCTURE		
METHOD OF FABRICATING SEMICONDUCTOR DEVICE	1999/6/9	09/328,967
METHOD FOR MANUFACTURING EVEN DIELECTRIC LAYER	1999/6/9	09/328,977
METHOD OF FORMING UNLANDED VIA HOLE	1999/6/9	09/329,113
METHOD OF MANUFACTURING TRANSISTOR WITH T-SHAPED GATE ELECTRODE	1999/6/16	09/334,532
METHOD OF FORMING A CONTACT PLUG IN A SEMICONDUCTOR DEVICE	1999/6/18	09/335,808
FABRICATION METHOD OF A SELF-ALIGNED CONTACT WINDOW	1999/6/19	09/336,553
METHOD OF FABRICATING CONDUCTIVE LINE STRUCTURE	1999/6/19	09/336,554
METHOD OF MANUFACTURING INTERCONNECT	1999/6/28	09/340,928
METHOD FOR MANUFACTURING METAL OXIDE SEMICONDUCTOR TRANSISTOR HAVING RAISED SOURCE/DRAIN	1999/6/28	09/340,969
FABRICATION METHOD OF AN INTERCONNECT	1999/6/28	09/344,865
METHOD OF MANUFACTURING SALICIDE LAYER	1999/7/1	09/345,435
METHOD OF MANUFACTURING CONTACT PAD	1999/7/2	09/347,180
METHOD FOR FORMING POLYSILICON GATE ELECTRODE	1999/7/7	09/348,389
METHOD FOR FABRICATING PASSIVATION LAYER ON METAL PAD	1999/7/7	09/348,396
METHOD OF FABRICATING PRESERVE LAYER	1999/7/7	09/348,407
SHALLOW TRENCH ISOLATION PROCESS	1999/7/7	09/348,409
METHOD OF FABRICATING FLOATING GATE	1999/7/7	09/348,410
FOR FLASH MEMORY		
METHOD OF FABRICATING INTERCONNECT	1999/7/7	09/348,984
FABRICATION METHOD OF A GATE JUNCTION	1999/7/19	09/356,961
CONDUCTIVE STRUCTURE		
METHOD FOR STABILIZING A PLASMA MACHINE OPERATION	1999/7/23	09/360,076
METHOD OF MONITORING DEEP ULTRAVIOLET	1999/8/9	09/370,773
EXPOSURE SYSTEM		
METHOD FOR FORMING CROWN SHAPE CAPACITOR	1999/8/9	09/370,774
FABRICATION METHOD FOR A MOS DEVICE WITH REDUCED RESISTANCE	1999/8/10	09/371,470
CONVEYANCE ARM DEVICE	1999/8/10	09/372,431
FABRICATION METHOD FOR GATE STRUCTURE HAVING GATE DIELECTRIC LAYERS OF DIFFERENT THICKNESSES	1999/8/17	09/375,877
METHOD OF FABRICATING FLASH MEMORY	1999/8/23	09/379,382
FLASH MEMORY	1999/8/23	09/379,890

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Title	Filing/Issue Date	Serial/Patent No.
METHOD OF FABRICATING A MOS TRANSISTOR	1999/8/25	09/383,033
METHOD FOR FABRICATING GATE OXIDE LAYER	1999/8/30	09/385,805
METHOD OF FABRICATING MULTILEVEL INTERCONNECT	1999/9/3	09/389,823
METHOD FOR MANUFACTURING DYNAMIC RANDOM ACCESS MEMORY	1999/9/3	09/389,824
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/9/9	09/392,924
LIFETIME MEASUREMENT OF AN ULTRA-THIN DIELECTRIC LAYER	1999/9/9	09/393,054
METHOD TO REDUCE PARASITIC CAPACITANCE	1999/9/13	09/394,636
METHOD FOR MANUFACTURING BIT LINE AND BIT LINE CONTACT	1999/9/13	09/394,637
METHOD OF FABRICATING PASSIVATION LAYER	1999/9/14	09/395,442
METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION	1999/9/15	09/396,140
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/9/15	09/397,161
POST-ETCHING CLEANING PROCESS	1999/9/23	09/404,113
METHOD OF FABRICATING PROTECTION STRUCTURE	1999/9/28	09/406,356
METHOD OF PROTECTING A WELL AT A FLOATING STAGE	1999/9/28	09/406,517
METHOD OF FORMING A SELF-ALIGNED SILICIDE STRUCTURE IN INTEGRATED CIRCUIT FABRICATION	1999/9/29	09/408,152
RETARDATION LAYER FOR PREVENTING DIFFUSION OF METAL LAYER AND FABRICATION METHOD THEROF	1999/9/30	09/408,612
ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH A REDUCED TRIGGER VOLTAGE	1999/10/4	09/411,993
AN POLYSILICON ETCHING METHOD	1999/10/5	09/412,872
METHOD OF MANUFACTURING A TANTALUM OXIDE FILM	1999/10/8	09/414,741
METHOD FOR INCREASING SURFACE AREA OF A BOTTOM ELECTRODE FOR A DRAM	1999/10/8	09/415,564
METHOD OF FABRICATING DUAL DAMASCENE	1999/10/12	09/417,830
METHOD TO MAINTAIN CONSISTENT THICKNESS OF THIN FILM DEPOSITED BY CHEMICAL VAPOR DEPOSITION	1999/10/20	09/420,961
METHOD OF FORMING SEMICONDUCTOR DEVICE CONTACT	1999/10/20	09/421,312
METHOD FOR REDUCING INVERSE-NARROW-WIDTH-EFFECT	1999/10/20	09/421,842
METHOD FOR FABRICATING A DYNAMIC RANDOM ACCESS MEMORY CELL	1999/10/21	09/422,577
METHOD OF FORMING A FLASH MEMORY	1999/10/21	09/422,625
THREE-DIMENSIONAL FLASH MEMORY STRUCTURE AND FABRICATION METHOD THEREOF	1999/10/21	09/422,626
FABRICATION METHOD FOR FLASH MEMORY CELL	1999/10/22	09/425,395

Title	Filing/Issue Date	Serial/Patent No.
METHOD OF FABRICATING SELF-ALIGNED ULTRA SHORT CHANNEL	1999/10/22	09/426,923
METHOD OF REDUCING A CRITICAL DIMENSION OF A PATTERNED PHOTORESIST LAYER	1999/10/27	09/427,793
FABRICATION METHOD FOR ULTRA SHORT CHANNEL DEVICE COMPRISING SELF-ALIGNED LANDING PAD	1999/10/27	09/427,880
METHOD FOR MANUFACTURING TWO-BIT FLASH MEMORY	1999/10/28	09/428,356
METHOD OF FABRICATING HIGH VOLTAGE MOS DEVICE	1999/10/28	09/429,150
METHOD OF FABRICATING MOS TRANSISTOR	1999/10/29	09/430,730
METHOD OF FABRICATING A SPLIT GATE FLASH MEMORY DEVICE	1999/10/29	09/432,024
METHOD OF MANUFACTURING FLASH MEMORY	1999/11/4	09/433,955
ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR MULTI-VOLTAGE POWER SUPPLY CIRCUIT	1999/11/4	09/433,996
FABRICATION METHOD FOR A SEMICONDUCTOR DEVICE COMPRISING GATE OXIDE LAYERS OF VARIOUS THICKNESSES	1999/11/4	09/434,033
METHOD OF MANUFACTURING BINARY PHASE SHIFT MASK	1999/11/4	09/434,046
APPARATUS FOR AVOIDING PLASMA DAMAGE ON A WAFER	1999/11/8	09/435,724
METHOD OF FORMING SELF-ALIGNED DRAM CELL	1999/11/12	09/437,952
METHOD TO REDUCE INVERSE-NARROW-WIDTH-EFFECT	1999/11/12	09/439,032
FABRICATION METHOD FOR SELF-ALIGNED SILICIDE	1999/11/12	09/439,557
METHOD FOR FORMING DYNAMIC RANDOM ACCESS MEMORY DEVICE WITH AN ULTRA-SHORT CHANNEL AND AN ULTRA-SHALLOW JUNCTION	1999/11/12	09/439,791
FABRICATION METHOD FOR A DUAL DAMASCENE COMPRISING AN AIR-GAP	1999/11/12	09/439,930
MASK WITH ALTERNATING SCATTERING BARS	1999/11/18	09/442,839
OPTICAL PROXIMITY CORRECTION OF PATTERN ON NEGATIVE PHOTORESIST	1999/11/18	09/442,861
THREE-PHASE PHASE SHIFT MASK	1999/11/22	09/444,466
MULTI-LAYER POLYSILICON PLUG AND METHOD FOR MAKING THE SAME	1999/11/22	09/447,325
FABRICATION METHOD FOR A TWO-BIT FLASH MEMORY CELL	1999/11/24	09/449,297
MONITOR METHOD FOR TESTING PROBE PINS	1999/11/30	09/449,662
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORY	1999/11/30	09/451,136
METHOD FOR FORMING A STACKED CAPACITOR	1999/11/30	09/451,425
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORY	1999/11/30	09/451,426

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Title	Filing/Issue Date	Serial/Patent No.
METHOD OF FORMING DUAL DAMASCENE STRUCTURE	1999/12/3	09/454,005
FLUID DELIVERING SYSTEM	1999/12/3	09/454,261
METHOD OF REMOVING POLYMER RESIDUES AFTER TUNGSTEN ETCH BACK	1999/12/3	09/455,006
FABRICATION METHOD FOR A MULTILEVEL INTERCONNECT STRUCTURE	1999/12/7	09/455,719
METHOD FOR REMOVING PHOTORESIST IN METALLIZATION PROCESS	1999/12/7	09/455,721
METHOD OF MANUFACTURING METALLIC INTERCONNECTS	1999/12/9	09/457,561
FABRICATION METHOD FOR A SHALLOW TRENCH ISOLATION STRUCTURE	1999/12/9	09/457,578
FABRICATION METHOD FOR A SHALLOW TRENCH ISOLATION STRUCTURE	1999/12/20	09/460,178
METHOD FOR ISOLATING A HIGH-VOLTAGE DEVICE BY UTILIZING A SHIELDING EFFECT	1999/12/15	09/464,504
METHOD FOR MANUFACTURING A COMB-SHAPED LOWER ELECTRODE FOR A DRAM CAPACITOR	1998/11/24	5,840,606
FLASH MEMORY CELL STRUCTURE HAVING A HIGH GATE-COUPLING COEFFICIENT AND A SELECT GATE	1998/12/22	5,852,313
METHOD OF FABRICATING SPLIT-GATE FLASH MEMORY	1999/1/5	5,856,224
METHOD OF MANUFACTURING A SPLIT-GATE FLASH MEMORY CELL	1999/2/16	5,872,036
METHOD OF FABRICATING A BURIED BIT LINE	1999/3/16	5,882,972
METHOD OF REDUCING FRINGE CAPACITANCE	1999/4/6	5,891,783
METHOD FOR FABRICATING FLASH MEMORY CELLS	1999/5/4	5,899,718
SUB-MICRON MOSFET	1999/5/4	5,899,719
SPLIT-GATE FLASH MEMORY CELL STRUCTURE	1999/5/25	5,907,172
METHOD OF INSPECTING A DEFECT ON A TRANSLUCID FILM	1999/5/25	5,907,397
PROCESS OF FABRICATING AN ANTIFUSE STRUCTURE	1999/6/22	5,915,171
FLASH MEMORY CELL STRUCTURE HAVING ELECTRICALLY ISOLATED STACKED GATE	1999/8/3	5,932,910
PROCESS FOR FABRICATING BOTTOM ELECTRODE OF CAPACITOR	1999/8/3	5,933,728
METHOD FOR MANUFACTURING ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/8/10	5,937,298
METHOD OF FABRICATING A STATIC RANDOM ACCESS MEMORY	1999/8/24	5,943,566
TEST CONNECTING DEVICE INCLUDING TESTKEY AND PROBE CARD FOR USE IN THE TESTING OF INTEGRATED CIRCUITS	1999/9/7	5,949,240
METHOD FOR FABRICATING A DYNAMIC RANDOM ACCESS MEMORY WITH A VERTICAL PASS TRANSISTOR	1999/9/28	5,960,282

Title	Filing/Issue Date	Serial/Patent No.
FLASH EEPROM DEVICE	1999/9/28	5,960,285
METHOD OF FABRICATING ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/9/28	5,960,288
DRAM PROCESS WITH A MULTILAYER STACK STRUCTURE	1999/10/12	5,966,600
TECHNIQUES FOR REDUCED DISHING IN CHEMICAL MECHANICAL POLISHING	1999/10/19	5,968,842
METHOD OF MANUFACTURING A FLASH MEMORY CELL HAVING A TUNNEL OXIDE WITH A LONG NARROW TOP PROFILE	1999/10/26	5,972,752
METHOD FOR MANUFACTURING MOS TRANSISTOR	1999/10/26	5,972,764
METHOD OF FABRICATING AN ELECTRICALLY ERASABLE AND PROGRAMMABLE READ-ONLY MEMORY(EEPROM) WITH IMPROVED QUALITY FOR THE TUNNELING OXIDE LAYER THEREIN	1999/11/2	5,976,935
METHOD FOR MANUFACTURING CMOS	1999/11/9	5,981,325

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ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

United Semiconductor Corp., A Taiwanese corporation having a place of business at No. 3, Li-Hsin Rd. 2, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C., (hereafter ASSIGNOR) has been assigned or otherwise has an ownership interest in certain new and useful improvements as set forth in the patents and patent applications listed in attached Appendix A.

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, ASSIGNOR hereby:

1) Sell(s), assign(s) and transfer(s) to United Microelectronics Corp., a Taiwanese corporation having a place of business at No. 3, Li-Hsin Rd. 2, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C. (hereinafter referred to as "ASSIGNEE") the entire right, title and interest in any and all improvements and inventions disclosed in, application(s) based upon, and Patent(s) (including foreign patents) granted upon the information which is disclosed therein.

2) Authorize and request the Commissioner of Patents to issue any and all Letters Patents resulting from said application(s) or any division(s), continuation(s), substitute(s), re-examination(s) or reissue(s) thereof to the ASSIGNEE.

3) Agree to execute all papers and documents and, entirely at the ASSIGNEE's expense, perform any acts which are reasonably necessary in connection with the prosecution of said application(s), as well as any derivative and applications thereof, foreign applications based thereon, and/or the enforcement of patents resulting from such applications.

4) Agree that the terms, covenants and conditions of this assignment shall inure to the benefit of the ASSIGNEE, its successors, assigns and other legal representative(s), and shall be binding upon the inventor(s), as well as the inventor's heirs, legal representatives and assigns.

5) Warrant and represent that ASSIGNOR has not entered, and will not enter into any assignment, contract, or understanding that conflicts with this assignment.

Signed on the date(s) indicated beside my (our) signature(s).

United Semiconductor Corp.

By: _____ Date: December 30, 1999

Typed Name: Peter Chang
President
United Semiconductor Corp.

Witnesses:

Signature _____ Date: December 30, 1999

Wilson H.L. Lee
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Signature _____ Date: December 30, 1999

Felix Yeh
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Taipei, Taiwan, R.O.C.

Appendix A

Title	Filing/Issue Date	Serial/Patent No.
METHOD OF FORMING FLUOROSILICATE GLASS (FSG) LAYERS WITH MOISTURE-RESISTANT CAPABILITY	1997/6/5	08/868,752
METHOD OF REMOVING SILICON CARBIDE FROM DAMAGED SILICON SUBSTRARE	1997/6/12	08/873,925
SHALLOW TRENCH ISOLATION FOR SEMICONDUCTOR DEVICES	1997/8/27	08/924,432
METHOD OF REDUCING CROSS CONTAMINATION IN ION IMPLANTORS	1997/11/7	08/965,783
METHOD AND CONTROLLING SYSTEM FOR PREVENTING THE SCRATCHING OF WAFER BACKS BY THE FETCH ARM OF A STEPPER MACHINE	1997/12/16	08/991,187
METHOD FOR FORMING ETOX CELL USING SELF-ALIGNED SOURCE ETCHING PROCESS	1997/12/18	08/992,884
ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1997/12/24	08/998,000
IMPROVED METHOD OF ETCHING	1997/12/29	08/998,769
FABRICATING METHOD FOR FIELD OXIDE ISOLATION DEVICE	1997/12/29	08/999,135
METHOD FOR IMPROVING DIFFERENTIAL ETCHING RATE OF A METALLIC LAYER	1997/12/30	09/000,966
METHOD OF MANUFACTURING SHALLOW TRENCH ISOLATION	1998/1/20	09/008,858
METHOD FOR PREVENTING THE FORMATION OF RECESSES IN BOROPHOSPHOSILICATE GLASS	1998/2/13	09/023,235
METHOD FOR FABRICATING CAPACITOR	1998/2/13	09/023,879
METHOD OF FABRICATING FLASH MEMORY CELL	1998/2/17	09/024,163
FLASH MEMORY CELL	1998/2/17	09/024,782
MANUFACTURING METHOD FOR A THIN FILM WITH AN ANTI-REFLECTION ROUGH SURFACE	1998/3/2	09/033,113
METHOD OF FABRICATING A SPLIT GATE FLASH MEMORY DEVICE	1998/3/2	09/033,376
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1998/3/18	09/040,912
METHOD OF FORMING A SELF-ALIGNED CONTACT IN SEMICONDUCTOR FABRICATIONS	1998/3/23	09/046,059
METHOD OF NITRIDE-SEALED OXIDE –BUFFERED LOCAL OXIDATION OF SILICON	1998/3/26	09/048,697
METHOD OF GROW SELF-ALIGNED SILICON ON A POLY-GATE, SOURCE AND DRAIN REGION	1998/3/26	09/048,924
METHOD FOR MANUFACTURING DRAM CAPACITOR	1998/4/3	09/054,836
METHOD OF FABRICATING STORAGE CAPACITOR FOR DYNAMIC RANDOM ACCESS MEMORY	1998/4/3	09/054,837
METHOD FOR MANUFACTURING DRAM CAPACITOR	1998/4/10	09/058,579
NON-FURNACE CURING PROCESS OS LOW K KIELECTRIC MATERIAL WITH IMPLANT TREATMENT FOR THERMAL	1998/4/14	09/059,684

Title	Filing/Issue Date	Serial/Patent No.
STABILITY LOW K AND RIA POISON IMPROREMENT		
INVERCE-π CAPACITOR WITH RUGGED-POLY SARFACE	1998/4/4	09/059,686
METHOD FOR MANUFACTURING CAPACITOR'S LOWER ELECTRODE	1998/4/17	09/061,658
ETCHING MACHINE HAVING LOWER ELECTRODE BIAS VOLTAGE SOURCE	1998/4/17	09/062,116
METHOD FOR FORMING METALLIC LAYER	1998/4/21	09/063,672
METHOD OF FABRICATING DUAL CYLINDRICAL CAPACITOR	1998/4/24	09/066,196
DUAL CYLINDRICAL CAPACITOR	1998/4/24	09/066,197
METHOD OF PLANARIZING DIELECTRIC LAYER	1998/4/27	09/067,548
METHOD OF FABRICATING STACK CAPACITOR	1998/4/30	09/070,374
STACK CAPACITOR	1998/4/30	09/070,375
METHOD OF FORMING SHALLOW TRENCH ISOLATION	1998/5/6	09/073,708
METHOD OF MANUFACTURING SELF-ALIGNED SILICIDE	1998/5/8	09/075,420
METHOD OF FABRICATING SPLIT-GATE SOURCE SIDE INJECTION FLASH MEMORY ARRAY	1998/5/12	09/076,672
FABRICATING METHOD OF NON-VOLATILE FLASH MEMORY DEVICE	1998/5/12	09/076,676
METHOD OF FABRICATING BIT LINE	1998/5/21	09/082,660
METHOD OF FABRICATING A CAPACITOR OVER A BIT LINE OF A DRAM	1998/6/2	09/089,245
METHOD FOR FABRICATING A CAPACITOR IN A DYNAMIC RANDOM ACCESS MEMORY	1998/6/24	09/103,957
THE NOVEL MEASUREMENT METHOD OF KIND (HUMP) EFFECT IN EFFECT IN SECONDARY APPROACH	1998/6/30	09/106,745
THE METHOD OF KIND EFFECT WITH CHANNEL WIDTH MODULATIN IN EXTRAPOLATION	1998/6/30	09/106,752
TOOL FOR INSPECTING BROKEN WAFER EDGES	1998/6/9	09/107,164
METHOD OF FORMING A VIA	1998/7/10	09/113,471
STRUCTURE OF BURIED BIT LINE	1998/7/10	09/113,844
PREHEATING METHOD FOR HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION	1998/7/17	09/118,054
METHOD FOR FABRICATING A VIA	1998/8/11	09/132,384
METHOD OF FABRICATING DOUBLE DOPED SOURCE REGION	1998/3/2	09/133,148
METHOD OF REDUCING THE REFLECTIVITY AND SWING EFFECT OF WAFER SURFACES IN A PHOTOLITHOGRAPHIC PROCESS	1998/8/19	09/136,566
METHOD OF FABRICATING CAPACITOR	1998/8/20	09/137,028
METHOD OF FABRICATING FLASH ELECTRICALLY-ERASABLE AND PROGRAMMABLE READ-ONLY MEMORY (EEPROM) DEVICE	1998/8/24	09/138,757

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Title	Filing/Issue Date	Serial/Patent No.
METHOD FOR ETCHING (AS AMENDED)	1998/8/24	09/138,758
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1998/8/25	09/140,114
ARCHITECTURE OF POLY FUSES	1998/9/9	09/149,929
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/9/14	09/152,360
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/9/14	09/152,450
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1998/10/1	09/164,288
HIGH VOLTAGE DEVICE	1998/10/1	09/164,690
SETUP FOR REMOVING SLURRY FROM A POLISHING PAD	1998/10/14	09/172,280
METHOD OF COATING AMORPHOUS SILICON FILM	1998/10/30	09/183,061
METHOD OF FABRICATING HIGH VOLTAGE SEMICONDUCTOR DEVICE	1998/10/30	09/183,062
CHEMICAL MECHANICAL POLISHING METHOD	1998/11/4	09/185,808
METHOD OF FABRICATING AN INTEL TYPE FLASH ERASABLE PROGRAMMABLE READ ONLY MEMORY CELL	1998/11/4	09/185,941
METHOD FOR FABRICATING A NON-VOLATILE MEMORY DEVICE	1998/11/4	09/186,129
METHOD OF REMOVING RESIDUE ON A BONDING PAD	1998/11/5	09/186,531
METHOD OF FABRICATING A FLASH MEMORY CELL	1998/11/5	09/186,743
METHOD OF MENDING EROSION OF BONDING PAD	1998/11/5	09/186,744
FLASH MEMORY STRUCTURE AND METHOD OF MANUFACTURE	1998/11/5	09/186,748
ANTI-LEAKAGE APPARATUS	1998/11/6	09/186,999
METHOD FOR FABRICATING A PASSIVATION LAYER	1998/11/6	09/187,958
STRUCTURE OF A FLASH MEMORY	1998/11/13	09/191,326
METHOD OF FORMING HEMISPHERICAL GRAIN POLYSILICON OVER LOWER ELECTRODE CAPACITOR	1998/11/13	09/191,327
METHOD OF MANUFACTURING FLASH MEMORY CELLS	1998/11/13	09/191,798
EEPROM CELL STRUCTURE	1998/11/13	09/191,933
METHOD FOR ANALYZING A CONSEQUENT EFFECT OF A FABRICATION MACHINE CLUSTER	1998/11/25	09/200,330
METHOD OF FABRICATING A DRAM CAPACITOR	1998/12/4	09/206,109
METHOD FOR FABRICATING A TRANSISTOR	1998/12/4	09/206,111
METHOD OF FABRICATING BIT LINES BY DAMASCENE	1998/12/4	09/206,112
METHOD OF FORMING A SHALLOW TRENCH ISOLATION	1998/12/4	09/206,182
FLASH MEMORY STRUCTURE	1998/12/17	09/213,344
METHOD OF MANUFACTURING A FLASH MEMORY STRUCTURE	1998/12/17	09/213,345
METHOD OF FABRICATING METAL OXIDE	1998/12/17	09/213,599

Title	Filing/Issue Date	Serial/Patent No.
SEMICONDUCTOR		
METHOD OF FABRICATING A FLASH MEMORY	1998/12/17	09/213,600
METHOD OF FORMING A SHALLOW TRENCH ISOLATION	1998/12/17	09/213,700
METHOD OF FABRICATING A DYNAMIC RANDOM ACCESS MEMORY CAPACITOR	1998/12/17	09/213,783
METHOD FOR BOTTOM ELECTRODE OF CAPACITOR	1998/12/17	09/213,934
METHOD OF FABRICATING AN ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT	1998/12/17	09/215,599
DYANMIC RANDOM ACCESS MEMORY CAPACITOR	1998/12/17	09/215,619
METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION STRUCTURE	1998/12/30	09/223,200
METHOD FOR FABRICATING A METAL VIA	1998/12/30	09/223,328
METHOD FOR FORMING VIA HOLE	1998/12/30	09/223,330
SPIN-ON-GLASS PLANARIZATION	1998/12/30	09/223,334
METHOD OF FABRICATING FLASH ERASABLE PROGRAMMABLE READ ONLY MEMORY	1998/12/30	09/223,337
PLANARIATION PROCESS	1998/12/30	09/223,398
METHOD FOR FORMING FLASH MEMORY CELL	1998/12/30	09/223,613
A METHOD FOR FORMING A VIA	1999/1/8	09/227,347
METHOD FOR FORMING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/8	09/227,379
ETCHING PROCESS	1999/1/8	09/227,627
SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/8	09/227,660
METHOD FOR FABRICATING A FLASH MEMORY	1999/1/8	09/227,680
METHOD FOR FABRICATING A FLASH MEMORY	1999/1/8	09/227,974
METHOD FOR FORMING A VIA	1999/1/8	09/227,975
FLASH MEMORY STRUCTURE	1999/1/22	09/235,261
METHOD OF FORMING SHALLOW TRENCH ISOLATION	1999/1/22	09/235,268
METHOD OF FORMING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/1/25	09/236,951
METHOD OF MANUFACTURING SHALLOW TRENCH ISOLATION	1999/1/25	09/236,955
METHOD OF COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR	1999/1/25	09/236,962
SELF-ALIGNED SILICIDE PROCESS	1999/1/25	09/237,211
METHOD FOR FABRICATING FLASH MEMORY	1999/1/25	09/237,295
METHOD OF REMOVING CARBON CONTAMINATION ON SEMICONDUCTOR SUBSTRATE	1999/2/1	09/241,338
METHOD FOR MANUFACTURING A CYLINDRICAL CAPACITOR	1999/2/1	09/241,522
TRIPLE WELL STRUCTURE	1999/2/1	09/241,524

Title	Filing/Issue Date	Serial/Patent No.
SURFACE TREATMENT FOR BONDING PAD	1999/2/1	09/241,525
METHOD FOR FORMING HEMISPHERICAL SILICON GRAINS ON DESIGNATED AREAS OF SILICON LAYER	1999/2/1	09/241,526
METHOD FOR FABRICATING CONTACT HOLE	1999/2/1	09/241,527
METHOD FOR REMOVING POLY DEFECT	1999/2/1	09/241,528
METHOD FOR FABRICATING A FLASH MEMORY	1999/2/1	09/241,544
DAMASCENE PROCESS	1999/2/1	09/241,742
ETCHING METHOD FOR DOPED POLYSILICON LAYER	1999/2/1	09/241,757
METHOD OF FORMING A FLASH MEMORY DEVICE	1999/2/1	09/241,759
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/2/1	09/241,760
METHOD FOR FORMING SHALLOW TRENCH ISOLATION	1999/2/1	09/241,789
METHOD OF REDUCING SALICIDE LATERAL GROWTH	1999/2/1	09/241,792
SELF-ALIGNED CONTACT PROCESS	1999/2/1	09/241,793
METHOD FOR FABRICATING SHALLOW TRENCH ISOLATION STRUCTURE	1999/2/1	09/241,977
METHOD FOR FORMING HEMISPHERICAL GRAINED SILICON STRUCTURE	1999/2/8	09/246,226
SHALLOW TRENCH ISOLATION	1999/2/8	09/246,278
METHOD FOR REMOVING PHOTORESIST	1999/2/8	09/246,737
METHOD OF MANUFACTURING PASSIVATION LAYER	1999/2/8	09/246,755
METHOD FOR FORMING SALICIDE LAYERS	1999/2/8	09/246,762
METHOD FOR FORMING INTER-METAL DIELECTRICS	1999/2/16	09/249,882
METHOD OF FABRICATING SELF-ALIGNED SILICIDE	1999/2/16	09/250,618
METHOD OF MANUFACTURING CAPACITOR FOR MIXED-MODE CIRCUIT DEVICE	1999/2/16	09/250,628
METHOD OF FABRICATING SHALLOW TRENCH ISOLATION	1999/2/16	09/250,749
METHOD OF MANUFACTURING BIT LINE	1999/2/16	09/252,600
METHOD FOR FABRICATING SELF-ALIGNED METAL PLUG	1999/3/1	09/260,628
METHOD FOR FABRICATING A SHALLOW TRENCH ISOLATION STRUCTURE	1999/3/2	09/261,094
METHOD OF FABRICATING A GATE STRUCTURE OF SEMICONDUCTOR DEVICE	1999/3/2	09/261,096
METHOD OF CHEMICAL-MECHANICAL POLISHING	1999/3/2	09/261,098
METHOD OF MANUFACTURING FLASH MEMORY	1999/3/11	09/267,760
METHOD OF FABRICATING BARRIER LAYER	1999/3/11	09/267,875
METHOD OF MANUFACTURING LINER INSULATING LAYER	1999/3/11	09/267,883
METHOD FOR FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/3/11	09/267,884

Title	Filing/Issue Date	Serial/Patent No.
METHOD FOR MONITORING DOSAGE/FOCUS/LEVELING	1999/3/16	09/270,278
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORIES	1999/3/16	09/270.027
METHOD FOR CLEANING A CHEMICAL VAPOR DEPOSITION CHAMBER	1999/3/18	09/272,013
METHOD OF FABRICATING FLASH MEMORY	1999/3/19	09/273,067
METHOD OF FABRICATING A DUAL DAMASCENE STRCUTURE	1999/3/23	09/274,603
IN AN INTEGRATED CIRCUIT		
SEMICONDUCTOR DEVICE WITH AN ANTI-DOPED REGION	1999/3/29	09/280,297
METHOD FOR FABRICATING A SELF-ALIGNED SILICIDE	1999/3/29	09/280,626
METHOD OF FABRICATING DUAL DAMASCENE STRUCTURE	1999/3/29	09/280,892
METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH AN ANTI-DOPED REGION	1999/3/29	09/282,018
METHOD OF FABRICATING SILICIDE LAYER ON GATE ELECTRODE	1999/4/5	09/286,004
METHOD OF MANUFACTURING INTERCONNECT	1999/4/5	09/286,005
METHOD OF FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/4/5	09/286,018
METHOD OF MANUFACTURING BOTTOM ELECTRODE	1999/4/5	09/286,021
METHOD OF MANUFACTURING FLASH MEMORY	1999/4/5	09/286,139
METHOD FOR IN-SITU REMOVING PHOTORESIST AND SIDEWALL POLYMER	1999/4/5	09/286,219
METHOD FOR MANUFACTURING SHALLOW TRENCH	1999/4/5	09/286,231
ISOLATION STRUCTURE		
METHOD OF FABRICATING SILICIDE LAYER	1999/4/5	09/286,687
METHOD FOR FABRICATING A FLASH MEMORY	1999/4/16	09/292,870
METHOD OF FABRICATING ANTI-REFLECTION LAYER	1999/4/16	09/292,871
SELF-ALIGNED METAL SILICIDE	1999/4/16	09/293,419
METHOD OF MANUFACTURING INTERCONNECT	1999/4/16	09/293,420
FULLY SELF-ALIGNED METHOD FOR FABRICATING TRANSISTOR AND MEMORY	1999/4/16	09/293,430
METHOD FOR FORMING A STACKED GATE	1999/4/16	09/293,434
METHOD OF FABRICATING SELF-ALIGNED METAL SILICIDE	1999/4/16	09/293,826
METHOD OF FORMING DIELECTRIC LAYER WITH LOW DIELECTRIC CONSTANT	1999/4/19	09/294,541
METHOD OF MANUFACTURING BOTTOM ELECTRODE	1999/4/20	09/295,067
OF CAPACITOR		
METHOD OF OPTICAL PROXIMITY CORRECTION	1999/4/23	09/298,324
METHOD FOR FABRICATING A HYBRID ISOLATION	1999/4/26	09/299,719

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STRUCTURE		
METHOD FOR FABRICATING CAPACITOR	1999/5/6	09/306,093
METHOD OF MANUFACTURING METAL-OXIDE SEMICONDUCTOR TRANSISTOR	1999/5/6	09/306,094
FLASH MEMORY	1999/5/6	09/306,119
METHOD OF MANUFACTURING INTERCONNECT	1999/5/6	09/306,130
EQUIPMENT AND METHOD FOR MORNITORING A WAFER SURFACE	1999/5/6	09/306,166
ELECTROSTATIC DISCHARGE PROTECTIVE CIRCUIT	1999/5/6	09/306,243
METHOD OF FABRICATING FLASH MEMORY	1999/5/6	09/306,348
TRANSISTOR STRUCTURE OF ESD PROTECTION DEVICE	1999/5/7	09/307,319
METHOD OF FABRICATING DUAL DAMASCENE	1999/5/10	09/309,186
METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR	1999/5/17	09/313,166
METHOD FOR FORMING GATE TERMINAL	1999/5/17	09/313,167
METHOD FOR FORMING CONDUCTIVE LINE	1999/5/17	09/313,510
METHOD OF FABRICATING FLASH MEMORY	1999/5/17	09/313,511
METHOD FOR FABRICATING PASSIVATION LAYER	1999/5/17	09/313,516
METHOD OF FABRICATING SEMICONDUCTOR DEVICE	1999/5/21	09/315,797
TEST KEY ARCHITECTURE	1999/5/21	09/316,196
METHOD FOR FABRICATING INTER-METAL DIELECTRIC LAYER	1999/5/21	09/316,475
STRUCTURE OF ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/5/21	09/316,584
METHOD OF FABRICATING PASSIVATION LAYER IN LIQUID CRYSTAL DISPLAY	1999/5/21	09/316,585
METHOD OF FABRICATING STORAGE NODE	1999/5/24	09/316,979
METHOD OF FABRICATING CAPACITOR	1999/5/27	09/322,051
METHOD OF FABRICATING METAL PLUG	1999/5/27	09/322,054
METHOD FOR FABRICATING FIELD EMISSION DISPLAY CATHODE	1999/5/27	09/322,055
METHOD FOR IMPROVING STABILITY OF ANTI-COATING LAYER	1999/6/4	09/325,365
METAL ETCHING PROCESS	1999/6/4	09/326,380
METHOD AND STRUCTURE FOR MEASURING A RELATIVE POSITIONAL DEVIATION OF A RETICLE PATTERN	1999/6/4	09/326,392
METHOD OF FABRICATING PASSIVATION OF GATE ELECTRODE	1999/6/8	09/328,056
METHOD FOR FABRICATING A GATE CONDUCTIVE STRUCTURE	1999/6/9	09/328,850
METHOD FOR FABRICATING SILICON-ON-INSULATOR STRUCTURE WITH SHALLOW TRENCH ISOLATION	1999/6/9	09/328,851

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STRUCTURE		
METHOD OF FABRICATING SEMICONDUCTOR DEVICE	1999/6/9	09/328,967
METHOD FOR MANUFACTURING EVEN DIELECTRIC LAYER	1999/6/9	09/328,977
METHOD OF FORMING UNLANDED VIA HOLE	1999/6/9	09/329,113
METHOD OF MANUFACTURING TRANSISTOR WITH T-SHAPED GATE ELECTRODE	1999/6/16	09/334,532
METHOD OF FORMING A CONTACT PLUG IN A SEMICONDUCTOR DEVICE	1999/6/18	09/335,808
FABRICATION METHOD OF A SELF-ALIGNED CONTACT WINDOW	1999/6/19	09/336,553
METHOD OF FABRICATING CONDUCTIVE LINE STRUCTURE	1999/6/19	09/336,554
METHOD OF MANUFACTURING INTERCONNECT	1999/6/28	09/340,928
METHOD FOR MANUFACTURING METAL OXIDE SEMICONDUCTOR TRANSISTOR HAVING RAISED SOURCE/DRAIN	1999/6/28	09/340,969
FABRICATION METHOD OF AN INTERCONNECT	1999/6/28	09/344,865
METHOD OF MANUFACTURING SALICIDE LAYER	1999/7/1	09/345,435
METHOD OF MANUFACTURING CONTACT PAD	1999/7/2	09/347,180
METHOD FOR FORMING POLYSILICON GATE ELECTRODE	1999/7/7	09/348,389
METHOD FOR FABRICATING PASSIVATION LAYER ON METAL PAD	1999/7/7	09/348,396
METHOD OF FABRICATING PRESERVE LAYER	1999/7/7	09/348,407
SHALLOW TRENCH ISOLATION PROCESS	1999/7/7	09/348,409
METHOD OF FABRICATING FLOATING GATE	1999/7/7	09/348,410
FOR FLASH MEMORY		
METHOD OF FABRICATING INTERCONNECT	1999/7/7	09/348,984
FABRICATION METHOD OF A GATE JUNCTION	1999/7/19	09/356,961
CONDUCTIVE STRUCTURE		
METHOD FOR STABILIZING A PLASMA MACHINE OPERATION	1999/7/23	09/360,076
METHOD OF MONITORING DEEP ULTRAVIOLET	1999/8/9	09/370,773
EXPOSURE SYSTEM		
METHOD FOR FORMING CROWN SHAPE CAPACITOR	1999/8/9	09/370,774
FABRICATION METHOD FOR A MOS DEVICE WITH REDUCED RESISTANCE	1999/8/10	09/371,470
CONVEYANCE ARM DEVICE	1999/8/10	09/372,431
FABRICATION METHOD FOR GATE STRUCTURE HAVING GATE DIELECTRIC LAYERS OF DIFFERENT THICKNESSES	1999/8/17	09/375,877
METHOD OF FABRICATING FLASH MEMORY	1999/8/23	09/379,382
FLASH MEMORY	1999/8/23	09/379,890

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METHOD OF FABRICATING A MOS TRANSISTOR	1999/8/25	09/383,033
METHOD FOR FABRICATING GATE OXIDE LAYER	1999/8/30	09/385,805
METHOD OF FABRICATING MULTILEVEL INTERCONNECT	1999/9/3	09/389,823
METHOD FOR MANUFACTURING DYNAMIC RANDOM ACCESS MEMORY	1999/9/3	09/389,824
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/9/9	09/392,924
LIFETIME MEASUREMENT OF AN ULTRA-THIN DIELECTRIC LAYER	1999/9/9	09/393,054
METHOD TO REDUCE PARASITIC CAPACITANCE	1999/9/13	09/394,636
METHOD FOR MANUFACTURING BIT LINE AND BIT LINE CONTACT	1999/9/13	09/394,637
METHOD OF FABRICATING PASSIVATION LAYER	1999/9/14	09/395,442
METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION	1999/9/15	09/396,140
METHOD FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE	1999/9/15	09/397,161
POST-ETCHING CLEANING PROCESS	1999/9/23	09/404,113
METHOD OF FABRICATING PROTECTION STRUCTURE	1999/9/28	09/406,356
METHOD OF PROTECTING A WELL AT A FLOATING STAGE	1999/9/28	09/406,517
METHOD OF FORMING A SELF-ALIGNED SILICIDE STRUCTURE IN INTEGRATED CIRCUIT FABRICATION	1999/9/29	09/408,152
RETARDATION LAYER FOR PREVENTING DIFFUSION OF METAL LAYER AND FABRICATION METHOD THEROF	1999/9/30	09/408,612
ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH A REDUCED TRIGGER VOLTAGE	1999/10/4	09/411,993
AN POLYSILICON ETCHING METHOD	1999/10/5	09/412,872
METHOD OF MANUFACTURING A TANTALUM OXIDE FILM	1999/10/8	09/414,741
METHOD FOR INCREASING SURFACE AREA OF A BOTTOM ELECTRODE FOR A DRAM	1999/10/8	09/415,564
METHOD OF FABRICATING DUAL DAMASCENE	1999/10/12	09/417,830
METHOD TO MAINTAIN CONSISTENT THICKNESS OF THIN FILM DEPOSITED BY CHEMICAL VAPOR DEPOSITION	1999/10/20	09/420,961
METHOD OF FORMING SEMICONDUCTOR DEVICE CONTACT	1999/10/20	09/421,312
METHOD FOR REDUCING INVERSE-NARROW-WIDTH-EFFECT	1999/10/20	09/421,842
METHOD FOR FABRICATING A DYNAMIC RANDOM ACCESS MEMORY CELL	1999/10/21	09/422,577
METHOD OF FORMING A FLASH MEMORY	1999/10/21	09/422,625
THREE-DIMENSIONAL FLASH MEMORY STRUCTURE AND FABRICATION METHOD THEREOF	1999/10/21	09/422,626
FABRICATION METHOD FOR FLASH MEMORY CELL	1999/10/22	09/425,395

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METHOD OF FABRICATING SELF-ALIGNED ULTRA SHORT CHANNEL	1999/10/22	09/426,923
METHOD OF REDUCING A CRITICAL DIMENSION OF A PATTERNED PHOTORESIST LAYER	1999/10/27	09/427,793
FABRICATION METHOD FOR ULTRA SHORT CHANNEL DEVICE COMPRISING SELF-ALIGNED LANDING PAD	1999/10/27	09/427,880
METHOD FOR MANUFACTURING TWO-BIT FLASH MEMORY	1999/10/28	09/428,356
METHOD OF FABRICATING HIGH VOLTAGE MOS DEVICE	1999/10/28	09/429,150
METHOD OF FABRICATING MOS TRANSISTOR	1999/10/29	09/430,730
METHOD OF FABRICATING A SPLIT GATE FLASH MEMORY DEVICE	1999/10/29	09/432,024
METHOD OF MANUFACTURING FLASH MEMORY	1999/11/4	09/433,955
ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR MULTI-VOLTAGE POWER SUPPLY CIRCUIT	1999/11/4	09/433,996
FABRICATION METHOD FOR A SEMICONDUCTOR DEVICE COMPRISING GATE OXIDE LAYERS OF VARIOUS THICKNESSES	1999/11/4	09/434,033
METHOD OF MANUFACTURING BINARY PHASE SHIFT MASK	1999/11/4	09/434,046
APPARATUS FOR AVOIDING PLASMA DAMAGE ON A WAFER	1999/11/8	09/435,724
METHOD OF FORMING SELF-ALIGNED DRAM CELL	1999/11/12	09/437,952
METHOD TO REDUCE INVERSE-NARROW-WIDTH-EFFECT	1999/11/12	09/439,032
FABRICATION METHOD FOR SELF-ALIGNED SILICIDE	1999/11/12	09/439,557
METHOD FOR FORMING DYNAMIC RANDOM ACCESS MEMORY DEVICE WITH AN ULTRA-SHORT CHANNEL AND AN ULTRA-SHALLOW JUNCTION	1999/11/12	09/439,791
FABRICATION METHOD FOR A DUAL DAMASCENE COMPRISING AN AIR-GAP	1999/11/12	09/439,930
MASK WITH ALTERNATING SCATTERING BARS	1999/11/18	09/442,839
OPTICAL PROXIMITY CORRECTION OF PATTERN ON NEGATIVE PHOTORESIST	1999/11/18	09/442,861
THREE-PHASE PHASE SHIFT MASK	1999/11/22	09/444,466
MULTI-LAYER POLYSILICON PLUG AND METHOD FOR MAKING THE SAME	1999/11/22	09/447,325
FABRICATION METHOD FOR A TWO-BIT FLASH MEMORY CELL	1999/11/24	09/449,297
MONITOR METHOD FOR TESTING PROBE PINS	1999/11/30	09/449,662
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORY	1999/11/30	09/451,136
METHOD FOR FORMING A STACKED CAPACITOR	1999/11/30	09/451,425
METHOD OF FABRICATING DYNAMIC RANDOM ACCESS MEMORY	1999/11/30	09/451,426

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METHOD OF FORMING DUAL DAMASCENE STRUCTURE	1999/12/3	09/454,005
FLUID DELIVERING SYSTEM	1999/12/3	09/454,261
METHOD OF REMOVING POLYMER RESIDUES AFTER TUNGSTEN ETCH BACK	1999/12/3	09/455,006
FABRICATION METHOD FOR A MULTILEVEL INTERCONNECT STRUCTURE	1999/12/7	09/455,719
METHOD FOR REMOVING PHOTORESIST IN METALLIZATION PROCESS	1999/12/7	09/455,721
METHOD OF MANUFACTURING METALLIC INTERCONNECTS	1999/12/9	09/457,561
FABRICATION METHOD FOR A SHALLOW TRENCH ISOLATION STRUCTURE	1999/12/9	09/457,578
FABRICATION METHOD FOR A SHALLOW TRENCH ISOLATION STRUCTURE	1999/12/20	09/460,178
METHOD FOR ISOLATING A HIGH-VOLTAGE DEVICE BY UTILIZING A SHIELDING EFFECT	1999/12/15	09/464,504
METHOD FOR MANUFACTURING A COMB-SHAPED LOWER ELECTRODE FOR A DRAM CAPACITOR	1998/11/24	5,840,606
FLASH MEMORY CELL STRUCTURE HAVING A HIGH GATE-COUPLING COEFFICIENT AND A SELECT GATE	1998/12/22	5,852,313
METHOD OF FABRICATING SPLIT-GATE FLASH MEMORY	1999/1/5	5,856,224
METHOD OF MANUFACTURING A SPLIT-GATE FLASH MEMORY CELL	1999/2/16	5,872,036
METHOD OF FABRICATING A BURIED BIT LINE	1999/3/16	5,882,972
METHOD OF REDUCING FRINGE CAPACITANCE	1999/4/6	5,891,783
METHOD FOR FABRICATING FLASH MEMORY CELLS	1999/5/4	5,899,718
SUB-MICRON MOSFET	1999/5/4	5,899,719
SPLIT-GATE FLASH MEMORY CELL STRUCTURE	1999/5/25	5,907,172
METHOD OF INSPECTING A DEFECT ON A TRANSLUCID FILM	1999/5/25	5,907,397
PROCESS OF FABRICATING AN ANTIFUSE STRUCTURE	1999/6/22	5,915,171
FLASH MEMORY CELL STRUCTURE HAVING ELECTRICALLY ISOLATED STACKED GATE	1999/8/3	5,932,910
PROCESS FOR FABRICATING BOTTOM ELECTRODE OF CAPACITOR	1999/8/3	5,933,728
METHOD FOR MANUFACTURING ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/8/10	5,937,298
METHOD OF FABRICATING A STATIC RANDOM ACCESS MEMORY	1999/8/24	5,943,566
TEST CONNECTING DEVICE INCLUDING TESTKEY AND PROBE CARD FOR USE IN THE TESTING OF INTEGRATED CIRCUITS	1999/9/7	5,949,240
METHOD FOR FABRICATING A DYNAMIC RANDOM ACCESS MEMORY WITH A VERTICAL PASS TRANSISTOR	1999/9/28	5,960,282

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FLASH EEPROM DEVICE	1999/9/28	5,960,285
METHOD OF FABRICATING ELECTROSTATIC DISCHARGE PROTECTION DEVICE	1999/9/28	5,960,288
DRAM PROCESS WITH A MULTILAYER STACK STRUCTURE	1999/10/12	5,966,600
TECHNIQUES FOR REDUCED DISHING IN CHEMICAL MECHANICAL POLISHING	1999/10/19	5,968,842
METHOD OF MANUFACTURING A FLASH MEMORY CELL HAVING A TUNNEL OXIDE WITH A LONG NARROW TOP PROFILE	1999/10/26	5,972,752
METHOD FOR MANUFACTURING MOS TRANSISTOR	1999/10/26	5,972,764
METHOD OF FABRICATING AN ELECTRICALLY ERASABLE AND PROGRAMMABLE READ-ONLY MEMORY(EEPROM) WITH IMPROVED QUALITY FOR THE TUNNELING OXIDE LAYER THEREIN	1999/11/2	5,976,935
METHOD FOR MANUFACTURING CMOS	1999/11/9	5,981,325