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U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks. Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):
DynaChip Corporation

00 APR 20 PM 12: 19

CPD/FINANCE

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

2. Name and address of receiving party(ies):

Name: **Xilinx, Inc.**

Internal Address:

Street Address: **2100 Logic Drive**

City: **San Jose** State: **California** Zip: **95124**

Additional name(s) & address(es) attached? [ ] Yes [**X**] No

3. Nature of Conveyance:

[X] Assignment [ ] Merger
[ ] Security Agreement [ ] Change of Name
[ ] Other

Execution Date: March 31, 2000

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the filing date of the application is:

A. Patent Application No.(s)

B. Patent No.(s)

5,355,035; 5,397,943; 5,406,133; 5,497,108
5,504,440; 5,570,059; 5,614,844; 5,654,665
5,668,495; 5,742,179; 5,744,981; 5,808,479
5,883,852; 5,940,606; 6,002,268; 6,025,736

Additional numbers attached? [ ] Yes [X] No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: **EDEL M. YOUNG**

Internal Address: **Xilinx, Inc.**

Street Address: **2100 Logic Drive**

City: **San Jose** State: **California** Zip: **95124**

6. Total number of applications and patents involved: 16

7. Total fee (37 CFR 3.41):.....$ $640.00

[ ] Enclosed
[X] Authorized to be charged to deposit account

8. Deposit Account Number: **24-0040**

(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

EDEL M. YOUNG, 32,451
Name of Person Signing

Edel M Young
Signature

April 14, 2000
Date

Total number of pages including cover sheet, attachments, and document: [5]

MOM

Mail documents to be recorded with required cover sheet information to

Assistant Commissioner for Patents, Box Assignments
Washington. D. C. 20231

05/10/2000 DNGUYEN 00000152 240040 5355035
01 FC:581 640.00 CH

U.S. PATENT ASSIGNMENT

This Patent Assignment (this "**Assignment**") is made as of March 31, 2000 by DynaChip Corporation, a California corporation ("**Assignor**"), having a principal place of business at 1255 Oakmead Parkway, Sunnyvale, California 94086, to Xilinx, Inc., a Delaware corporation ("**Assignee**"), having a principal place of business at 2100 Logic Drive, San Jose, California 95124.

RECITALS

A. Assignor and Assignee have entered into an Asset Purchase Agreement of even date herewith (the "**Purchase Agreement**").

B. Pursuant to the Purchase Agreement, Assignor desires to assign to Assignee all of Assignor's right, title and interest in and to the patents issued by the United States Patent and Trademark Office and set forth on Exhibit A hereto (the "**Patents**"), together with the goodwill of the business pertaining thereto.

AGREEMENT

NOW, THEREFORE, in consideration of the foregoing premises, the mutual covenants and agreements contained in the Purchase Agreement and the covenants and agreements in this Assignment and to induce Assignee to consummate the transactions contemplated by the Purchase Agreement, Assignor agrees as follows:

1. Assignor does hereby sell, transfer, convey, assign and deliver to Assignee all of Assignor's right, title and interest in and to the Patents, including any foreign counterparts, divisions, continuations or reissues thereof, together with the goodwill of the business pertaining thereto, the same to be held by Assignee for Assignee's own use and enjoyment, and for the use and enjoyment of Assignee's successors, assigns and other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor if this Assignment and sale had not been made, together with all claims for damages by reason of past infringements of the Patents, along with the right to sue for and collect such damages for the use and benefit of Assignee and its successors, assigns and other legal representatives.

IN WITNESS WHEREOF, Assignor has executed this Assignment on the date first above written.

DYNACHIP CORPORATION

By: Richard G. Couch

Name: Richard G. Couch

Title: Chief Executive Officer

Acknowledgment by Notary Public

State of California

County of Contra Costa

On this 30 day of March, 2000, before me, the undersigned Notary Public, personally appeared Richard E Couch, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument, and acknowledged to me that he executed the same.

Seal:

Signature: T Adams

Name: T Adams, Notary Public

T. ADAMS
Commission # 1228323
Notary Public - California
Contra Costa County
My Comm. Expires Jul 10, 2003

EXHIBIT A – U.S. Patents

PATENT NO.:	**5,355,035**
ISSUE DATE:	Oct. 11, 1994
TITLE:	High Speed BiCMOS Switches And Multiplexers
INVENTOR(S):	Madhukar B. Vora; Burnell G. West
PATENT NO.:	**5,397,943**
ISSUE DATE:	Mar. 14, 1985
TITLE:	Clock Distribution Method And Apparatus For High Speed Circuits With Low Skew Using Counterpropaging True And Complement Re-Generated Clock Signals With Predetermined Ramp Shapes
INVENTOR(S):	Burnell G. West; Madhukar B. Vora
PATENT NO.:	**5,406,133**
ISSUE DATE:	Apr. 11, 1995
TITLE:	BiCMOS Reprogrammable Logic
INVENTOR(S):	Madhukar B. Vora; Burnell G. West
PATENT NO.:	**5,497,108**
ISSUE DATE:	Mar. 5, 1996
TITLE:	BiCMOS Repeater Circuit For A Programmable Logic Device
INVENTOR(S):	Suresh M. Menon; Stanley Wilson; Tsung C. Whang
PATENT NO.:	**5,504,440**
ISSUE DATE:	Apr. 2, 1996
TITLE:	High Speed Programmable Logic Architecture
INVENTOR(S):	Paul T. Sasaki
PATENT NO.:	**5,570,059**
ISSUE DATE:	Oct. 29, 1996
TITLE:	BiCMOS Multiplexers And Crossbar Switches
INVENTOR(S):	Madhukar B. Vora; Burnell G. West
PATENT NO.:	**5,614,844**
ISSUE DATE:	Mar. 25, 1997
TITLE:	High Speed Programmable Logic Architecture
INVENTOR(S):	Paul T. Sasaki; Suresh M. Menon; Tsung C. Whang
PATENT NO.:	**5,654,665**
ISSUE DATE:	Aug. 5, 1997
TITLE:	Programmable Logic Bias Driver
INVENTOR(S):	Suresh M. Menon; Tsung C. Whang
PATENT NO.:	**5,668,495**
ISSUE DATE:	Sep. 16, 1997
TITLE:	BiCMOS Reprogrammable Logic
INVENTOR(S):	Madhukar B. Vora; Burnell G. West
PATENT NO.:	**5,742,179**
ISSUE DATE:	Apr. 21, 1998
TITLE:	High Speed Programmable Logic Architecture
INVENTOR(S):	Paul T. Sasaki

EXHIBIT A - U.S. Patents (cont'd.)

PATENT NO.: **5,744,981**
ISSUE DATE: Apr. 28, 1998
TITLE: Programmable Logic Cell With Input Polarity Control
INVENTOR(S): Paul T. Sasaki; Suresh M. Menon; Tsung C. Whang

PATENT NO.: **5,808,479**
ISSUE DATE: Sep. 15, 1998
TITLE: High Speed Programmable Logic Architecture
INVENTOR(S): Paul T. Sasaki; Suresh M. Menon; Tsung C. Whang

PATENT NO.: **5,883,852**
ISSUE DATE: Mar. 16, 1999
TITLE: Configurable SRAM For Field Programmable Gate Array
INVENTOR(S): Atul V. Ghia; Paul Takao Sasaki

PATENT NO.: **5,940,606**
ISSUE DATE: Aug. 17, 1999
TITLE: Duty Cycle Controller For Clock Signal To Synchronous SRAM On FPGA
INVENTOR(S): Atul V. Ghia; Suresh M. Menon

PATENT NO.: **6,002,268**
ISSUE DATE: Dec. 14, 1999
TITLE: FPGA With Conductors Segmented By Active Repeaters
INVENTOR(S): Paul Takao Sasaki; Madhukar B. Vora; Burnell G. West

PATENT NO.: **6,025,736**
ISSUE DATE: Feb. 15, 2000
TITLE: Fast Programmable Logic With Active Links Between Cells
INVENTOR(S): Madhukar B. Vora; Burnell G. West