FORM PTO-1595 (Rev. 6-93) OMB No. 0651-0011 (exp. 4/94)

RECO 9.6-00

09-21-2000

101465723

EET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Commissioner o ginal documents or copy thereof.

1. Name of conveying part(ies):

Acer Semiconductor Manufacturing Inc.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: TSMC-Acer Semiconductor Manufacturing Corporation

Street Address:
No. 6, Creation Rd. II
Science-Based Industrial Park
Hsinchu, Taiwan, R.O.C.

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other:

Execution Date: June 30 , 2000

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:

A. Patent application No.(s)

See Appendix A

B. Patent No.(s)

See Appendix A

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Daniel R. McClure
Thomas, Kayden, Horstemeyer & Risley, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339

6. Total number of applications/patents involved: [209]

113 Applications

96 Patents

7. Total fee (37 CFR 3.41) $ 8,360.00

☒ Enclosed
☐ Authorized to be charged to deposit account

8. Deposit Account Number:

20-0778
(Attach duplicate copy of this page if paying by Deposit Account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Daniel R. McClure

Type Name of Person Signing - Daniel R. McClure

Aug 30, 2000

Date

Docket #: 251002-9010

Total number of pages including cover sheet, attachments, and document: [6]

Mail documents to be recorded with required cover sheet information to:
Assistant Commissioner for Patents, Box Assignments
Washington, D.C. 20231

09/20/2000 TALLAH2 00000113 08599075
AssignCoverSht.doc
01 FC:581 8360.00 OP

Appendix A

Assignee--Acer Semiconductor Manufacturing Inc.

Filing No.	Filing Date	Pat. No.	Date of Pat.	Title
08/599,075	1996/2/9	US06061759	2000/5/9	Hidden precharge pseudo cache DRAM
08/681,718	1996/7/29	US05888579	1999/3/30	Method and apparatus for preventing particle contamination in a process chamber
08/953,609	1997/10/17	US05915182	1999/6/22	MOSFET with self-aligned silicidation and gate-side air-gap structure
08/954,412	1997/10/20	US05930622	1999/7/27	Method for forming a DRAM cell with a double-crown shaped capacitor
08/954,413	1997/10/20	US05866455	1999/2/2	Method for forming a dram cell with a multiple pillar-shaped capacitor
08/954,416	1997/10/20	US05834353	1998/11/10	Method of making deep sub-micron meter MOSFET with a high permitivity gate dielectric
08/954,448	1997/10/20			METHOD FOR FORMING A RUGGED STACKED TRENCH (RST)..
08/958,536	1997/10/27	US06027981	2000/2/22	Method for forming a DRAM cell with a fork-shaped capacitor
08/960,870	1997/10/31	US06011286	2000/1/4	Double stair-like capacitor structure for a DRAM cell
08/962,003	1997/10/31	US06020609	2000/2/1	DRAM cell with a rugged stacked trench (RST) capacitor
08/962,623	1997/11/3	US05766995	1998/6/16	Method for forming a DRAM cell with a ragged polysilicon crown-shaped capacitor
08/962,625	1997/11/3	US05807777	1998/9/15	Method of making a double stair-like capacitor for a high density DRAM cell
08/984,871	1997/12/4			SELF-ALIGNED SILICIDED MOSFETS WITH A GRADED S/D..
08/988,031	1997/12/10	US05909620	1999/6/1	Method for a ring-like capacitor in a semiconductor memory device
08/988,032	1997/12/10			DRAM cell with capacitor having multiple concave structure
08/988,034	1997/12/10	US06060394	2000/5/9	Method for forming shallow trench isolation with global planarization
08/988,035	1997/12/10	US05817558	1998/10/6	Method of forming a T-gate Lightly-Doped Drain semiconductor device
08/988,518	1997/12/10			CIRCUIT OF REDUCING TRANSMISSION DELAY FOR...
08/990,117	1997/12/12	US05913118	1999/6/15	Method of manufacturing trench DRAM cells with self-aligned field plate
08/990,167	1997/12/12			SELF-ALIGNED SLILCIDED MOS TRANSISTOR WITH A...
08/994,053	1997/12/19	US05856226	1999/1/5	Method of making ultra-short channel MOSFET with self-aligned silicided contact and extended S/D junction
08/994,178	1997/12/19	US06087234	2000/7/11	Method of forming a self-aligned silicide MOSFET with an extended ultra-shallow S/D junction
08/995,569	1997/12/22	US05966612	1999/10/12	Method of making a multiple mushroom shape capacitor for high density DRAMs
08/996,694	1997/12/23	US06022769	2000/2/8	Method of making self-aligned silicided MOS transistor with ESD protection improvement
08/998,796	1997/12/29	US05972761	1999/10/26	Method of making MOS transistors with a gate-side air-gap structure and an extension ultra-shallow S/D junction
08/998,933	1997/12/29	US05877053	1999/3/2	Method of fabricating DRAM cell with capacitor having multiple concave structure
08/999,268	1997/12/29	US05902125	1999/5/11	Method to form stacked-Si gate pMOSFETs with elevated and extended S/D junction
08/999,449	1997/12/29			DRAM CELL WITH A MULTIPLE MUSHROOM-SHAPE CAPACITOR
09/001,978	1997/12/31	US05994178	1999/11/30	Method of fabricating CMOS transistors with a planar shallow trench isolation
09/002,607	1998/1/5	US06008087	1999/12/28	Method to form high density NAND structure nonvolatile memories
09/002,608	1998/1/5	US05972762	1999/10/26	Method of forming mosfets with recessed self-aligned silicide gradual S/D junction
09/004,448	1998/1/8	US05877056	1999/3/2	Ultra-short channel recessed gate MOSFET with a buried contact
09/004,449	1998/1/8	US05895244	1999/4/20	Process to fabricate ultra-short channel nMOSFETs with self-aligned silicide contact
09/013,424	1998/1/23			METHOD OF FABRICATING CMOS TRANSISTORS WITH...
09/013,425	1998/1/26			METHOD TO FORM DIFFERENT THRESHOLD NMOSFETs FOR...
09/013,429	1998/1/26	US05946580	1999/8/31	Method to form elevated source/drain with solid phase diffused source/drain extension for MOSFET
09/013,676	1998/1/26	US05989950	1999/11/23	Reduced mask CMOS salicided process
09/013,682	1998/1/23	US05837588	1998/11/17	Method for forming a semiconductor device with an inverse-T gate lightly-doped drain structure
09/013,689	1998/1/26			METHOD OF FORMING A TRENCH CAPACITOR FOR A DRAM...
09/013,690	1998/1/26	US05905281	1999/5/18	DRAM cell with a fork-shaped capacitor
09/013,691	1998/1/26	US05811342	1998/9/22	Method for forming a semiconductor device with a graded lightly-doped drain structure
09/013,694	1998/1/23	US06069031	2000/5/30	Process to form CMOS devices with higher ESD and hot carrier immunity
09/014,862	1998/1/28	US06057205	2000/5/2	Method to form a ragged poly-Si structure for high density DRAM cells
09/014,864	1998/1/28	US06063706	2000/5/16	Method to simulataneously fabricate the self-aligned silicided devices and ESD protective devices
09/014,865	1998/1/28	US05963802	1999/10/5	CMOS process for forming planarized twin wells
09/014,866	1998/1/28	US06074932	2000/6/13	Method for forming a stress-free shallow trench isolation
09/014,867	1998/1/28	US06034396	2000/3/7	Ultra-short channel recessed gate MOSFET with a buried contact
09/014,868	1998/1/28	US06020621	2000/2/1	Stress-free shallow trench isolation
09/020,229	1998/2/6			Method to fabricate deep sub-uM CMOSFETs
09/020,230	1998/2/6	US06091100	2000/7/18	High density NAND structure nonvolatile memories
09/023,218	1998/2/13			METHOD OF FABRICATING GATE-DRAIN OVERLAPPED...
09/023,260	1998/2/13	US06081032	2000/6/27	Dual damascene multi-level metallization and interconnection structure
09/023,261	1998/2/13	US05976967	1999/11/2	Dual damascene process for multi-level metallization and interconnection structure

Assignee--Acer Semiconductor Manufacturing Inc.

Filing No.	Filing Date	Pat. No.	Date of Pat.	Title
09/023,453	1998/2/13	US05899715	1999/5/4	Method to form a capacitor for high density DRAM cell
09/023,454	1998/2/13	US05994747	1999/11/30	MOSFETs with recessed self-aligned silicide gradual S/D junction
09/024,772	1998/2/17	US05920774	1999/7/6	Method to fabricate short-channel MOSFETS with an improvement in ESD resistance
09/025,969	1998/2/19	US06063680	2000/5/16	MOSFETS with a recessed self-aligned silicide contact and an extended source/drain junction
09/025,970	1998/2/19	US06005269	1999/12/21	DRAM cell with a double-crown shaped capacitor
09/025,971	1998/2/19	US05994176	1999/11/30	Method for forming self-aligned silicided MOS transistors with asymmetric ESD protecting transistors
09/032,008	1998/2/27	US06083793	2000/7/4	Method to manufacture nonvolatile memories with a trench-pillar cell structure for high capacitive coupling ratio
09/033,526	1998/3/2	US05977561	1999/11/2	Elevated source/drain MOSFET with solid phase diffused source/drain extension
09/033,527	1998/3/2	US06010934	2000/1/4	Method of making nanometer Si islands for single electron transistors
09/033,546	1998/3/2	US06008517	1999/12/28	High density and low power flash memories with a high capacitive-coupling ratio
09/033,560	1998/3/2			METHOD OF MAKING SINGLE-ELECTRON-TUNNELING CMOS...
09/033,948	1998/3/2	US06001695	1999/12/14	Method to form ultra-short channel MOSFET with a gate-side airgap structure
09/034,635	1998/3/4	US05985737	1999/11/16	Method for forming an isolation region in an integrated circuit
09/036,027	1998/3/6	US05970342	1999/10/19	Method of forming high capacitive-coupling ratio and high speed flash memories with a textured tunnel oxide
09/036,038	1998/3/6			METHOD OF FORMING HIGH DENSITY AND LOW POWER...
09/042,347	1998/3/13	US06043124	2000/3/28	Method for forming high density nonvolatile memories with high capacitive-coupling ratio
09/042,348	1998/3/13	US05956580	1999/9/21	Method to form ultra-short channel elevated S/D MOSFETS on an ultra-thin SOI substrate
09/042,349	1998/3/13	US05998277	1999/12/7	Method to form global planarized shallow trench isolation
09/042,351	1998/3/13	US05897348	1999/4/27	Low mask count self-aligned silicided CMOS transistors with a high electrostatic discharge resistance
09/042,352	1998/3/12			METHOD TO FABRICATE DUAL THRESHOLD CMOS CIRCUITS
09/044,442	1998/3/19			DEEP-SHALLOW TRENCH ISOLATION
09/046,331	1998/3/23	US05877048	1999/3/2	3-D CMOS transistors with high ESD reliability
09/046,332	1998/3/23	US05963799	1999/10/5	Blanket well counter doping process for high speed/low power MOSFETs
09/046,343	1998/3/23			HIGH DENSITY/SPEED NONVOLATILE MEMORIES WITH A...
09/046,343	1998/3/23			METHOD FOR MANUFACTURING MASK ROM DEVICES WITH MINIMAL BAND-TO-BANK TUNNELING
09/048,154	1998/3/25	US05930617	1999/7/27	Method of forming deep sub-micron CMOS transistors with self-aligned silicided contact and extended S/D junction
09/048,549	1998/3/25	US06008079	1999/12/28	Method for forming a high density shallow trench contactless nonvolatile memory
09/050,540	1998/3/30	US06084265	2000/7/4	High density shallow trench contactless nonvolitile memory
09/050,541	1998/3/30	US05956584	1999/9/21	Method of making self-aligned silicide CMOS transistors
09/050,668	1998/3/30	US05982001	1999/11/9	MOSFETS structure with a recessed self-aligned silicide contact and an extended source/drain junction
09/050,669	1998/3/30	US05986305	1999/11/16	Semiconductor device with an inverse-T gate lightly-doped drain structure
09/050,670	1998/3/30			ULTRA-SHORT CHANNEL MOSFETs WITH SELF-ALIGNED...
09/052,280	1998/3/31	US05929493	1999/7/27	CMOS transistors with self-aligned planarization twin-well by using fewer mask counts
09/054,128	1998/4/2	US05985729	1999/11/16	Method for manufacturing a capacitor of a trench DRAM cell
09/056,222	1998/4/7	US06020240	2000/2/1	Method to simultaneously fabricate the self-aligned silicided devices and ESD protection devices
09/057,866	1998/4/9	US05998247	1999/12/7	Process to fabricate the non-silicide region for electrostatic discharge protection circuit
09/057,867	1998/4/9			LOW MASK COUNT PROCESS TO FABRICATE MASK READ...
09/057,869	1998/4/9			SINGLE ELECTRON TRANSISTOR MEMORY ARRAY
09/060,565	1998/4/14	US05973350	1999/10/26	Stacked capacitor structure for high density DRAM cells
09/060,566	1998/4/14	US06037225	2000/3/14	Manufacturing method for mask ROM devices
09/060,567	1998/4/14			METHOD FOR MANUFACTURING MASK ROM DEVICES WITH...
09/062,827	1998/4/20			3-D CMOS TRANSISTORS WITH HIGH ESD RELIABILITY
09/062,829	1998/4/20			SELF-ALIGNED SILICIDED MOS DEVICES WITH ESD...
09/063,210	1998/4/20	US05989977	1999/11/23	Shallow trench isolation process
09/063,211	1998/4/20	US05885873	1999/3/23	Double coding processes for mask read only memory (ROM) devices
09/064,260	1998/4/22			BURIED CONTACT STRUCTURE FOR SRAM DEVICES
09/064,261	1998/4/22	US06020230	2000/2/1	Process to fabricate planarized deep-shallow trench isolation having upper and lower portions with oxidized semiconductor trench fill in the upper portion and semiconductor trench fill in the lower portion

Assignee--Acer Semiconductor Manufacturing Inc.

Filing No.	Filing Date	Pat. No.	Date of Pat.	Title
09/064,262	1998/4/22	US05869374	1999/2/9	Method to form mosfet with an inverse T-shaped air-gap gate structure
09/064,430	1998/4/22	US06001674	1999/12/14	Method of eliminating buried contact trench in SRAM devices
09/064,976	1998/4/22			PLANARIZED DEEP-SHALLOW TRENCH ISOLATION FOR...
09/065,323	1998/4/23			TRENCH-FREE BURIED CONTACT TRENCH IN MOSFET...
09/065,472	1998/4/23	US06060749	2000/5/9	Ultra-short channel elevated S/D MOSFETS formed on an ultra-thin SOI substrate
09/072,289	1998/5/4			METHOD TO FORM SOI/CMOS TRANSISTORS
09/072,290	1998/5/4			METHOD TO FORM SHALLOW TRENCH ISOLATION WITH AN...
09/072,291	1998/5/4	US06084275	2000/7/4	Double coding mask read only memory (mask ROM) for minimizing band-to-band leakage
09/075,758	1998/5/11	US05889727	1999/3/30	Circuit for reducing the transmission delay of the redundancy evaluation for synchronous DRAM
09/076,024	1998/5/11			TRENCH FREE PROCESS FOR SRAM WITH BURIED CONTACT..
09/083,609	1998/5/22	US06057195	2000/5/2	Method of fabricating high density flat cell mask ROM
09/088,457	1998/6/1			STRUCTURE OF A MASK ROM DEVICE ON A...
09/088,458	1998/6/1			METHOD OF MANUFACTURING A MULTIPLE FIN-SHAPED...
09/089,873	1998/6/4	US06064085	2000/5/16	DRAM cell with a multiple fin-shaped structure capacitor
09/089,897	1998/6/3	US06048765	2000/4/11	Method of forming high density buried bit line flash EEPROM memory cell with a shallow trench floating gate
09/089,899	1998/6/3			METHOD OF ELIMINATING PHOTORESIST OUTGASSING IN...
09/099,699	1998/6/19	US06091119	2000/7/18	Double poly-gate high density multi-state flat mask ROM cells
09/099,705	1998/6/19			VOID-FREE TUNGSTEN-PLUG CONTACT FOR ULSI...
09/104,532	1998/6/25			METHOD OF MANUFACTURING MASK ROM DEVICES WITH...
09/104,533	1998/6/25	US06034403	2000/3/7	High density flat cell mask ROM
09/105,337	1998/6/26			METHOD FOR POLY-BUFFERED LOCOS WITHOUT PITTING...
09/105,338	1998/6/26			GAS VENT SYSTEM FOR A VACUUM CHAMBER
09/109,347	1998/6/30			MULTIPLE BARRIER METAL TECHNOLOGY FOR VOLCANO...
09/109,348	1998/6/30			HIGH-DENSITY BURIED BIT LINE FLASH EEPROM MEMORY..
09/113,931	1998/7/10			METHOD OF FABRICATING DOUBLE POLY-GATE HIGH...
09/122,813	1998/7/27			TRENCH DRAM CELLS WITH SELF-ALIGNED FIELD PLATE
09/122,825	1998/7/27			VOID-FREE AND VOLCANO-FREE TUNGSTEN-PLUG FOR...
09/123,746	1998/7/27			STRESS-FREE SHALLOW TRNCH ISOLATION
09/123,747	1998/7/27			MASK ROM DEVICES WITH SELF-ALIGNED CODING IMPLANT
09/123,748	1998/7/27	US06063683	2000/5/16	Method of fabricating a self-aligned crown-shaped capacitor for high density DRAM cells
09/124,409	1998/7/29	US05880508	1999/3/9	MOSFET with a high permitivity gate dielectric
09/131,492	1998/8/10			HIGH-DENSITY AND HIGH-SPEED NAND-TYPE MASK ROMS
09/134,885	1998/8/15	US05907782	1999/5/25	Method of forming a multiple fin-pillar capacitor for a high density dram cell
09/138,298	1998/8/21			METHOD OF MANUFACTURING MULTIPLE FIN-SHAPED...
09/189,612	1998/11/9			SIMULATOR FOR THE POST-EXPOSURE BAKE OF...
09/232,552	1999/1/18			DRAM CELL WITH A FORK-SHAPED CAPACITOR
09/238,381	1999/1/27			DOUBLE CODING MASK READ ONLY MEMORY(MASK ROM)FOR..
09/243,916	1999/2/3	US06090653	2000/7/18	Method of manufacturing CMOS transistors
09/248,955	1999/2/12			METHOD OF FORMING ULTRA-SHORT CHANNEL AND...
09/249,840	1999/2/15			A FLOWER-LIKE CAPACITOR STRUCTURE FOR A MEMORY...
09/261,027	1999/3/2	US06008090	1999/12/28	Method of forming high density flash memories with high capacitive-coupling ratio and high speed operation
09/265,062	1999/3/9			HIGH DENSITY FLASH MEMORIES WITH HIGH CAPACITIVE..
09/266,352	1999/3/11			METHOD OF FORMING A CROWN-FIN SHAPED CAPACITOR...
09/266,552	1999/3/11			METHOD OF FORMING HIGH DENSITY FLASH MEMORIES WITH MIM STRUCTURE
09/266,553	1999/3/11			HIGH DENSITY FLASH MEMORIES WITH MOM STRUCTURE
09/270,908	1999/3/15			METHOD OF FORMING HIGH CAPACITIVE-COUPLING RATIO..
09/271,736	1999/3/18			METHOD OF FABRICATING HIGH DENSITY BURIED BIT...
09/273,418	1999/3/19			CROWN-FIN SHAPED CAPACITORS FOR HIGH DENSITY...
09/275,133	1999/3/23			METHOD FOR FABRICATING MOSFETS WITH A RECESSED...
09/275,134	1999/3/23			METHOD FOR FABRICATING MOSFETS WITH A RECESSED...
09/275,135	1999/3/23			METHOD FOR FABRICATING MOSFETS WITH A RECESSED...
09/275,136	1999/3/23			METHOD FOR FABRICATING ULTRA SHORT CHANNEL...
09/283,405	1999/4/1			METHOD FOR FORMING HIGH DENSITY NONVOLATILE...
09/283,406	1999/4/1			A METHOD FOR FORMING HIGH DENSITY NONVOLATILE...
09/288,948	1999/4/9			METHOD TO FABRICATE SHORT-CHANNEL MOSFETs WITH...
09/291,264	1999/4/14	US06046090	2000/4/4	Process to fabricate ultra-short channel MOSFETS with self-aligned silicide contact
09/291,265	1999/4/14			METHOD OF MANUFACTURING DEEP SUB-MICRON CMOS...

Assignee--Acer Semiconductor Manufacturing Inc.

Filing No.	Filing Date	Pat. No.	Date of Pat.	Title
09/291,266	1999/4/14			DEEP SUB-MICRON CMOS TRANSISTORS
09/291,269	1999/4/14			PROCESS TO FABRICATE ULTRA-SHORT CHANNEL MOSFETS..
09/291,270	1999/4/14	US06069044	2000/5/30	Process to fabricate ultra-short channel nMOSFETS with self-aligned silicide contact
09/291,271	1999/4/14			PROCESS TO FABRICATE ULTRA-SHORT CHANNEL MOSFETS..
09/292,475	1999/4/15			A DRAM CAPACITOR WITH POROUS STORAGE NODE AND...
09/292,476	1999/4/15			A DRAM CAPACITOR WITH POROUS STORAGE NODE AND...
09/292,477	1999/4/15			METHOD FOR FORMING A DRAM CAPACITOR WITH POROUS...
09/292,478	1999/4/15			CMOS PROCESS FOR FORMING PLANARIZED TWIN WELLS
09/293,454	1999/4/16			METHOD FOR FORMING A DRAM CAPACITOR WITH POROUS...
09/298,928	1999/4/23			RUGGED POLYSILICON CUP-SHAPED CAPACITOR
09/298,929	1999/4/23	US06090663	2000/7/18	Method for forming a high-density DRAM cell with a rugged polysilicon cup-shaped capacitor
09/298/927	1999/4/23			METHOD FOR FORMING A DRAM CELL WITH A RAGGED..
09/300,638	1999/4/27	US06008514	1999/12/28	Double-crown shape capacitor with high-dielectric constant material
09/303,143	1999/4/30			METHOD TO FORM MOSFET WITH AN ELEVATED SOURCE...
09/307,629	1999/5/7			METHOD OF FABRICATING CMOS TRANSISTORS WITH...
09/307,630	1999/5/7			METHOD TO FORM MOSFET WITH AN ELEVATED SOURCE...
09/307,634	1999/5/7			METHOD OF FABRICATING A SELF-ALIGNED CROWN...
09/307,635	1999/5/7			SELF-ALIGNED CROWN-SHAPED RUGGED CAPACITOR FOR...
09/310,487	1999/5/12			METHOD FOR FORMING A RAGGED POLYSILICON CROWN-...
09/310,888	1999/5/12			METHOD FOR FORMING A RAGGED POLYSILICON CROWN-...
09/310,889	1999/5/12			METHOD FOR FORMING A HIGH-DENSITY DRAM CELL WITH..
09/310,890	1999/5/12	US06091098	2000/7/18	Double-crown rugged polysilicon capacitor
09/313,084	1999/5/17			METHOD FOR FORMING HIGH DENSITY NONVOLATILE...
09/313,085	1999/5/17			METHOD OF FORMING SELF-ALGINED PLANARIZATION...
09/323,772	1999/6/1			METHOD OF ELIMINATING BURIED CONTACT TRENCH IN...
09/323,773	1999/6/1			ELIMINATING BURIED CONTACT TRENCH IN MOSFET...
09/325,810	1999/6/4			METHOD OF FORMING HIGH DENSITY BURIED BIT LINE...
09/325,811	1999/6/4			METHOD OF FORMING MOSFET WITH BURIED CONTACT AND..
09/326,857	1999/6/7			METHOD FOR FORMING HIGH DENSITY NONVOLATILE...
09/326,858	1999/6/7			SHALLOW TRENCH ISOLATION PROCESS
09/336,868	1999/6/18			SHALLOW TRENCH ISOLATION PROCESS
09/336,869	1999/6/18			METHOD OF FORMING HIGH DENSITY AND LOW POWER...
09/336,870	1999/6/18			METHOD OF FORMING HIGH DENSITY AND LOW POWER...
09/343,674	1999/6/30			DRAM CELL WITH A MULTIPLE PILLAR-SHAPED CAPACITOR
09/345,925	1999/7/1			Method to fabricate deep sub-uM CMOSFETs
09/346,041	1999/7/6			MOSFET WITH BURIED CONTACT AND AIR-GAP GATE...
09/346,042	1999/7/6			DRAM CELL WITH A FORK-SHAPED CAPACITOR
09/351,873	1999/7/13			METHOD FOR FABRICATING HIGH-DENSITY AND HIGH...
09/351,876	1999/7/13			Method to fabricate deep sub-uM CMOSFETs
09/351,877	1999/7/13			AN ULTRA-SHORT CHANNEL RECESSED GATE MOSFET WITH..
09/353,508	1999/7/14			METHOD FOR FABRICATING AN EXTENDED SELF-ALIGNED...
09/353,509	1999/7/14			EXTENDED SELF-ALIGNED CROWNE-SHAPED RUGGED...
09/361,447	1999/7/26			METHOD FOR FORMING TRENCH ISOLATION REGIONS
09/361,448	1999/7/26			TRENCH ISOLATION REGIONS FOR INTEGRATED TWIN WELLS
09/366,604	1999/8/3			SELF-ALIGNED SILICIDED MOS DEVICES WITH...
09/366,605	1999/8/3			SELF-ALIGNED SILICIDED MOS TRANSISTORS WITH ESD...
09/366,606	1999/8/3			METHOD FOR FORMING SELF-ALIGNED MOS TRANSISTOR...
09/394,296	1999/9/10			METHOD OF FABRICATING DEEP-SHALLOW TRENCH...
09/418,840	1999/10/15			A self aligned dual damascene method
09/439,431	1999/11/15			METHOD FOR FORMING MOSFET WITH AN ELEVATED...
09/439,432	1999/11/15			MOSFET WITH AN ELEVATED SOURCE/DRAIN
09/439,433	1999/11/15			METHOD FOR FORMING MOSFET WITH AN ELEVATED...

ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

Acer Semiconductor Manufacturing Inc., A Taiwanese corporation having a place of business at No. 6, Creation Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C., (hereafter ASSIGNOR) has been assigned or otherwise has an ownership interest in certain new and useful improvements as set forth in the patents and patent applications listed in attached Appendix A.

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, ASSIGNOR hereby:

1) Sell(s), assign(s) and transfer(s) to TSMC - Acer Semiconductor Manufacturing Corporation, a Taiwanese corporation having a place of business at No. 6, Creation Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C. (hereinafter referred to as "ASSIGNEE") the entire right, title and interest in any and all improvements and inventions disclosed in, application(s) based upon, and Patent(s) (including foreign patents) granted upon the information which is disclosed therein.

2) Authorize and request the Commissioner of Patents to issue any and all Letters Patents resulting from said application(s) or any division(s), continuation(s), substitute(s), re-examination(s) or reissue(s) thereof to the ASSIGNEE.

3) Agree to execute all papers and documents and, entirely at the ASSIGNEE's expense, perform any acts which are reasonably necessary in connection with the prosecution of said application(s), as well as any derivative and applications thereof, foreign applications based thereon, and/or the enforcement of patents resulting from such applications.

4) Agree that the terms, covenants and conditions of this assignment shall inure to the benefit of the ASSIGNEE, its successors, assigns and other legal representative(s), and shall be binding upon the inventor(s), as well as the inventor's heirs, legal representatives and assigns.

5) Warrant and represent that ASSIGNOR has not entered, and will not enter into any assignment, contract, or understanding that conflicts with this assignment.

Signed on the date(s) indicated beside my (our) signature(s).

Acer Semiconductor Manufacturing Inc.

By: Chong Ping Huang Date: June 30, 2000

Typed Name: Chong-Ping Huang
Assistant Vice-President of QRA
Acer Semiconductor Manufacturing Inc.

Witnesses:

Signature _____ Date: June 30, 2000

Wilson H.L. Lee
7F-1, No. 100, Roosevelt Rd., Sec. 2
Taipei, Taiwan, R.O.C.

Signature _____ Date: June 30, 2000

Felix Yeh
7F-1, No. 100, Roosevelt Rd., Sec. 2
Taipei, Taiwan, R.O.C.