FORM **PTO 1595**
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# RECORDATION COVER SHEET
# PATENTS ONLY

U.S. DEPARTMENT OF COMMERCE
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To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof

1. Name of conveying party(ies):

Micron Electronics, Inc.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: Micron Technology, Inc.

Internal Address:

Street Address: 8000 South Federal Way

City: Boise State: ID ZIP: 83707-0006

Additional name(s) & address(es) attached ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☐ Other

Execution Date: March 17, 2000

4. Application number(s) or patent number(s): 09/619,597, filed July 19,2000

If this document is being filed together with a new application, the execution date of the app

10-12-2000

101485896

A. Patent Application No.(s)

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Stuart R. Hemphill

Internal Address: Dorsey & Whitney LLP

Street Address: 220 South Sixth Street

City: Minneapolis State: MN ZIP 55402

6. Total Number of applications and and patents involved:. . . . . One (1)

7. Total fee (37 CFR 3.41). . . . . $

☒ Enclosed

☐ Authorized to be charged to deposit account

8. Deposit account number:

(Attach duplicate copy of this page if paying by deposit account)

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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Stuart R. Hemphill
Name of person Signing

Signature
Reg. No. 28,084

September 21, 2000
Date

Total number of pages including cover sheet, attachments, and document: 10

**Mail documents to be recorded with required cover sheet information to:**

**Commissioner of Patents & Trademarks, Box Assignments**
**Washington, D.C. 20231**

# ASSIGNMENT

Micron Electronics, Inc., a Minnesota corporation, having an office at 900 East Karcher Road, Nampa, Idaho 83687, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, hereby sells, assigns, and transfers its entire right, title and interest in and to the Patents, including without limitation, damages and payments for past or future infringements thereof, and the right to bring suit and recover against any third party for acts of infringement occurring before the date of this Assignment, and including all divisions, continuations, continuations-in-part, reissues, reexaminations, extensions or equivalents thereof in all pending applications therefor, all foreign counterparts thereof and all pending applications therefor, and any period of market exclusivity relating thereto, in and to the following patents and patent applications to Micron Technology, Inc., a Delaware corporation, having a place of business at 8000 South Federal Way, Boise, ID 83707-0006:

## PATENTS

| [illegible] | [illegible] |
|---|---|
| 6,037,803 | Integrated Circuit Having Two Modes of I/O Pad Termination |
| 6,031,787 | Apparatus For Providing Additional Latency For Synchronously Accessed Memory |
| 6,029,253 | Method For Synchronizing Data With A Bi-Directional Buffer |
| 6,029,223 | Advanced Programmable Interrupt Controller |
| 6,026,463 | Method For Improving Data Transfer Rates For User Data Stored On A Desk Storage Device |
| 6,026,046 | Apparatus For Decoding Addresses |
| 6,018,807 | Simulation "Bus Contention" Detection |
| 6,018,792 | Apparatus For Performing A Low Latency Memory Read With Concurrent Snoop |
| 6,006,310 | Single Memory Device That Functions As A Multi-Way Set Associative Cache Memory |
| 6,006,166 | Apparatus For Testing A Controller With Random Constraints |
| 6,000,001 | Multiple Priority Accelerated Graphics Port (AGP) Request Queue |
| 5,991,855 | Low Latency Bus Memory Read With Concurrent Pipelined Snoops |
| 5,991,843 | Method and System For Concurrent Computer Transaction Processing |
| 5,978,872 | Method and System For Concurrent Computer Transaction Processing |
| 5,974,239 | Data Transfer Method For A Bus Device In A Computer System By Placing First and Second Addresses Corresponding to a Bridge and With The Bus Device Respectively On A Bus |
| 5,968,139 | Method of Redirecting I/O Operations To Memory |
| 5,953,743 | Method For Accelerating Memory Bandwidth |

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|---|---|
| 5,950,229 | System For Accelerating Memory Bandwidth |
| 5,935,233 | Computer System With A Switch Interconnector For Computer Devices |
| 5,933,859 | Processor To Memory Interface Logic For Use In a Computer System Using A Multiplexed Memory Address |
| 5,933,852 | System and Method For Accelerated Remapping Defective Memory Locations |
| 5,931,937 | Symmetric Parallel Multi-Processing Bus Architecture |
| 5,926,838 | Interface For High Speed Memory |
| 5,920,881 | Method And System For Using A Virtual Register File In System Memory |
| 5,919,252 | Process and Apparatus For Adaptive Bus Termination |
| 5,911,078 | Method For Multi-Threaded Disk Drive Operation In A Computer System |
| 5,911,077 | System For Multithreaded Disk Drive Operation In A Computer System |
| 5,909,701 | Interface For High Speed Memory |
| 5,905,910 | System For Multi-Threaded Disk Drive Operation In A Computer System Using an Interrupt Processor Software Module Analyzing and Processing Interrupt Signals To Control Data Transfer |
| 5,905,878 | Method For Controlling Access To A Computer Bus |
| 5,905,858 | System For Method Memory Error Handling |
| 5,903,776 | Multiple Priority Accelerated Graphics Port (AGP) Request Queue |
| 5,898,891 | Method For Transferring Data Directly Between The First And Second Data Storage Devices Without Transferring Data To The Memory Array or Over The Input-Output Bus |
| 5,889,726 | Apparatus For Providing Additional Latency For Synchronously Accessed Memory |
| 5,887,157 | Local Bus Interface |
| 5,878,235 | Method and System For Concurrent Computer Transaction Processing |
| 5,867,733 | Mass Data Storage Controller Permitting Data to be Directly Transferred Between Storage Devices Without Transferring Data To Main Memory and Without Transferring Data Over Input-Output Bus |
| 5,862,314 | System and Method For Remapping Defective Memory Locations |
| 5,857,095 | Method For Aligning A Control Signal and A Clock Signal |
| 5,857,084 | Hierarchical Bus Structure Access System |
| 5,832,418 | Apparatus For Testing A Controller With Random Constraints |
| 5,829,036 | Method For Providing and Operating Upgradeable Cache Circuitry |
| 5,822,549 | Computer System and Bus Controller For Controlling Access To A Computer Bus |
| 5,819,076 | Memory Controller Apparatus With Low Skew Control Signal |
| 5,815,674 | Method And System For Interfacing A Plurality of Bus Requesters With A Computer Bus |
| 5,813,029 | Upgradeable Cache Circuit Using High Speed Multiplexer |
| 5,805,841 | Symmetric Parallel Multi-Processing Bus Architecture |

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|---|---|
| 5,805,835 | Parallel Architecture Computer System and Method |
| 5,771,358 | Method and System For Apportioning Computer Bus Bandwidth |
| 5,745,772 | Advanced Programmable Interrupt Controller |
| 5,740,380 | Method and System For Apportioning Computer Bus Bandwidth |
| 5,692,165 | Memory Controller With Low Skew Control Signal |
| 5,666,522 | Variable Speed Controller |
| 5,664,140 | Processor To Memory Interface Logic For Use In a Computer System Using A Multiplexed Memory Address |
| 5,649,162 | Local Bus Interface |
| 5,581,793 | System For Bypassing Setup States In A Bus Operation |
| TW/94625 | Pipelined Burst Multi-Way Associative Cache Memory Device |
| TW/090594 | Memory Controller With Low Skew Control Signal |

## PATENT APPLICATIONS

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| 09/432,687 |
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| PCT/US99/04017 |
| PCT/US98/27791 |
| PCT/US98/27784 |

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|---|---|---|---|---|
| Not Yet Assigned | 98.00198.00 | 1/24/00 | Computer System Having Reduced Number of Bus Bridge Terminals | James Meyer, Terry Cronin |
| Not Yet Assigned | 98.00198.01 | 1/18/00 | Method of Reducing The Number of Bus Bridge Terminals in a Computer System | James Meyer, Terry Cronin |

Executed on this 17th day of March 2000 at Nampa, Idaho.

Micron Electronics, Inc.

By _____
Steven P. Arnold
Vice President, General Counsel

& DATE

State of Idaho }
} ss.
County of Canyon }

This 17th day of March, 2000, before me personally came the above-named Steve Arnold, who executed the foregoing instrument in my presence, and who acknowledged to me that he executed the same of his own free will for the purposes set forth therein.

_____
Notary Public for Idaho

[Seal] ALICIA A. BROWN NOTARY PUBLIC STATE OF IDAHO

My commission expires 6/9/00