

02-22-2001

FORM PTO-1619A
Expires 06/30/99
OMB 0651-0027



101616778

U.S. Department of Commerce
Patent and Trademark Office
PATENT

11-17-00

**RECORDATION FORM COVER SHEET
PATENTS ONLY**

TO: The Commissioner of Patents and Trademarks: Please record the attached original document(s) or copy(ies).

Submission Type

New

Resubmission (Non-Recordation)
Document ID#

Correction of PTO Error
Reel # Frame #

Corrective Document
Reel # Frame #

Conveyance Type

Assignment Security Agreement

License Change of Name

Merger Other

U.S. Government
(For Use ONLY by U.S. Government Agencies)

Departmental File Secret File

Conveying Party(ies)

Mark if additional names of conveying parties attached

Execution Date
Month Day Year

Name (line 1)

Name (line 2)

Second Party

Name (line 1)

Name (line 2)

Execution Date
Month Day Year

Receiving Party

Mark if additional names of receiving parties attached

Name (line 1)

Name (line 2)

Address (line 1)

Address (line 2)

Address (line 3)
City State/Country Zip Code

If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative is attached. (Designation must be a separate document from Assignment.)

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name

Address (line 1)

Address (line 2)

Address (line 3)

Address (line 4)

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Public burden reporting for this collection of information is estimated to average approximately 30 minutes per Cover Sheet to be recorded, including time for reviewing the document and gathering the data needed to complete the Cover Sheet. Send comments regarding this burden estimate to the U.S. Patent and Trademark Office, Chief Information Officer, Washington, D.C. 20231 and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Paperwork Reduction Project (0651-0027), Washington, D.C. 20503. See OMB Information Collection Budget Package 0651-0027, Patent and Trademark Assignment Practice. DO NOT SEND REQUESTS TO RECORD ASSIGNMENT DOCUMENTS TO THIS ADDRESS.

Mail documents to be recorded with required cover sheet(s) information to:
Commissioner of Patents and Trademarks, Box Assignments, Washington, D.C. 20231

PATENT
REEL: 011491 FRAME: 0917

Correspondent Name and Address Area Code and Telephone Number

Name

Address (line 1)

Address (line 2)

Address (line 3)

Address (line 4)

Pages Enter the total number of pages of the attached conveyance document including any attachments. #

Application Number(s) or Patent Number(s) Mark if additional numbers attached

Enter either the Patent Application Number or the Patent Number (DO NOT ENTER BOTH numbers for the same property).

Patent Application Number(s)

Patent Number(s)

<input type="text" value="09/395,875"/>	<input type="text" value="08/844,543"/>	<input type="text" value="08/998,591"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
<input type="text" value="09/536,829"/>	<input type="text" value="09/024,940"/>	<input type="text" value="09/078,377"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
<input type="text" value="09/083,524"/>	<input type="text" value="09/103,760"/>	<input type="text" value="09/161,189"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>

If this document is being filed together with a new Patent Application, enter the date the patent application was signed by the first named executing inventor. Month Day Year

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned.

PCT PCT PCT

PCT PCT PCT

Number of Properties Enter the total number of properties involved. #

Fee Amount Fee Amount for Properties Listed (37 CFR 3.41): \$

Method of Payment: Enclosed Deposit Account

Deposit Account
(Enter for payment by deposit account or if additional fees can be charged to the account.)

Deposit Account Number: #

Authorization to charge additional fees: Yes No

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Antoinette E. Baker Antoinette E Baker 2/16/01
Name of Person Signing Signature Date

**RECORDATION FORM COVER SHEET
CONTINUATION
PATENTS ONLY**

FORM PTO-1619C
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U.S. Department of Commerce
Patent and Trademark Office
PATENT

Conveying Party(ies)

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Enter additional Conveying Parties

Execution Date
Month Day Year

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Patent Application Number(s)

Patent Number(s)

09/176,048	09/176,614	09/199,041
09/199,115	09/199,706	09/203,720
09/203,826	09/220,987	09/223,236
09/223,471	09/233,980	09/238,468
09/240,422	09/240,423	09/246,574

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Patent Application Number(s)

09/261,077	09/261,280	09/262,789
09/287,711	09/305,170	09/309,448
09/310,660	09/324,710	09/348,772
09/349,416	09/365,596	09/370,600
09/378,358	09/383,022	09/383,064

Patent Number(s)

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Patent Application Number(s)

09/385,694	09/385,695	09/385,696
09/387,377	09/391,792	09/393,016
09/412,889	09/420,065	09/421,454
09/421,918	09/422,027	09/422,115
09/434,546	09/434,589	09/436,158

Patent Number(s)

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Application Number(s) or Patent Number(s)

Mark if additional numbers attached

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Patent Application Number(s)

09/437,013	09/437,574	09/439,075
09/439,917	09/440,221	09/440,805
09/440,808	09/441,115	09/444,035
09/447,202	09/448,538	09/449,070
09/452,454	09/457,505	09/457,513

Patent Number(s)

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Application Number(s) or Patent Number(s)

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Mark if additional numbers attached

Patent Application Number(s)

Patent Number(s)

09/457,515	09/457,516	09/457,517
09/458,033	09/460,175	09/461,523
09/461,629	09/483,212	09/484,192
09/484,869	09/490,317	09/490,713
09/490,717	09/491,112	09/496,991

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City State/Country Zip Code

Application Number(s) or Patent Number(s)

Mark if additional numbers attached

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Patent Application Number(s)

09/497,377	09/498,144	09/504,007
09/505,395	09/513,067	09/513,232
09/513,285	09/519,962	09/536,236
09/536,574	09/536,830	09/539,311
09/539,314	09/548,702	09/548,705

Patent Number(s)

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PATENT

Conveying Party(ies)

Enter additional Conveying Parties

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Execution Date
Month Day Year

Name (line 1)

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City

State/Country

Zip Code

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City

State/Country

Zip Code

Application Number(s) or Patent Number(s)

Mark if additional numbers attached

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Patent Application Number(s)

09/551,416	09/558,392	09/561,180
09/565,586	09/565,881	09/566,069
09/566,658	09/566,680	09/566,849
09/568,086	09/569,716	09/569,718
09/574,006	09/576,595	09/577,692

Patent Number(s)

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Application Number(s) or Patent Number(s)

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Patent Application Number(s)

09/585,506	09/585,703	09/585,704
09/585,901	09/585,915	09/587,136
09/591,705	09/593,269	09/595,620
09/602,076	09/602,162	09/602,195
09/602,196	09/608,197	09/608,357

Patent Number(s)

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09/608,419	09/608,502	09/608,678
09/608,915	09/615,107	09/615,670
09/617,193		

Patent Number(s)

12-14-2000

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Patent and Trademark Office

PATENT

101550710

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Submission Type

New

Resubmission (Non-Recordation)
Document ID#

Correction of PTO Error
Reel # Frame #

Corrective Document
Reel # Frame #

Conveyance Type

Assignment Security Agreement

License Change of Name

Merger Other

U.S. Government
(For Use ONLY by U.S. Government Agencies)

Departmental File Secret File

Conveying Party(ies)

Mark if additional names of conveying parties attached

Execution Date
Month Day Year

Name (line 1) Amkor Technology, Inc.

April 28, 2000

Name (line 2)

Execution Date
Month Day Year

Second Party

Name (line 1)

Name (line 2)

Receiving Party

Mark if additional names of receiving parties attached

If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative is attached. (Designation must be a separate document from Assignment.)

Name (line 1) Guardian Assets, Inc.

Name (line 2)

Address (line 1) Goshen Corporate Park

Address (line 2) 1345 Enterprise Drive

Address (line 3) West Chester

PA / USA

State/Country

19380

Zip Code

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name Shearman & Sterling

Address (line 1) 599 Lexington Avenue

Address (line 2) New York, NY 10022

Address (line 3)

Address (line 4)

FOR OFFICE USE ONLY

12/12/2000 6TQM11 00000149 09395875

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Mail documents to be recorded with required cover sheet(s) information to:
Commissioner of Patents and Trademarks, Box Assignments, Washington, D.C. 20231

PATENT

REEL: 011491 FRAME: 0928

Correspondent Name and Address

Area Code and Telephone Number

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Pages Enter the total number of pages of the attached conveyance document including any attachments. #

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Patent Number(s)

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If this document is being filed together with a new Patent Application, enter the date the patent application was signed by the first named executing inventor.

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned.

PCT <input type="text"/>	PCT <input type="text"/>	PCT <input type="text"/>
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Number of Properties

Enter the total number of properties involved. #

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): \$

Method of Payment:

Enclosed Deposit Account

Deposit Account

(Enter for payment by deposit account or if additional fees can be charged to the account.)

Deposit Account Number: #

Authorization to charge additional fees: Yes No

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Antoinette E. Baker

Antoinette E. Baker

11/15/00

Name of Person Signing

Signature

Date

Serial Number	Date Filed	Docket #	Title
09/395,875	09/14/1999	M-5897-1D US	Methods for making integrated circuit device packages and micro-leadframes for the packages
08/844,543	04/18/1997	M-3146 PCT	Method of making integrated circuit package having adhesive bead supporting planar lid above planar
08/998,591	12/29/1997	AB-602 US	Circuit board with eye-shaped internal circuit tip alignment structure for mounting electronic components
09//536,829	03/27/2000	G-0006B US	A flip chip array package for image array sensors; using optically transparent epoxy
09/024,940	02/17/1998	AB-609 US	Method of fabricating semiconductor package
09/078,377	05/12/1998	M-2963-1D US	Integrated circuit chip to substrate interconnection and
09/083,524	05/22/1998	M-3398-1P US	RF shielded device
09/103,760	06/24/1998	M-5599 US	Plastic integrated circuit package and method and leadframe for making the package
09/161,189	09/25/1998	M-3431-2C US	Carrier strip and molded flex circuit ball grid array
09/176,048	10/20/1998	M-4869-1D US	A method of making integrated circuit package employing a transparent encapsulant
09/176,614	10/21/1998	M-5897 US	Plastic integrated circuit device package and micro-leadframe and method for making the package
09/199,041	11/24/1998	AB-751 US	Method of forming titanium silicide
09/199,115	11/24/1998	AB-749 US	LDD CMOS Transistor and a fabrication process thereof
09/199,706	11/24/1998	AB-750 US	Method for forming isolation trenches on a semiconductor
09/203,720	12/01/1998	AB-510-1D US	Grid array type lead frame having lead ends in different
09/203,826	12/01/1998	M-3404/1D US	Grid array assembly
09/220,987	12/23/1998	AB-761 US	method of forming titanium silicide by heating a silicon substrate having a titanium film and a method of measuring the temperature during the heating process
09/223,236	12/30/1998	AB-766 US	A MOS transistor that inhibits punch through and method for fabricating the same
09/223,471	12/30/1998	AB-764 US	Trench, structure for isolating semiconductor elements and method for forming the same
09/233,980	01/20/1999	M-6001 US	Microcircuit die-sawing protector and method
09/238,468	01/28/1999	AB-726 US	Semiconductor package with multilevel lead frame
09/240,422	01/29/1999	AB-748 US	A printed circuit board for ball grid array semiconductor
09/240,423	01/29/1999	AB-747 US	Method of molding a printed circuit board for a
09/246,574	02/08/1999	M-5771 US	Electrostatic discharge dissipation package and method
09/261,077	03/02/1999	AB-799 US	narrow deep trench isolation method for semiconductor
09/261,280	03/02/1999	AB-798 US	Test pattern for measuring variations of critical dimensions of wiring patterns formed in the fabrication of
09/262,789	03/04/1999	AB-800 US	Method for forming a metal wiring pattern on a
09/287,711	04/07/1999	AB-811 US	Thin stackable semiconductor packages
09/305,170	05/04/1999	AB-812 US	Printed circuit board with oval solder ball lands for BGA semiconductor packages
09/309,448	05/11/2000	AB-564-1D US	Ball grid array semiconductor package with solder balls fused on printed circuit board and method for fabricating
09/310,660	05/12/1999	M-7149 US	Low cost printed circuit board with integral heat sink for semiconductor package
09/324,710	06/03/1999	M-6016 US	Plastic package for an optical integrated circuit device and method of making

Serial Number	Date Filed	Docket #	Title
09/348,772	07/07/1999	M-3398-4D US	Near chip size integrated circuit package
09/349,416	07/06/1999	M-3398-3D US	Near chip size integrated circuit package
09/365,596	07/30/1999	M-7576 US	TSSOP exposed pad options
09/370,600	08/09/1999	M-7664 US	Electronic device package and leadframe and method for making the package
09/378,358	08/20/1999	M-3398-2P US	Chip-sized optical sensor package
09/383,022	08/25/1999	M-5311 US	Method of forming an integrated circuit device package
09/383,064	08/25/1999	M-5398 US	A partially cured expansion stabilizer layer on a package containing an electronic device and method of making and
09/385,694	08/30/1999	AB-858 US	Wafer-scale production of chip-scale semiconductor packages using wafer mapping techniques
09/385,695	08/30/1999	AB-860 US	Method of laminating circuit pattern tape on
09/385,696	08/30/1999	M-5499 US	Surface acoustical wave flip chip
09/387,377	08/30/1999	AB-859 US	Circuit pattern tape for wafer-scale production of chip size
09/391,792	09/08/1999	AB-866 US	Lead frame used for the fabrication using the same
09/393,016	09/10/1999	M-5599-1D US	Plastic integrated circuit package and method and leadframe for making the package
09/412,889	10/05/1999	M-7899 US	Method of making integrated circuit package using a batch step for curing a die attachment film and a system for
09/420,065	10/18/1999	M-7662 US	Thin package integrated circuit including recessed heatsink with exposed surface
09/421,454	10/19/1999	AB-893 US	Methods and a device for heat treating a semiconductor wafer having different kinds of impurities
09/421,918	10/20/1999	AB-885 US	Semiconductor device and method of manufacturing such
09/422,027	10/20/1999	AB-884 US	Chip-scale semiconductor package of the fan-out type and method of manufacturing such packages
09/422,115	10/20/1999	AB-886 US	Semiconductor device and method of manufacturing such
09/434,546	11/05/1999	M-7814-1D US	Exposed copper pad polyimide chip carrier
09/434,589	11/05/1999	M-7814 US	Integrated circuit device packages and substrates for making the packages
09/436,158	11/09/1999	M-7744 US	MLP Deep Coining Option
09/437,013	11/09/1999	M-3399 US	Chip-Size semiconductor packages
09/437,574	11/09/1999	M-3146-3D US	Method of making integrated circuit package having adhesive bead supporting planar lid above planar
09/439,075	11/12/1999	M-7807 US	A package for an integrated circuit device and passive devices including electromagnetic interference protection
09/439,917	11/12/1999	M-7745 US	Cavity MLP
09/440,221	11/15/1999	M-7834 US	Core located input/output design
09/440,805	11/15/1999	G-0004B US	Micro-machine package and method of fabricating
09/440,808	11/15/1999	G-0010 US	Micro-machine package fabrication method
09/441,115	11/17/1999	M-7663 US	Method of molding plastic semiconductor packages
09/444,035	11/19/1999	AB-908 US	Lead frame with lead separation preventing means, semiconductor package using the lead frame. And method to fabricate the semiconductor package
09/447,202	11/22/1999	G-0002B US	Thin image sensor package and method
09/448,538	11/22/1999	G-0009 US	Thin image sensor package and method
09/449,070	11/23/1999	M-7896 US	Method of attaching a sheet of an adhesive film to substrate in the course of making integrated circuit

Serial Number	Date Filed	Docket #	Title
09/452,454	12/01/1999	M-7813 US	Conductive strap attachment process that allows electrical connection between an integrated circuit die and a lead
09/457,505	12/08/1999	G-0005B US	Molded image sensor package
09/457,513	12/08/1999	G-0011B US	Molded image sensor package having lens holder
09/457,515	12/08/1999	G-0012 US	Method of assembling a snap lid image sensor package
09/457,516	12/08/1999	G-0007B US	A snap lid image sensor package and method
09/457,517	12/08/1999	G-0014 US	Method of fabricating image sensor packages in an array
09/458,033	12/08/1999	G-0013 US	Image sensor package having sealed cavity over active
09/460,175	12/10/1999	M-4915-1D US	A microelectronic device package having a heat sink structure for increasing the thermal conductivity
09/461,523	12/14/1999	AB-909 US	Semiconductor package and method for fabricating the
09/461,629	12/14/1999	AB-910 US	A wire for a semiconductor package
09/483,212	01/14/2000	M-7897 US	Package for multiple integrated circuits and method
09/484,192	01/18/2000	M-8117 US	Stackable package for integrated circuit
09/484,869	01/18/2000	M-8117-1D US	Method of making and mounting stackable package for
09/490,317	01/24/2000	M-7898 US	Package for stacked integrated circuits and method of
09/490,713	01/25/2000	AB-947 US	Method of forming gate oxynitride for a semiconductor
09/490,717	01/01/2500	G-0015B US	Protected image sensor package
09/491,112	01/25/2000	G-0020 US	Protected image sensor fabrication method
09/496,991	02/02/2000	M-8064 US	Method of making ultra-thin package for flip chip
09/497,377	02/03/2000	M-8118 US	Stackable package for integrated circuit with interposer
09/498,144	02/04/2000	M-8193 US	Making chip size semiconductor packages
09/504,007	02/14/2000	M-5311-1P US	Method of forming an integrated circuit package using a plastic tape as a base
09/505,395	02/16/2000	M-8195 US	Low cost thermal BGA
09/513,067	02/24/2000	AB-928 US	Leadframe and heat sink attached semiconductor package using the same
09/513,232	02/24/2000	AB-816 US	Leadframe and heat sink attached semiconductor package using the same
09/513,285	02/24/2000	M-8526 US	Method of forming silicide for semiconductor device
09/519,962	03/07/2000	M-8135 US	Exposed pad cavity BGA
09/536,236	03/27/2000	M-8520 US	Copper strap design for low resistance path in an integrated circuit package
09/536,574	03/28/2000	M-8296 US	Method of making a package containing stacked
09/536,830	03/27/2000	G-0006M	flip chip image sensor package fabrication method'
09/539,311	03/30/2000	G-0016B US	Snapable multi-package substrate and array
09/539,314	03/30/2000	G-0017 US	method for fabricating a snapable multi package array substrate, snapable multi-package array and snapable
09/548,702	04/13/2000	M-5397-1D US	Electromagnetic interference shield device and method
09/548,705	04/13/2000	AB-978 US	Matrix Type Printed Circuit Board for Semiconductor
09/551,416	04/18/2000	M-5397-2D US	Electromagnetic interference shield device and method
09/558,392	04/25/2000	G-0021 US	Precision aligned and marked structure
09/558,392	04/25/2000	G-0021M US	Precision marking and singulation method
09/561,180	04/27/2000	M-8196 US	Moisture resistant integrated circuit chip package and
09/565,586	05/04/2000	M-8194 US	MRT level 2 - non bussed, full body gold tape carrier
09/565,881	05/05/2000	G-0003 US	Long Wire IC Package
09/566,069	05/05/2000	AB-974 US	Semiconductor package and method for fabricating the
09/566,658	05/08/2000	M-8119 US	Stackable package for integrated circuit having a cavity

Serial Number	Date Filed	Docket #	Title
09/566,680	05/08/2000	M-8816 US	Stackable package with heat sink
09/566,849	05/05/2000	G-0003M	Long Wire IC Package fabrication method
09/568,086	05/08/2000	M-8166 US	Ball grid array package w/stacked semiconductor dies "flip chip stacked die in superBGA"
09/569,716	05/11/2000	M-8121 US	Apparatus for mounting an electronic device to a substrate without soldering
09/569,718	05/11/2000	M-8122 US	Flip chip mountable on substrate without underfill
09/574,006	05/19/2000	AB-976 US	Semiconductor package and method for manufacturing
09/576,595	05/22/2000	G-0019M US	Method of forming an image sensor package having sealed cavity over active area
09/577,692	05/22/2000	G-0019 US	Image sensor package having sealed cavity over active
09/585,506	06/01/2000	M-8712 US	Reinforcing solder connections of electronic devices
09/585,703	05/31/2000	G-0029M US	Reverse contrast marking method
09/585,704	05/31/2000	G-0029 US	Reverse contrast marking for plastic packages
09/585,901	06/02/2000	M-3398-5D US	RF shielded device
09/585,915	06/02/2000	M-8595 US	Semiconductor package with spacer strips
09/587,136	06/01/2000	M-8822 US	Packaging high power integrated circuit devices
09/591,705	06/09/2000	M-8714 US	Making solder ball mounting pads on substrates
09/593,269	06/13/2000	M-7664-1D	Electronic Device package and leadframe
09/595,620	06/16/2000	M-7807-1D	A package for an integrated circuit device and passive devices including electromagnetic interference protection
09/602,076	06/22/2000	M-8133 US	Overhead material transport system for IC assembly and test manufacturing
09/602,162	06/23/2000	M-9210 US	Material transport method
09/602,195	06/23/2000	M-8768 US	Hoist assembly
09/602,196	06/23/2000	M-8769 US	Gripper assembly
09/608,197	06/30/2000	M-8871 US	Low profile exposed die package for semiconductor chip
09/608,197	07/20/2000	M-8922 US	Thin semiconductor package with stacked die
09/608,357	06/29/2000	G-0023M US	Flip chip integrated circuit and passive chip component package fabrication method
09/608,419	06/30/2000	M-8120 US	Stackable package for integrated circuit having chips for fastening package and tool for opening clips
09/608,502	06/30/2000	G-0008M US	Flip-chip micromachine package fabrication method
09/608,678	06/29/2000	G-0023 US	Improved IC package with a flip chip integrated circuit and passive chip components on a laminate substrate that is
09/608,915	06/30/2000	M-3398-6D US	Making chip sized optical semiconductor packages
09/615,107	07/13/2000	M-5599-2D	Plastic integrated circuit package and method and leadframe for making the package
09/615,670	07/14/2000	M-6001-1D US	Microcircuit die-sawing protector and method
09/617,193	07/17/2000	M-8239 US	Semiconductor packaging method for multiple chip
09/8447 US	03/20/2000	M-8447 US	Ultra low cost method for increasing mold cap thickness

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This INTELLECTUAL PROPERTY SECURITY AGREEMENT (as amended, amended and restated, supplemented or otherwise modified from time to time, the "*IP Security Agreement*") dated April 28, 2000, is made by the Persons listed on the signature pages hereof (collectively, the "*Grantors*") in favor of Société Générale ("*SG*"), as collateral agent (the "*Collateral Agent*") for the Secured Parties (as defined in the Credit Agreement referred to below).

WHEREAS, Amkor Technology, Inc. (the "*Borrower*"), a Delaware corporation, has entered into a Credit Agreement dated as of April 28, 2000 (as amended, amended and restated, supplemented or otherwise modified from time to time, the "*Credit Agreement*"; terms defined therein, unless otherwise defined herein, being used herein as therein defined) among the Borrower, certain Lender Parties party thereto, Salomon Smith Barney Inc. ("*SSBI*") as Book Manager, SG, as Administrative Agent and as Collateral Agent, SSBI, SG Cowen Securities Corporation ("*SG Cowen*") and Deutsche Bank Securities Inc., as Arrangers, SSBI and SG as Syndication Agents, and (ii) the Security Agreement dated as of April 28, 2000 (as amended, amended and restated, supplemented or otherwise modified from time to time, the "*Security Agreement*"; terms defined therein, unless otherwise defined herein, being used herein as therein defined) made by the Grantors from time to time party thereto in favor of the Collateral Agent for the Secured Parties.

WHEREAS, as a condition precedent to the making of Advances and the issuance of Letters of Credit by the Lender Parties under the Credit Agreement from time to time, each Grantor has executed and delivered that certain Security Agreement dated April 28, 2000 made by the Grantors to the Collateral Agent (as amended, amended and restated, supplemented or otherwise modified from time to time, the "*Security Agreement*").

WHEREAS, under the terms of the Security Agreement, Grantors have granted a security interest in, among other property, certain intellectual property of the Grantors to the Collateral Agent for the ratable benefit of the Secured Parties, and have agreed as a condition thereof to execute this IP Security Agreement covering such intellectual property for recording with the U.S. Patent and Trademark Office, the United States Copyright Office and other governmental authorities.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, each Grantor agrees as follows:

SECTION 1. Grant of Security. Each Grantor hereby grants to the Collateral Agent for the ratable benefit of the Secured Parties a security interest in and to all of such Grantor's right, title and interest in and to the following (the "*Collateral*"):

- (i) the United States, international, and foreign patents, patent applications and patent licenses set forth in Schedule A hereto (as such Schedule A may be supplemented from time to time by supplements to the Security Agreement and this IP Security Agreement, each such supplement being in substantially the form of Exhibit G to the Security Agreement (an "*IP Security Agreement Supplement*"), executed and delivered by such Grantor to the Collateral Agent from time to time), together with all reissues, divisions, continuations, continuations-in-part, extensions and reexaminations thereof, and all rights therein provided by international treaties or conventions (the "*Patents*");

(ii) the United States and foreign trademark and service mark registrations, applications, and licenses set forth in Schedule B hereto (as such Schedule B may be supplemented from time to time by IP Security Agreement Supplements executed and delivered by such Grantor to the Collateral Agent from time to time) (the "Trademarks");

(iii) the copyrights, United States and foreign copyright registrations and applications and copyright licenses set forth in Schedule C hereto (as such Schedule C may be supplemented from time to time by IP Security Agreement Supplements executed and delivered by such Grantor to the Collateral Agent from time to time) (the "Copyrights");

(iv) any and all claims for damages for past, present and future infringement, misappropriation or breach with respect to the Patents, Trademarks and Copyrights, with the right, but not the obligation, to sue for and collect, or otherwise recover, such damages; and

(v) any and all proceeds of the foregoing.

Notwithstanding the foregoing, the term "Collateral" does not include any license or contract right to the extent that (i) the granting of a security interest therein would be contrary to applicable law or (ii) such license or contract right is not assignable according to its terms (but only to the extent any such prohibition is enforceable under applicable law, including, without limitation, Section 9-318(4) of the N.Y. Uniform Commercial Code).

Section 2. Security for Obligations. The grant of a security interest in, the Collateral by each Grantor under this IP Security Agreement secures the payment of all Obligations of such Grantor now or hereafter existing under or in respect of the Loan Documents, whether direct or indirect, absolute or contingent, and whether for principal, reimbursement obligations, interest, premiums, penalties, fees, indemnifications, contract causes of action, costs, expenses or otherwise.

SECTION 3. Recordation. Each Grantor authorizes and requests that the Register of Copyrights, the Commissioner of Patents and Trademarks and any other applicable government officer record this IP Security Agreement.

SECTION 4. Execution in Counterparts. This Agreement may be executed in any number of counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement.

SECTION 5. Grants, Rights and Remedies. This IP Security Agreement has been entered into in conjunction with the provisions of the Security Agreement. Each Grantor does hereby acknowledge and confirm that the grant of the security interest hereunder to, and the rights and remedies of, the Collateral Agent with respect to the Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein.

SECTION 6. Governing Law. This IP Security Agreement shall be governed by, and construed in accordance with, the laws of the State of New York.

IN WITNESS WHEREOF, each Grantor has caused this Agreement to be duly executed and delivered by its officer thereunto duly authorized as of the date first above written.

AMKOR TECHNOLOGY, INC.

By Kenneth T. Joyce
Name: Kenneth T. Joyce
Title: Chief Financial Officer

Address for Notices:

Goshen Corporate Park
1345 Enterprise Drive
West Chester, PA 19380

GUARDIAN ASSETS, INC.

By Kenneth T. Joyce
Name: Kenneth T. Joyce
Title: Chief Financial Officer

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