FORM PTO-1619A Expires 06/30/99 OMB 0651-0027

02-22-2001



101616778

U.S. Department of Commerce Patent and Trademark Office **PATENT**

11-17-0 U RECORL	PATENTS ONLY			
TO: The Commissioner of Patents and Trademar	ks: Please record the attached original document	(s) or copy(ies).		
Submission Type	Conveyance Type			
New	Assignment X Security Agree	ment		
X Resubmission (Non-Recordation) Document ID# 101550710	License Change of Nan	ne		
Correction of PTO Error Reel # Frame #	Merger Other U.S. Government			
Corrective Document Reel # Frame #	(For Use ONLY by U.S. Government Departmental File	nt Agencies) Secret File		
Conveying Party(ies)	Mark if additional names of conveying parties att	ached Execution Date Month Day Year		
Name (line 1) Amkor Technology, Inc.		April 28, 2000		
Name (line 2) Second Party		Execution Date		
Name (line 1) Guardian Assets, Inc.		✓ Apriff 28, 200		
Name (line 2)				
Receiving Party	Mark if additional names of receiv	ring partles attached		
Name (line 1) Societe Generale	1) Societe Generale and specific an assignment and the 1 receiving perity is not demiciled in the United States and			
Name (line 2)		appointment of a domestic representative is attached. (Designation must be a		
	S.G. Cowen Security Corporation separate document from Assignment.)			
Address (line 2) 1 Financial Square, 30 th Floor				
Address (line 3) New York	NY / USA 100 State/Country Zip 0	Code		
Domestic Representative Name and Ad	dress Enter for the first Receiving Party of	only.		
Name Shearman & Sterling				
Address (line 1) 599 Lexington Avenue				
Address (line 2) New York, NY 10022				
Address (line 3)				
Address (line 4)				
	FOR OFFICE USE ONLY	5600E		

Public burden reporting for this collection of information is estimated to average approximately 30 minutes per Cover Sheet to be recorded, including time for reviewing the document and gathering the data needed to complete the Cover Sheet. Send comments regarding this burden estimate to the U.S. Patent and Trademark Office, Chief Information Officer, Washington, D.C. 20231 and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Paperwork Reduction Project (0651-0027), Washington, D.C. 20503. See OMB Information Collection Budget Package 0651-0027, Patent and Trademark Assignment Practice. DO NOT SEND REQUESTS TO RECORD ASSIGNMENT DOCUMENTS TO THIS ADDRESS.

Mail documents to be recorded with required cover sheet(s) information to:

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Со	rresponde	nt Name and Address Area Code and Telephone Number	212 848-4000			
	Name	Antoinette E. Baker				
A	ddress (line 1)	Shearman & Sterling				
A	ddress (line 2)	599 Lexington Avenue				
A	ddress (line 3)	New York, NY 10022				
A	ddress (line 4)					
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	onl	er PCT application number y if a U.S. Application Number not been assigned.	PCT			
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Fee	Amount	Fee Amount for Properties Listed (37 CFR 3.	41): \$			
	Method	of Payment: Enclosed Deposit Account				
		t Account payment by deposit account or if additional fees can be charged to the account.) Deposit Account Number:	# 500324			
		Authorization to charge additional fees:	Yes No X			
Statement and Signature						
	To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as					
	attached	d copy is a true copy of the original				
	indicate	d herein.	<u> 2/16/01</u>			
		Signature	Date			
	Name	e of Person Signing				

FORM PTO- Expires 06/30/99 OMB 0651-0027	RECORDATION FORM COVER SHEET CONTINUATION PATENTS ONLY	U.S. Department of Commerce Patent and Trademark Office PATENT
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FORM PTO- Expires 06/30/99 OMB 0651-0027	RECORDATION FORM COVER SHEET CONTINUATION PATENTS ONLY	U.S. Department of Commerce Patent and Trademark Office PATENT
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FORM PTO-1 Expires 06/30/99 OMB 0651-0027		CORDATION FOI CONTINU PATENTS		Т	U.S. Department of Commerce Patent and Trademark Office PATENT
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	09/568,086	09/569,710	69,718			
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FORM PTO Expires 06/30/5 OMB 0651-002	O-1619C	DATION FORM COVER SHEET CONTINUATION PATENTS ONLY	U.S. Department of Commerce Patent and Trademark Office PATENT
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Signature Date

indicated herein. Antoinette E. Baker

Name of Person Signing

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Methods for making integrated circuit device packages and micro-leadframes for the packages with package (and the packages)	Serial Number	Date Filed	Docket #	Title
Method of making integrated circuit package having adhesive bead supporting planar lid above planar Circuit board with eye-shaped internal circuit tip alignment structure for mounting electronic components A flip chip array package for image array sensors; using optically transparent epoxy optical device package and method of fabricating transparent epoxy optically transparent epoxy optica				Methods for making integrated circuit device packages
08/844,543 04/18/1997 M-3146 PCT adhesive bead supporting planar lid above planar 08/998,591 12/29/1997 AB-602 US activate for mounting electronic components 09/9536,829 03/27/2000 G-0006B US Aftip chip array package for image array sensors; using optically transparent epoxy. 09/078,377 05/12/1998 AB-809 US Method of fabricating semiconductor package 09/083,524 05/22/1998 M-3983-TP US RF shielded device 09/103,760 06/24/1998 M-3599 US Plastic integrated circuit package and method and leadframe for making the package 09/176,048 10/20/1998 M-3431-2C US Carrier strip and molded flex circuit ball grid array 09/176,614 10/21/1998 M-3431-2C US Carrier strip and molded flex circuit package and microleadframe and method of making integrated circuit package and microleadframe and method for making the package 09/176,614 10/21/1998 M-8751 US Method of forming ittanium silicide 09/189,706 11/24/1998 AB-751 US Method of forming ittanium silicide 09/193,041 11/24/1998 AB-750 US Method for forming titanium silicide by heating a silicon substrate having a transparent package and method for forming th	09/395,875	09/14/1999	M-5897-1D US	and micro-leadframes for the packages
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Serial Number	Date Filed	Docket #	Title
09/348,772	07/07/1999		Near chip size integrated circuit package
09/349,416	07/06/1999	M-3398-3D US	Near chip size integrated circuit package
09/365,596	07/30/1999	M-7576 US	TSSOP exposed pad options
			Electronic device package and leadframe and method for
09/370,600	08/09/1999	M-7664 US	making the package
09/378,358	08/20/1999	M-3398-2P US	Chip-sized optical sensor package
09/383,022	08/25/1999	M-5311 US	Method of forming an integrated circuit device package
			A partially cured expansion stabilizer layer on a package
09/383,064	08/25/1999	M-5398 US	containing an electronic device and method of making and
			Wafer-scale production of chip-scale semiconductor
09/385,694	08/30/1999	AB-858 US	packages using wafer mapping techniques
09/385,695	08/30/1999	AB-860 US	Method of laminating circuit pattern tape on
09/385,696	08/30/1999	M-5499 US	Surface acoustical wave flip chip
09/387,377	08/30/1999	AB-859 US	Circuit pattern tape for wafer-scale production of chip size
09/391,792	09/08/1999	AB-866 US	Lead frame used for the fabrication using the same
			Plastic integrated circuit package and method and
09/393,016	09/10/1999	M-5599-1D US	leadframe for making the package
			Method of making integrated circuit package using a batch
09/412,889	10/05/1999	M-7899 US	step for curing a die attachment film and a system for
			Thin package integrated circuit including recessed
09/420,065	10/18/1999	M-7662 US	heatsink with exposed surface
			Methods and a device for heat treating a semiconductor
09/421,454	10/19/1999	AB-893 US	wafer having different kinds of impurities
09/421,918	10/20/1999	AB-885 US	Semiconductor device and method of manufacturing such
			Chip-scale semiconductor package of the fan-out type and
09/422,027	10/20/1999	AB-884 US	method of manufacturing such packages
09/422,115	10/20/1999	AB-886 US	Semiconductor device and method of manufacturing such
09/434,546	11/05/1999	M-7814-1D US	Exposed copper pad polyimide chip carrier
			Integrated circuit device packages and substrates for
09/434,589	11/05/1999	M-7814 US	making the packages
09/436,158	11/09/1999		MLP Deep Coining Option
09/437,013	11/09/1999	M-3399 US	Chip-Size semiconductor packages
			Method of making integrated circuit package having
09/437,574	11/09/1999	M-3146-3D US	adhesive bead supporting planar lid above planar A package for an integrated circuit device and passive
			devices including electromagnetic interference protection
09/439,075	11/12/1999	M-7807 US	
09/439,917	11/12/1999	M-7745 US	Cavity MLP Core located input/output design
09/440,221	11/15/1999	M-7834 US	Micro-machine package and method of fabricating
09/440,805	11/15/1999	G-0004B US	Micro-machine package fabrication method
09/440,808	11/15/1999	G-0010 US	Teached of molding plastic semiconductor packages
09/441,115	11/17/1999	M-7663 US	to the lood separation preventing means,
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09/444,035 09/447,202 09/448,538		G-0002B US	to fabricate the semiconductor package Thin image sensor package and method Thin image sensor package and method Thin image sensor package and method
09/447,202	11/22/1999	G-0002B US G-0009 US	to fabricate the semiconductor package This image sensor package and method

Serial Number	Date Filed	Docket #	Title
			Conductive strap attachment process that allows electrical
09/452,454	12/01/1999	M-7813 US	connection between an integrated circuit die and a lead
09/457,505	12/08/1999	G-0005B US	Molded image sensor package
09/457,513	12/08/1999	G-0011B US	Molded image sensor package having lens holder
09/457,515	12/08/1999	G-0012 US	Method of assembling a snap lid image sensor package
09/457,516	12/08/1999	G-0007B US	A snap lid image sensor package and method
09/457,517	12/08/1999	G-0014 US	Method of fabricating image sensor packages in an array
09/458,033	12/08/1999	G-0013 US	Image sensor package having sealed cavity over active
			A microelectronic device package having a heat sink
09/460,175	12/10/1999	M-4915-1D US	structure for increasing the thermal conductivity
09/461,523	12/14/1999	AB-909 US	Semiconductor package and method for fabricating the
09/461,629	12/14/1999	AB-910 US	A wire for a semiconductor package
09/483,212	01/14/2000	M-7897 US	Package for multiple integrated circuits and method
09/484,192	01/18/2000	M-8117 US	Stackable package for integrated circuit
09/484,869	01/18/2000	M-8117-1D US	Method of making and mounting stackable package for
09/490,317	01/24/2000	M-7898 US	Package for stacked integrated circuits and method of
09/490,713	01/25/2000		Method of forming gate oxynitride for a semiconductor
09/490,717	01/01/2500	G-0015B US	Protected image sensor package
09/491,112	01/25/2000	G-0020 US	Protected image sensor fabrication method
09/496,991	02/02/2000	M-8064 US	Method of making ultra-thin package for flip chip
09/497,377	02/03/2000	M-8118 US	Stackable package for integrated circuit with interposer
09/498,144	02/04/2000	M-8193 US	Making chip size semiconductor packages
			Method of forming an integrated circuit package using a
09/504,007	02/14/2000	M-5311-1P US	plastic tape as a base
09/505,395	02/16/2000	M-8195 US	Low cost thermal BGA
			Leadframe and heat sink attached semiconductor
09/513,067	02/24/2000	AB-928 US	package using the same
			Leadframe and heat sink attached semiconductor
09/513,232	02/24/2000	AB-816 US	package using the same
09/513,285	02/24/2000		Method of forming silicide for semiconductor device
09/519,962	03/07/2000	M-8135 US	Exposed pad cavity BGA
		-	Copper strap design for low resistance path in an
09/536,236	03/27/2000	M-8520 US	integrated circuit package
09/536,574	03/28/2000	M-8296 US	Method of making a package containing stacked
09/536,830	03/27/2000	G-0006M	flip chip image sensor package fabrication method'
09/539,311	03/30/2000	G-0016B US	Snapable multi-package substrate and array
			method for fabricating a snapable multi package array
09/539,314	03/30/2000	G-0017 US	substrate, snapable multi-package array and snapable
09/548,702	04/13/2000	M-5397-1D US	Electromagnetic interference shield device and method Matrix Type Printed Circuit Board for Semiconductor
09/548,705	04/13/2000	AB-978 US	The state of the s
09/551,416	04/18/2000	M-5397-2D US	Electromagnetic interference structure
09/558,392	04/25/2000	G-0021 US	Precision aligned and marked structure Precision marking and singulation method
09/558,392	04/25/2000	G-0021M US	Moisture resistant integrated circuit chip package and
09/561,180	04/27/2000	M-8196 US	MRT level 2 - non bussed, full body gold tape carrier
09/565,586	05/04/2000		Lana Mira IC Backage
09/565,881	05/05/2000		Long Wire IC Package Semiconductor package and method for fabricating the
09/566,069	05/05/2000		Stackable package for integrated circuit having a cavity
09/566,658	05/08/2000	M-8119 US	Stackable package for integration

Serial Number	Date Filed	Docket #	Title
09/566,680	05/08/2000	M-8816 US	Stackable package with heat sink
09/566,849	05/05/2000	G-0003M	Long Wire IC Package fabrication method
			Ball grid array package w/stacked semiconductor dies "flip
09/568,086	05/08/2000	M-8166 US	chip stacked die in superBGA"
			Apparatus for mounting an electronic device to a substrate
09/569,716	05/11/2000	M-8121 US	without soldering
09/569,718	05/11/2000	M-8122 US	Flip chip mountable on substrate without underfill
09/574,006	05/19/2000	AB-976 US	Semiconductor package and method for manufacturing
			Method of forming an image sensor package having
09/576,595	05/22/2000	G-0019M US	sealed cavity over active area
09/577,692	05/22/2000	G-0019 US	Image sensor package having sealed cavity over active
09/585,506	06/01/2000	M-8712 US	Reinforcing solder connections of electronic devices
09/585,703	05/31/2000	G-0029M US	Reverse contrast marking method
09/585,704	05/31/2000	G-0029 US	Reverse contrast marking for plastic packages
09/585,901	06/02/2000		RF shielded device
09/585,915	06/02/2000	M-8595 US	Semiconductor package with spacer strips
09/587,136	06/01/2000	M-8822 US	Packaging high power integrated circuit devices
09/591,705	06/09/2000	M-8714 US	Making solder ball mounting pads on substrates
09/593,269	06/13/2000	M-7664-1D	Electronic Device package and leadframe
			A package for an integrated circuit device and passive
09/595,620	06/16/2000	M-7807-1D	devices including electromagnetic interference protection
			Overhead material transport system for IC assembly and
09/602,076	06/22/2000		test manufacturing
09/602,162	06/23/2000		Material transport method
09/602,195	06/23/2000		Hoist assembly
09/602,196	06/23/2000	M-8769 US	Gripper assembly
09/608,197	06/30/2000	M-8871 US	Low profile exposed die package for semiconductor chip
09/608,197	07/20/2000	M-8922 US	Thin semiconductor package with stacked die
		-	Flip chip integrated circuit and passive chip component
09/608,357	06/29/2000	G-0023M US	package fabrication method
			Stackable package for integrated circuit having chips for
09/608,419	06/30/2000	M-8120 US	fastening package and tool for opening clips
09/608,502	06/30/2000	G-0008M US	Flip-chip micromachine package fabrication method Improved IC package with a flip chip integrated circuit and
			passive chip components on a laminate substrate that is
09/608,678	06/29/2000	G-0023 US	
09/608,915	06/30/2000	M-3398-6D US	Making chip sized optical semiconductor packages
			Plastic integrated circuit package and method and
09/615,107	07/13/2000	M-5599-2D	leadframe for making the package
09/615,670	07/14/2000	M-6001-1D US	Microcircuit die-sawing protector and method Semiconductor packaging method for multiple chip
09/617,193	07/17/2000	M-8239 US	Semiconductor packaging method for metapro Ultra low cost method for increasing mold cap thickness
09/8447 US	03/20/2000		Ultra low cost metriod for increasing means
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This INTELLECTUAL PROPERTY SECURITY AGREEMENT (as amended, amended and restated, supplemented or otherwise modified from time to time, the "IP Security Agreement") dated April 28, 2000, is made by the Persons listed on the signature pages hereof (collectively, the "Grantors") in favor of Société Générale ("SG"), as collateral agent (the "Collateral Agent") for the Secured Parties (as defined in the Credit Agreement referred to below).

WHEREAS, Amkor Technology, Inc. (the "Borrower"), a Delaware corporation, has entered into a Credit Agreement dated as of April 28, 2000 (as amended, amended and restated, supplemented or otherwise modified from time to time, the "Credit Agreement"; terms defined therein, unless otherwise defined herein, being used herein as therein defined) among the Borrower, certain Lender Parties party thereto, Salomon Smith Barney Inc. ("SSBI") as Book Manager, SG, as Administrative Agent and as Collateral Agent, SSBI, SG Cowen Securities Corporation ("SG Cowen") and Deutsche Bank Securities Inc., as Arrangers, SSBI and SG as Syndication Agents, and (ii) the Security Agreement dated as of April 28, 2000 (as amended, amended and restated, supplemented or otherwise modified from time to time, the "Security Agreement"; terms defined therein, unless otherwise defined herein, being used herein as therein defined) made by the Grantors from time to time party thereto in favor of the Collateral Agent for the Secured Parties.

WHEREAS, as a condition precedent to the making of Advances and the issuance of Letters of Credit by the Lender Parties under the Credit Agreement from time to time, each Grantor has executed and delivered that certain Security Agreement dated April 28, 2000 made by the Grantors to the Collateral Agent (as amended, amended and restated, supplemented or otherwise modified from time to time, the "Security Agreement").

WHEREAS, under the terms of the Security Agreement, Grantors have granted a security interest in, among other property, certain intellectual property of the Grantors to the Collateral Agent for the ratable benefit of the Secured Parties, and have agreed as a condition thereof to execute this IP Security Agreement covering such intellectual property for recording with the U.S. Patent and Trademark Office, the United States Copyright Office and other governmental authorities.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, each Grantor agrees as follows:

SECTION 1. <u>Grant of Security</u>. Each Grantor hereby grants to the Collateral Agent for the ratable benefit of the Secured Parties a security interest in and to all of such Grantor's right, title and interest in and to the following (the "Collateral"):

(i) the United States, international, and foreign patents, patent applications and patent licenses set forth in Schedule A hereto (as such Schedule A may be supplemented from time to time by supplements to the Security Agreement and this IP Security Agreement, each such supplement being in substantially the form of Exhibit G to the Security Agreement (an "IP Security Agreement Supplement"), executed and delivered by such Grantor to the Collateral Agent from time to time), together with all reissues, divisions, continuations, continuations-in-part, extensions and reexaminations thereof, and all rights therein provided by international treaties or conventions (the "Patents");

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- (ii) the United States and foreign trademark and service mark registrations, applications, and licenses set forth in Schedule B hereto (as such Schedule B may be supplemented from time to time by IP Security Agreement Supplements executed and delivered by such Grantor to the Collateral Agent from time to time) (the "Trademarks");
- (iii) the copyrights, United States and foreign copyright registrations and applications and copyright licenses set forth in Schedule C hereto (as such Schedule C may be supplemented from time to time by IP Security Agreement Supplements executed and delivered by such Grantor to the Collateral Agent from time to time) (the "Copyrights");
- (iv) any and all claims for damages for past, present and future infringement, misappropriation or breach with respect to the Patents, Trademarks and Copyrights, with the right, but not the obligation, to sue for and collect, or otherwise recover, such damages; and
 - (v) any and all proceeds of the foregoing.

Notwithstanding the foregoing, the term "Collateral" does not include any license or contract right to the extent that (i) the granting of a security interest therein would be contrary to applicable law or (ii) such license or contract right is not assignable according to its terms (but only to the extent any such prohibition is enforceable under applicable law, including, without limitation, Section 9-318(4) of the N.Y. Uniform Commercial Code).

Section 2. <u>Security for Obligations</u>. The grant of a security interest in, the Collateral by each Grantor under this IP Security Agreement secures the payment of all Obligations of such Grantor now or hereafter existing under or in respect of the Loan Documents, whether direct or indirect, absolute or contingent, and whether for principal, reimbursement obligations, interest, premiums, penalties, fees, indemnifications, contract causes of action, costs, expenses or otherwise.

SECTION 3. <u>Recordation</u>. Each Grantor authorizes and requests that the Register of Copyrights, the Commissioner of Patents and Trademarks and any other applicable government officer record this IP Security Agreement.

SECTION 4. Execution in Counterparts. This Agreement may be executed in any number of counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement.

SECTION 5. Grants, Rights and Remedies. This IP Security Agreement has been entered into in conjunction with the provisions of the Security Agreement. Each Grantor does hereby acknowledge and confirm that the grant of the security interest hereunder to, and the rights and remedies of, the Collateral Agent with respect to the Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein.

SECTION 6. Governing Law. This IP Security Agreement shall be governed by, and construed in accordance with, the laws of the State of New York.

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IN WITNESS WHEREOF, each Grantor has caused this Agreement to be duly executed and delivered by its officer thereunto duly authorized as of the date first above written.

AMKOR TECHNOLOGY, INC.

Name: Kenneth

Title: Chief Financial

Address for Notices:

Goshen Corporate Park 1345 Enterprise Drive West Chester, PA 19380

GUARDIAN ASSETS, INC.

Name: Kenneth T. Jou

Title: Chief Financial Officer

Address for Notices:

Goshen Corporate Park 1345 Enterprise Drive West Chester, PA 19380

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UNITED STATES DEPARTMENT OF COMMERCE Patent and Trademark Office

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FEBRUARY 08, 2001

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