04-23-2001

101682079

RECORDATION FORM COVER SHEET
PATENTS ONLY

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

AGERE SYSTEMS GUARDIAN CORP. (DE Corporation)

4-5-01

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Name: The Chase Manhattan Bank, as Administrative Agent

Internal Address: _____

Street Address: P.O. Box 2558

City: Houston State: TX ZIP: 77252

Additional name(s) & addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☒ Other Conditional Assignment Of And Security Interest In Patent Rights

Execution Date: April 2, 2001

4. Application number(s) or patents number(s):

If this document is being filed together with a new application, the execution date of the application is: _____

A. Patent Application No.(s) **See Attached Schedule A**

B. Patent No.(s) **See Attached Schedule A**

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Alison Winick, Esq.

Internal Address: Simpson Thacher & Bartlett

Street Address: 425 Lexington Avenue

City: New York State: New York ZIP: 10017

6. Total number of applications and patents involved: 190

7. Total fee (37 CFR 3.41): ..... $ 7,600.00

☒ Enclosed

☐ Authorized to be charged to deposit account

8. Deposit account number:

_____

(Attached duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Alison Winick, Esq.
Name of Person Signing

Signature

4-5-01
Date

Total number of pages comprising cover sheet: 17

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents and Trademarks, Box Assignments
Washington, D.C. 20231

7600.00 39

SCHEDULE A

Patent/ Serial Number	Title
4347656	Method Of Fabricating Polysilicon Electrodes
4361461	Hydrogen Etching Of Semiconductors And Oxides
4362597	Method Of Fabricating High-Conductivity Silicide-On-Polysilicon Structures For Mos Devices
4378628	Cobalt Silicide Metallization For Semiconductor Integrated Circuits
4380490	Method Of Preparing Semiconductor Surfaces
4397724	Apparatus And Method For Plasma-Assisted Etching Of Wafers
4399610	Assembling An Electronic Device
4400235	Etching Apparatus And Method
4419201	Apparatus And Method For Plasma-Assisted Etching Of Wafers
4438450	Solid State Device With Conductors Having Chain-Shaped Grain Structure
4473455	Wafer Holding Apparatus And Method
4477782	Compound Current Mirror
4493142	Iii-V Based Semiconductor Devices And A Process For Fabrication
4510176	Removal Of Coating From Periphery Of A Semiconductor Wafer
4510514	Ohmic Contacts For Semiconductor Devices
4514647	Chipset Synchronization Arrangement
4516123	Integrated Circuit Including Logic Array With Distributed Ground Connections
4532697	Silicon Gigabit Metal-Oxide-Semiconductor Device Processing
4535532	Integrated Circuit Contact Technique
4544878	Switched Current Mirror
4574093	Deposition Technique
4607364	Multimode Data Communication System
4641420	Metalization Process For Headless Contact Using Deposited Smoothing Material
4645948	Field Effect Transistor Current Source
4649522	Fast Column Access Memory
4661375	Method For Increasing The Height Of Solder Bumps
4670770	Integrated Circuit Chip-And-Substrate Assembly
4676841	Fabrication Of Dielectrically Isolated Devices Utilizing Buried Oxygen Implant And Subsequent Heat Treatment At Temperatures Above 1300.Degree. C.
4680084	Interferometric Methods And Apparatus For Device Fabrication
4684971	Ion Implanted Cmos Devices
4698769	Supervisory Audio Tone Detection In A Radio Channel
4736404	Security Arrangement For Cordless Telephone System
4737112	Anisotropically Conductive Composite Medium
4742020	Multilayering Process For Stress Accommodation In Deposited Polysilicon
4742308	Balanced Output Analog Differential Amplifier Circuit
4750025	Depletion Stop Transistor
4769689	Stress Relief In Epitaxial Wafers
4773750	Deep-Uv Lithography
4774635	Semiconductor Package With High Density I/O Lead Connection
4782253	High Speed Mos Circuits
4821089	Protection Of Igfet Integrated Circuits From Electrostatic Discharge
4827428	Transistor Sizing System For Integrated Circuits
4851714	Multiple Output Field Effect Transistor Logic

4853758 Laser-Blown Links
4883352 Deep-Uv Lithography
4912347 Cmos To Ecl Output Buffer
4941154 Trellis Coding Method And Arrangement For Fractional Bit Rates
4947228 Integrated Circuit Power Supply Contact
4947425 Echo Measurement Arrangement
4965775 Image Derived Directional Microphones
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4999317 Metallization Processing
5001742 Baseband Signal Processing Unit And Method Of Operating The Same

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5040035 Mos Devices Having Improved Threshold Match
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5049982 Article Comprising A Stacked Array Of Electronic Subassemblies
5056117 Decision Feedback Equalization With Trellis Coding
5057462 Compensation Of Lithographic And Etch Proximity Effects
5063422 Devices Having Shallow Junctions
5102827 Contact Metallization Of Semiconductor Integrated-Circuit Devices
5105164 High Efficiency Uhf Linear Power Amplifier
5105442 Coded Modulation With Unequal Error Protection
5106771 Gaas Mesfets With Enhanced Schottky Barrier
5106786 Thin Coatings For Use In Semiconductor Integrated Circuits And Processes As Antireflection Coatings Consisting Of Tungsten Silicide

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5216694 Trellis Coding For Fractional Bits
5220564 Transmission Control For A Wireless Local Area Network Station
5227335 Tungsten Metallization
5234153 Permanent Metallic Bonding Method
5243229 Digitally Controlled Element Sizing
5254854 Scanning Microscope Comprising Force-Sensing Means And Position-Sensitive Photodetector
5264107 Pseudo-Electroless, Followed By Electroless, Metallization Of Nickel On Metallic Wires, As For Semiconductor Chip-To-Chip Interconne

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5298436 Forming A Device Dielectric On A Deposited Semiconductor Having Sub-Layers

5303307 Adjustable Filter For Differential Microphones
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5311088 Transconductance Cell With Improved Linearity
5311598 Method And Apparatus For Surface Inspection
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5334885 Automatic Control Of Buffer Speed
5346118 Surface Mount Solder Assembly Of Leadless Integrated Circuit Packages To Substrates
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5418476 Low Voltage Output Buffer With Improved Speed
5418798 Multidimensional Trellis-Coded Communication System
5422887 Medium Access Protocol For Wireless Local Area Network
5430396 Backplane Bus For Differential Signals
5439847 Integrated Circuit Fabrication With A Raised Feature As Mask
5443685 Composition And Method For Off-Axis Growth Sites On Nonpolar Substrates
5448590 Equalization Technique For Compensating For Degradation To The Transmission Of Digitally Modulated Signals
5454014 Digital Signal Processor
5457414 Power Supply Loss Sensor
5464783 Oxynitride-Dioxide Composite Gate Dielectric Process For Mos Manufacture
5465275 Efficient Utilization Of Present State/Next State Registers
5471500 Soft Symbol Decoding
5473701 Adaptive Microphone Array
5475345 Ultra-Fast Mos Device Circuits
5489552 Multiple Layer Tungsten Deposition Process
5490178 Power And Time Saving Initial Tracebacks
5500312 Masks With Low Stress Multilayer Films And A Process For Controlling The Stress Of Multilayer Films
5506908 Directional Microphone System
5513220 Digital Receiver With Minimum Cost Index Register
5519350 Circuitry For Delivering A Signal To Different Load Elements Located In An Electronic System
5528625 High Speed Quantization-Level-Sampling Modem With Equalization Arrangement
5537445 Variable Length Tracebacks
5546420 Methods Of And Devices For Enhancing Communications That Use Spread Spectrum Technology By Using Variable Code Techniques

5559503 Communications Device For Initializing Terminals In A Signal Distribution System
5559659 Enhanced Rc Coupled Electrostatic Discharge Protection
5559837 Efficient Utilization Of Present State/Next State Registers
5573965 Method Of Fabricating Semiconductor Devices And Integrated Circuits Using Sidewall Spacer Technology
5591037 Method For Interconnecting An Electronic Device Using A Removable Solder Carrying Medium
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5608397 Method And Apparatus For Generating Dc-Free Sequences
5618189 Solder Medium For Circuit Interconnection
5619514 In-Place Present State/Next State Registers
5636217 Method For Connecting Roaming Stations In A Source Routed Bridged Local Area Network
5636247 Information Transmission System
5643838 Low Temperature Deposition Of Silicon Oxides For Device Fabrication

5646619 Self-Calibrating High Speed D/A Converter
5654581 Integrated Circuit Capacitor
5668023 Composition For Off-Axis Growth Sites On Non-Polar Substrates
5670376 Methodology For Monitoring Solvent Quality
5693561 Method Of Integrated Circuit Fabrication Including A Step Of Depositing Tungsten
5706428 Multirate Wireless Data Communication System
5708389 Integrated Circuit Employing Quantized Feedback
5710430 Method And Apparatus For Terahertz Imaging
5712176 Doping Of Silicon Layers
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5724390 Mlse Before Derotation And After Derotation
5724393 Method And Apparatus Compensating For Effects Of Digital Loss Insertion In Signal Transmissions Between Modems
5728625 Process For Device Fabrication In Which A Thin Layer Of Cobalt Silicide Is Formed
5735963 Method Of Polishing
5739707 Wave Shaping Transmit Circuit
5748650 Digital Processor With Viterbi Process
5750312 Process For Fabricating A Device
5751065 Integrated Circuit With Active Devices Under Bond Pads
5807760 Method Of Despositing An Aluminum-Rich Layer
5831561 System And Method For Dynamically Optimizing A Symbol Table And Modem Employing The Same
5841813 Digital Communications System Using Complementary Codes And Amplitude Modulation
5862182 Ofdm Digital Communications System Using Complementary Codes

5870378 Method And Apparatus Of A Multi-Code Code Division Multiple Access Receiver Having A Shared Accumulator Circuits
5894125 Near Field Terahertz Imaging
5903037 Gaas-Based Mosfet, And Method Of Making Same

5909462	System And Method For Improved Spread Spectrum Signal Detection
5910950	Demodulator Phase Correction For Code Division Multiple Access Receiver
5935396	Method For Depositing Metal
5987033	Wireless Lan With Enhanced Capture Provision
5991287	System And Method For Providing Seamless Handover In A Wireless Computer Network
08/065328	Handover Method for Mobile Wireless Station
09/345919	An Integrated Circuit Including A DRAM Cell
09/356260	Method And System For Signalling
09/375645	CDMA System
09/379407	Instantaneous Clock And Data Recovery
09/411015	Oscillator Phase Noise Prediction
09/432725	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
09/454003	Define Via In Dual Damascene Process
09/459439	Communications System With Symmetrical Interfaces And Associated Methods
09/459831	Communications System And Associated Methods With Out-Of-Band Control
09/460165	Communications System Including Lower Rate Parallel Electronics With Skew Compensation And Associated Methods
09/488810	Wire Bonding Technique And Architecture Suitable For Copper Metallization In Semiconductor Structures
09/650038	Process For Fabricating Semiconductor Devices In Which The Distribution Of Dopants Is Controlled
09/712732	System And Method For Removal Of Material
09/742855	Optical Structures And Methods For X-Ray Applications
60/172654	X-Ray System And Method
Re32207	Method For Making Integrated Semiconductor Circuit Structure With Formation Of Ti Or Ta Silicide
Re34269	Semiconductor Integrated Circuit Packages

CONDITIONAL ASSIGNMENT OF AND SECURITY INTEREST IN PATENT RIGHTS

THIS CONDITIONAL ASSIGNMENT OF AND SECURITY INTEREST IN PATENT RIGHTS ("Conditional Assignment"), dated as of April 2, 2001, is made by AGERE SYSTEMS GUARDIAN CORP., a Delaware corporation (the "Obligor"), in favor of The Chase Manhattan Bank, a New York banking corporation, as Administrative Agent (the "Administrative Agent") for the Secured Parties referred to in the Guarantee and Collateral Agreement, dated as of April 2, 2001 (as amended, supplemented or otherwise modified from time to time, the "Guarantee and Collateral Agreement"), among Agere Systems Inc., a Delaware corporation, as the borrower (the "Borrower"), the Obligor, certain of its other subsidiaries and the Administrative Agent.

W I T N E S S E T H:

WHEREAS, pursuant to the 364-Day Revolving Credit and Term Loan Facility Agreement, dated as of February 22, 2001 (as amended, supplemented or otherwise modified from time to time, the "Credit Agreement"), among the Borrower, Lucent Technologies Inc. (solely to acknowledge its assignment of certain of its rights and obligations to the Borrower), the Lenders from time to time parties thereto and The Chase Manhattan Bank, as administrative agent, the Lenders have severally agreed to make Loans and other extensions of credit to the Borrower upon the terms and subject to the conditions set forth in the Credit Agreement;

WHEREAS, in connection with the Credit Agreement, the Borrower and certain of its subsidiaries, including the Obligor, have executed and delivered the Guarantee and Collateral Agreement in favor of the Administrative Agent, for the benefit of the Administrative Agent and the Lenders;

WHEREAS, pursuant to the Guarantee and Collateral Agreement, the Obligor pledged and granted to the Administrative Agent for the benefit of the Administrative Agent and the other Secured Parties a continuing security interest in all Intellectual Property, including the Patents; and

WHEREAS, the Obligor has duly authorized the execution, delivery and performance of this Conditional Assignment;

NOW THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, and in order to induce the Lenders to make their respective extensions of credit to the Borrower under the Credit Agreements, the Obligor agrees, for the benefit of the Administrative Agent and the other Secured Parties, as follows:

SECTION 1. Definitions. Unless otherwise defined herein or the context otherwise requires, terms used in this Conditional Assignment, including its preamble and recitals, have the meanings provided or provided by reference in the Guarantee and Collateral Agreement.

SECTION 2. Conditional Assignment and Grant of Security Interest. The Obligor hereby pledges and grants a continuing security interest in, and a right of setoff against, and effective upon demand made upon the occurrence and during the continuance of an Event of Default assigns, transfers and conveys, the Patents listed on Schedule A hereto, to the Administrative Agent, for the benefit of the Administrative Agent and the other Secured Parties, to secure payment, performance and observance of the Obligations.

SECTION 3. Purpose. This Conditional Assignment has been executed and delivered by the Obligor for the purpose of recording the conditional assignment and grant of security interest herein with the United States Patent and Trademark Office. The conditional assignment and security interest granted hereby has been granted to the Administrative Agent, for the benefit of the Secured Parties, in connection with the Guarantee and Collateral Agreement and is expressly subject to the terms and conditions thereof. The Guarantee and Collateral Agreement (and all rights and remedies of the Secured Parties thereunder) shall remain in full force and effect in accordance with its terms.

SECTION 4. Acknowledgment. The Obligor does hereby further acknowledge and affirm that the rights and remedies of the Administrative Agent with respect to the security interest in the Patents granted hereby are more fully set forth in the Credit Agreement and the Guarantee and Collateral Agreement, the terms and provisions of which (including the remedies provided for therein) are incorporated by reference herein as if fully set forth herein. For the avoidance of doubt, it is understood and agreed that any assignment of any Patent to the Administrative Agent or any other Person shall be subject to any licenses (and the rights granted therein) existing at the time of such assignment with respect to such Patent.

SECTION 5. Counterparts. This Conditional Assignment may be executed in counterparts, each of which will be deemed an original, but all of which together constitute one and the same original.

IN WITNESS WHEREOF, the parties hereto have caused this Conditional Assignment to be duly executed and delivered by their respective officers thereunto duly authorized as of the day and year first above written.

AGERE SYSTEMS GUARDIAN CORP.,

By: Paul Bento
Name:
Title:

THE CHASE MANHATTAN BANK,
as Administrative Agent for the Secured Parties

By:_____
Name:
Title:

STATE OF New Jersey)
) ss
COUNTY OF Hunterdon)

On the 2nd day of April, 2001, before me personally came Paul Bento, who is personally known to me to be the Vice President of Agere Systems Guardian Corp., a Delaware corporation; who, being duly sworn, did depose and say that ~~she~~/he is the Vice President in such corporation, the corporation described in and which executed the foregoing instrument; that ~~she~~/he executed and delivered said instrument pursuant to authority given by the Board of Directors of such corporation; and that ~~she~~/he acknowledged said instrument to be the free act and deed of said corporation.

DEBORAH W. FERGUSON
Notary Public, State of New Jersey
No. 2219308
Qualified in Hunterdon County
Commission Expires 10/30/2003

Notary Public

(PLACE STAMP AND SEAL ABOVE)

IN WITNESS WHEREOF, the parties hereto have caused this Conditional Assignment to be duly executed and delivered by their respective officers thereunto duly authorized as of the day and year first above written.

AGERE SYSTEMS GUARDIAN CORP.,

By:_____
Name:
Title:

THE CHASE MANHATTAN BANK,
as Administrative Agent for the Secured Parties

By:_____
Name: Robert H Kozlak
Title: V.P.

STATE OF New York)
) ss
COUNTY OF New York

On the 2nd day of April, 2001, before me personally came Thanks E. Kozlark, who is personally known to me to be the Vice President of The Chase Manhattan Bank, a New York banking corporation; who, being duly sworn, did depose and say that she/he is the Vice President in such corporation, the corporation described in and which executed the foregoing instrument; that she/he executed and delivered said instrument pursuant to authority given by the Board of Directors of such corporation; and that she/he acknowledged said instrument to be the free act and deed of said corporation.

Sandra M. Reddy
Notary Public

SANDRA M. REDDY
NOTARY PUBLIC, State of New York
No. 01RE6012762
Qualified in New York County
Commission Expires August 31, 2002

(PLACE STAMP AND SEAL ABOVE)

509265-0804-02381-NY03.2064683.3

SCHEDULE A

Patent/ Serial Number	Title
4347656	Method Of Fabricating Polysilicon Electrodes
4361461	Hydrogen Etching Of Semiconductors And Oxides
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5870378 Method And Apparatus Of A Multi-Code Code Division Multiple Access Receiver Having A Shared Accumulator Circuits
5894125 Near Field Terahertz Imaging
5903037 Gaas-Based Mosfet, And Method Of Making Same

5909462	System And Method For Improved Spread Spectrum Signal Detection
5910950	Demodulator Phase Correction For Code Division Multiple Access Receiver
5935396	Method For Depositing Metal
5987033	Wireless Lan With Enhanced Capture Provision
5991287	System And Method For Providing Seamless Handover In A Wireless Computer Network
08/065328	Handover Method for Mobile Wireless Station
09/345919	An Integrated Circuit Including A DRAM Cell
09/356260	Method And System For Signalling
09/375645	CDMA System
09/379407	Instantaneous Clock And Data Recovery
09/411015	Oscillator Phase Noise Prediction
09/432725	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
09/454003	Define Via In Dual Damascene Process
09/459439	Communications System With Symmetrical Interfaces And Associated Methods
09/459831	Communications System And Associated Methods With Out-Of-Band Control
09/460165	Communications System Including Lower Rate Parallel Electronics With Skew Compensation And Associated Methods
09/488810	Wire Bonding Technique And Architecture Suitable For Copper Metallization In Semiconductor Structures
09/650038	Process For Fabricating Semiconductor Devices In Which The Distribution Of Dopants Is Controlled
09/712732	System And Method For Removal Of Material
09/742855	Optical Structures And Methods For X-Ray Applications
60/172654	X-Ray System And Method
Re32207	Method For Making Integrated Semiconductor Circuit Structure With Formation Of Ti Or Ta Silicide
Re34269	Semiconductor Integrated Circuit Packages

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April 5, 2001

Re: Recordation of Conditional Assignment and Security Interest In Patent Rights

Commissioner of Patents and Trademarks
U.S. Patent and Trademark Office
Office of Public Records
Crystal Gateway 4, Room 335
Washington, D.C. 20231

Dear Madam or Sir:

Enclosed for recording please find a Conditional Assignment and Security Interest in Patent Rights in favor of The Chase Manhattan Bank, as Administrative Agent, covering 190 U.S. patents and patent applications.

A check in the amount of $ 7,600.00 has been enclosed to cover the filing fee. Please return confirmation of this filing to me at my firm's address as listed above.

Thank you for your consideration.

Respectfully submitted,

Alison Winick

Enclosures