04-06-2001

101657109

FORM PTO-1619A
Expires 06/30/99
OMB 0651-0027

U.S. Department of Commerce
Patent and Trademark Office
PATENT

3.16.01

CANCELLED

RECORDATION FORM COVER SHEET
PATENTS ONLY

TO: The Commissioner of Patents and Trademarks: Please record the attached original document(s) or copy(ies).

Submission Type

- [x] New
- [ ] Resubmission (Non-Recordation) Document ID#
- [ ] Correction of PTO Error Reel # Frame #
- [ ] Corrective Document Reel # Frame #

Conveyance Type

- [ ] Assignment
- [ ] Security Agreement
- [ ] License
- [ ] Change of Name
- [ ] Merger
- [x] Other Intelectual Property Partial Release

U.S. Government
(For Use ONLY by U.S. Government Agencies)
- [ ] Departmental File
- [ ] Secret File

Conveying Party(ies)

- [ ] Mark if additional names of conveying parties attached

Name (line 1): Credit Suisse First Boston — Execution Date (Month Day Year): March 3, 2001

Name (line 2):

Second Party

Name (line 1): — Execution Date (Month Day Year):

Name (line 2): 08310041

Receiving Party

- [ ] Mark if additional names of receiving parties attached

Name (line 1): Intersil Holding Corporation

Name (line 2):

Address (line 1): 7585 Irvine Center Drive

Address (line 2): Suite 100

Address (line 3): Irvine (City) CA (State/Country) 92618 (Zip Code)

- [ ] If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative is attached. *(Designation must be a separate document from Assignment.)*

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name:

Address (line 1):

Address (line 2):

Address (line 3):

Address (line 4):

04/05/2001 DBYRNE 00000332 08310041
01 FC:581 8440.00 OP

FOR OFFICE USE ONLY

Mail documents to be recorded with required cover sheet(s) information to:
Commissioner of Patents and Trademarks, Box Assignments , Washington, D.C. 20231

Correspondent Name and Address

Area Code and Telephone Number: 609-620-3218

Name: Daniel S. Goldberg

Address (line 1): Princeton Pike Corporate Center

Address (line 2): P.O. Box 5218

Address (line 3): Princeton, New Jersey 08543-5218

Address (line 4):

Pages

Enter the total number of pages of the attached conveyance document including any attachments. # 21

Application Number(s) or Patent Number(s)

☑ Mark if additional numbers attached

Enter either the Patent Application Number or the Patent Number (DO NOT ENTER BOTH numbers for the same property).

Patent Application Number(s)			Patent Number(s)		
08/310041	08/759865	08/873173	4344985	4374455	4417385
08/885228	09/036838	09/096217	4420765	4430792	4433008
09/098517	09/114769	09/167177	4441117	4443931	4455565

If this document is being filed together with a new Patent Application, enter the date the patent application was signed by the first named executing inventor. Month Day Year

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned.

PCT PCT PCT

PCT PCT PCT

Number of Properties

Enter the total number of properties involved. # 211

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): $ 8440.00

Method of Payment: Enclosed ☑ Deposit Account ☐

Deposit Account

(Enter for payment by deposit account or if additional fees can be charged to the account.)

Deposit Account Number: # 04-0480

Authorization to charge additional fees: Yes ☑ No ☐

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Daniel S. Goldberg	Daniel S. Goldberg	March 16, 2001
Name of Person Signing	Signature	Date

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Patent Application Number(s)			Patent Number(s)		
09/260411	09/283536	09/296472	4460913	4466176	4500609
09/303270	09/307879	09/314323	4500898	4505029	4506282
09/318334	09/338891	09/339356	4523111	4532534	4549926
09/344867	09/344868	09/345930	4561008	4571815	4578142
09/350575	09/358625	09/428616	4581626	4584028	4586240

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Enter either the Patent Application Number or the Patent Number (DO NOT ENTER BOTH numbers for the same property).

Patent Application Number(s)			Patent Number(s)		
09/449487	09/450872	09/498476	4587712	4587713	4597822
09/502712	09/525182	09/542561	4598461	4605948	4631564
09/551187	09/570009	09/603605	4634473	4639754	4639762
09/624533	09/649815	09/649837	4641162	4641164	4641174
09/654845	09/663235	09/664024	4644637	4645957	4646117

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Patent Application Number(s)			Patent Number(s)		
09/665850	09/689939	09/718219	4646129	4648174	4651179
09/726682	09/765177	60/198692	4656493	4661199	4663547
60/219858	60/234563		4675978	4677452	4682195
			4684413	4700460	4720308
			4739387	4743952	4749886

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Patent Application Number(s)			Patent Number(s)		
			4750666	4769744	4782379
			4783690	4794432	4799095
			4801985	4801986	4803533
			4809045	4809047	4810665
			4816422	4816892	4821095

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Patent Application Number(s)			Patent Number(s)		
			4823176	4837606	4847671
			4857977	4857983	4860080
			4883767	4890143	4901127
			4901135	4903189	4904609
			4910563	4927772	4933740

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Patent Application Number(s)			Patent Number(s)		
			4937467	4937644	4939101
			4941026	4967243	4969027
			4969028	4975751	4980740
			4980741	4982258	4985740
			4994871	4994883	4998151

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Patent Application Number(s)			Patent Number(s)		
			4999684	5018002	5023692
			5038197	5041896	5079608
			5082795	5091336	5095343
			5097319	5103290	5134321
			5148264	5164802	5218220

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			5243211	5293070	5317184
			5323036	5366932	5399892
			5422288	5424563	5446316
			5455442	5463344	5468668
			5473193	5497013	5577656

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			5594261	5654226	5694417
			5770878	5789982	5872028
			5877041	5877044	5880513
			5894141	5913130	5920452
			5940689	5970343	5995349

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			6037628	6054369	6055149
			6060795	6066878	6069403
			6077744	6078077	6080614
			6081009	6104062	6107127
			6110763	6110799	6121089

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Patent Application Number(s)			Patent Number(s)		
			6137139	6140152	6153495
			6162702	6188105	6188575
			6194290		

INTELLECTUAL PROPERTY PARTIAL RELEASE

THIS PARTIAL RELEASE dated as of March 2, 2001, by Credit Suisse First Boston, as Collateral Agent for the Lenders (as such terms are defined below). Terms used herein and not otherwise defined shall have the meanings assigned to such terms in the Credit Agreement referred to below.

W I T N E S S E T H :

WHEREAS, INTERSIL CORPORATION, a Delaware corporation (the "Borrower"), INTERSIL HOLDING CORPORATION, a Delaware corporation ("Holdings"), the LENDERS, and CREDIT SUISSE FIRST BOSTON, a bank organized under the laws of Switzerland, acting through its New York branch, as swingline lender, as an issuing bank, as administrative agent (in such capacity, the "Administrative Agent") and as collateral agent (in such capacity, the "Collateral Agent") are party to that certain Credit Agreement dated as of August 13, 1999, as amended by Amendment No. 1 and Waiver dated as of January 28, 2000, Amendment No. 2, Consent and Waiver dated as of May 5, 2000, Amendment No. 3 dated as of August 15, 2000, Consent and Waiver dated as of May 5, 2000, and Consent and Waiver dated as of January 26, 2001.

WHEREAS, the Borrower, Holdings and the domestic Subsidiaries (together with the Borrower and Holdings, the "Grantors") and the Collateral Agent are party to that certain Security Agreement dated as of August 13, 1999 (the "Security Agreement"), recorded by the United States Patent and Trademark Office on 1) March 1, 2000, at Reel No. 002035 and Frame No. 0506, 2) November 8, 1999, at Reel No. 010351 and Frame No. 0410, and 3) October 25, 1999, at Reel No. 001979 and Frame No. 0821, and pursuant to which, among other things, the Borrower and the Grantors granted a security interest to the Collateral Agent for the benefit of the Secured Parties in certain Collateral (as defined in the Security Agreement).

WHEREAS, as a result of the sale of the discrete power division of the Borrower pursuant to the Asset Purchase Agreement, by and among the Borrower, Intersil (Pennsylvania) LLC and Fairchild Semiconductor Corporation, dated as of January 20, 2001, the Collateral Agent has agreed to release of record its interest in the Collateral described on Schedules I - IV hereto;

NOW, THEREFORE, for good and valuable consideration, receipt and sufficiency of which are hereby acknowledged, the Collateral Agent hereby releases of record the security interest in the Collateral described on Schedules I - IV attached hereto.

IN WITNESS WHEREOF, the Collateral Agent has caused this Partial Release to be duly executed by its duly authorized officer as of the day and year above written.

CREDIT SUISSE FIRST BOSTON, as Collateral Agent,

by _____
Name: LALITA ADVANI
Title: ASSISTANT VICE PRESIDENT

by _____
Name: David L. Sawyer
Title: Vice President

STATE OF NEW YORK,)
) ss.:
COUNTY OF NEW YORK,)

The foregoing instrument was executed and acknowledged to me this 3 day of March, 2001 by Lalita Advani and David L. Sawyer, duly authorized officers of Credit Suisse First Boston.

Phyllis Tannenbaum
Notary Public

[Notarial Seal]

My commission expires:

PHYLLIS TANNENBAUM
Notary Public, State of New York
No. 01TA6015790
Qualified in Nassau County
Certificate Filed in New York County
Commission Expires November 8, 2002

<<NYCORP~1230769.1:4236D:03/01/01-7:42p>>

COPYRIGHTS OWNED BY INTERSIL CORPORATION

U.S. Copyright Registrations

None

Pending U.S. Copyright Applications for Registration

None

Non-U.S. Copyright Registrations

None

Non-U.S. Pending Copyright Applications for Registration

None

LICENSES

PART I

LICENSES/SUBLICENSES OF INTERSIL CORPORATION ON DATE HEREOF

A. Copyrights

None

B. Patents

None

C. Trademarks

None

D. Others

None

PART 2

LICENSES/SUBLICENSES OF INTERSIL CORPORATION AS LICENSEE ON DATE HEREOF

A. Copyrights

None

B. Patents

None

C. Trademarks

None

D. Others

None

SCHEDULE III

PATENTS OWNED BY INTERSIL CORPORATION

U.S. Patents

See Attached

U.S. Patent Applications

See Attached

Non-U.S. Patents

None

Non-U.S. Patent Applications

None

TRADEMARKS OWNED BY INTERSIL CORPORATION

U.S. Trademark Registrations

Record Owner in Patent and Trademark Office
Harris Corporation

Mark	Registration Date	Registration Number
LITTLEFET	09-23-1997	2,099,961
ULTRAFET	12-01-1998	2,206,791

U.S. Trademark Applications

Record Owner in Patent and Trademark Office
Intersil Corporation

Mark	Application Date	Application Number
ECOSPARK	06-30-2000	76/082,000
MICROFET	07-11-2000	76/086,566
STEALTH	07-21-2000	76/093,041
ULTRAFET & Design	09-22-2000	76/135,937

State Trademark Registrations

None

State Trademark Applications

None

Non-U.S. Trademark Registrations

None

Non-U.S. Trademark Applications

None

Trade Names

None

ISSUED PATENTS
OWNER: INTERSIL CORPORATION

Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
XRCA76036	METHOD OF PASSIVATING A SEMICONDUCTOR DEVICE WITH	US	248208	27-Mar-81	4344985	17-Aug-82
XRCA73807B	METHOD FOR MANUFACTURING A VERTICAL, GROOVED MOSFE	US	351250	22-Feb-82	4374455	22-Feb-83
RD 12966	SELF ALIGNED, MINIMUM MASK PROC FOR MFG INSULATED GATE SEMI DEVICES WITH INTEGRAL SHORTS	US	406731	09-Aug-82	4417385	29-Nov-83
XRCA72915	MULTI-LAYER PASSIVANT SYSTEM	US	268284	29-May-81	4420765	13-Dec-83
RD 14566	SELF ALIGNED MINIMAL MASK PROCESS EMPLOY 2-STEP ETCH FOR MFG INSUL GATE SEMICONDUCTORS	US	406738	09-Aug-82	4430792	14-Feb-84
XRCA75702	DOPED-OXIDE DIFFUSION OF PHOSPHORUS USING BOROPHOS	US	377197	11-May-82	4433008	21-Feb-84
28-IS-0008	MONOLITHICALLY MERGED FET AND BIPOLAR JUNCTION TRANSISTOR	US	287497	27-Jul-81	4441117	03-Apr-84
RD 14247	METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH A BASE REGION HAVING A DEEP PORTION	US	392870	28-Jun-82	4443931	24-Apr-84
XRCA74309A	VERTICAL MOSFET WITH AN ALIGNED GATE ELECTRODE AND	US	234834	13-Feb-81	4455565	19-Jun-84
XRCA72862	FAST SWITCHING TRANSISTOR	US	316660	30-Oct-81	4460913	17-Jul-84
RD 15071	SELF ALIGNED MINIMAL MASK PROCESS FOR MFG INSULATED GATE SEMI DEVICES WITH INTEGRAL SHORTS	US	502834	09-Jun-83	4466176	21-Aug-84
RD 12201	METHOD FOR PRODUCING EUTECTICS AS THIN FILMS	US	245764	20-Mar-81	4500609	19-Feb-85
RD 13626	METHOD FOR MAKING SEMICONDUCTOR DEVICES UTILIZING EUTECTIC	US	395761	06-Jul-82	4500898	19-Feb-85
28-SP-1307	SEMICONDUCTOR DEVICE WITH BUILT UP LOW RESISTANCE CONTACT	US	501745	08-Jul-83	4505029	19-Mar-85
RD 13310	NORMALLY OFF SEMICONDUCTOR DEVICE WITH LOW ON-RESISTANCE AN	US	455174	03-Jan-83	4506282	19-Mar-85
RD 14619	NORMALLY-OFF, GATE-CONTROLLED ELECTRICAL CIRCUIT WITH LOW ON-RESISTANCE	US	473089	07-Mar-83	4523111	11-Jun-85
XRCA78562	MOSFET WITH PERIMETER CHANNEL	US	415486	07-Sep-82	4532534	30-Jul-85

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
XRCA76808A	METHOD FOR GROWING MONOCRYSTALLINE SILICON ON A MA	US	553305	18-Nov-83	4549926	29-Oct-85
XRCA70125	BALLASTED, GATE CONTROLLED SEMICONDUCTOR DEVICE	US	870484	18-Jan-78	4561008	24-Dec-85
RD 16096	VERTICAL CHANNEL FIELD CONTROLLED DEVICE EMPLOYING A RECESS	US	650315	12-Sep-84	4571815	25-Feb-86
XRCA76808B	METHOD FOR GROWING MONOCRYSTALLINE SILICON THROUGH	US	608544	10-May-84	4578142	25-Mar-86
RD 11748	INSULATED GATE TURNOFF THYRISTORS AND TRANSISTORS	US	28576	09-Apr-79	4581626	08-Apr-86
XRCA80099	NEUTRALIZATION OF ACCEPTOR LEVELS IN SILICON BY AT	US	653559	24-Sep-84	4584028	22-Apr-86
XRCA76695A	VERTICAL IGFET WITH INTERNAL GATE AND METHOD FOR MAKING SAME	US	748940	26-Jun-85	4586240	06-May-86
RD 16329	VERTICAL CHANNEL FIELD CONTROLLED DEVICE EMPLOYING A RECESSED GATE STRUCTURE AND METHOD FOR MAKING	US	692073	17-Jan-85	4587712	13-May-86
XRCA79967	METHOD FOR MAKING VERTICAL MOSFET WITH REDUCED BIPOLAR EFFECTS	US	582601	22-Feb-84	4587713	13-May-86
28-SP-1305	METHOD FOR MAKING SILICON WAFERS	US	717364	28-Mar-85	4597822	01-Jul-86
RD 16326	SELF ALIGNED POWER MOSFET WITH INTERGRAL SOURCE-BASE SHORT AND METHODS FOR MAKING	US	693643	22-Jan-85	4598461	08-Jul-86
XRCA79781	SEMICONDUCTOR STRUCTURE FOR ELECTRIC FIELD DISTRIBUTION	US	637027	02-Aug-84	4605948	12-Aug-86
XRCA81062	GATE SHIELD STRUCTURE FOR POWER MOS DEVICE	US	664027	23-Oct-84	4631564	23-Dec-86
XRCA81626	METHOD FOR FABRICATING A RADIATION HARDENED OXIDE HAVING STRUCTURAL DAMAGE	US	773772	09-Sep-85	4634473	06-Jan-87
XRCA81313	VERTICAL MOSFET WITH DIMINISHED BIPOLAR EFFECTS	US	705371	25-Feb-85	4639754	27-Jan-87
XRCA79552	MOSFET WITH REDUCED BIPOLAR EFFECTS	US	605427	30-Apr-84	4639762	27-Jan-87
28-SP-1344	CURRENT LIMITED INSULATED GATE DEVICE	US	807597	11-Dec-85	4641162	03-Feb-87

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XRCA83282	BIDIRECTIONAL VERTICAL POWER MOS DEVICE AND FABRICATION MET	US	868633	30-May-86	4641164	03-Feb-87
RD 13565	PINCH RECTIFIER	US	510520	08-Aug-83	4641174	03-Feb-87
RD 12878	INSULATED GATE SEMICONDUCTOR DEVICE WITH IMPROVED SHORTING REGION AND METHOD OF MAKING	US	567116	30-Dec-83	4644637	24-Feb-87
RD 16293	NORMALLY OFF SEMICONDUCTOR DEVICE WITH LOW ON-RESISTANCE AND CIRCUIT ANALOGUE	US	685632	24-Dec-84	4645957	24-Feb-87
RD 15327	POWER SEMICONDUCTOR DEVICES WITH INCREASED TURN-OFF CURRENT RATINGS	US	678530	05-Dec-84	4646117	24-Feb-87
RD 17393	HERMETIC POWER CHIP PACKAGES	US	872792	11-Jun-86	4646129	24-Feb-87
RD 16144	METHOD OF MAKING HIGH BREAKDOWN VOLTAGE SEMICONDUCTOR DEVICE	US	698495	05-Feb-85	4648174	10-Mar-87
XRCA78841A	LOW RESISTANCE GALLIUM ARSENIDE FIELD EFFECT TRANSISTOR	US	749091	26-Jun-85	4651179	17-Mar-87
RD 16362	BIDIRECTIONAL HIGH SPEED POWER MOSFET DEVICES WITH DEEP LEVEL RECOMBINATION CENSORS IN BASE REGION	US	698498	05-Feb-85	4656493	07-Apr-87
XRCA81843	METHOD TO INHIBIT AUTODOPING IN EPITAXIAL LAYERS	US	797126	12-Nov-85	4661199	28-Apr-87
RD 13176	COMPOSITE CIRCUIT FOR POWER SEMICONDUCTOR SWITCHING	US	257080	24-Apr-81	4663547	05-May-87
XRCA80123	METHOD FOR FABRICATING A RADIATION HARDENED OXIDE	US	773771	09-Sep-85	4675978	30-Jun-87
28IS0007A	POWER FIELD-EFFECT TRANSISTOR STRUCTURES	US	767052	16-Aug-85	4677452	30-Jun-87
28-SP-1336	IMPROVED INSULATED GATE DEVICE	US	781383	30-Sep-85	4682195	21-Jul-87
XRCA82194	METHOD FOR INCREASING THE SWITCH SPEED OF A SEMI DEVICE BY NEUTRON IRRADIATION	US	784726	07-Oct-85	4684413	04-Aug-87
XRCA83282A	BIDIRECTIONAL VERTICAL POWER MOS DEVICE AND FABRICATION METHOD	US	924865	30-Oct-86	4700460	20-Oct-87
RD 17192	METHOD FOR PRODUCING HIGH ASPECT RATIO HOLLOW DIFFUSED REGI	US	843346	24-Mar-86	4720308	19-Jan-88

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RD 15057	SCR HAVING HIGH GATE SENSITIVITY AND HIGH DV/DT RATING	US	497339	23-May-83	4739387	19-Apr-88
RD 14617	INSULATED GATE SEMICONDUCTOR DEVICE WITH LOW ON RESISTANCE	US	482075	04-Apr-83	4743952	10-May-88
28-IS-0056	REDUCED PARALLEL EXCLUSIVE OR AND EXCLUSIVE NOR GATE	US	916869	09-Oct-86	4749886	07-Jun-88
RD 16758	METHOD OF FABRICATING GOLD BUMPS ON IC'S AND POWER CHIPS	US	853255	17-Apr-86	4750666	14-Jun-88
RD 17267	SEMICONDUCTOR CHIP PACKAGES HAVING SOLDER LAYERS OF ENHANCED DURABILITY	US	851275	10-Apr-86	4769744	06-Sep-88
RD 17963	SEMICONDUCTOR DEVICE HAVING RAPID REMOVAL OF MAJORITY CARRI	US	40693	17-Apr-87	4782379	01-Nov-88
RD 17481	POWER SEMICONDUCTOR DEVICE WITH MAIN CURRENT SECTION AND EMULATION CURRENT SECTION	US	892739	31-Jul-86	4783690	08-Nov-88
28SP01350	MOSFET STRUCTURE WITH SUBSTRATE COUPLED SOURCE	US	7034	27-Jan-87	4794432	27-Dec-88
RD 17439	METAL OXIDE SEMICONDUCTOR GATED TURN OFF THYRISTOR	US	69806	06-Jul-87	4799095	17-Jan-89
RD 17250	IMPROVED MONLITHICALLY INTEGRATED SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATION	US	51359	19-May-87	4801985	31-Jan-89
RD 17153	VERTICAL DOUBLE DIFFUSED METAL OXIDE SEMI (VDMOS) DEVICE WITH INCREASED SAFE OP AREA AND METHOD	US	33940	03-Apr-87	4801986	31-Jan-89
28-SP-1354	IGT AND MOSFET DEVICES HAVING REDUCED CHANNEL WIDTH	US	913785	30-Sep-86	4803533	07-Feb-89
28-SP-1311	INSULATED GATE DEVICE	US	781381	30-Sep-85	4809045	28-Feb-89
RD 18409	INSULATED-GATE SEMICONDUCTOR DEVICE WITH IMPROVED BASE-TO SOURCE ELECTRODE SHORT & METHOD OF FAB SAID SHORT	US	98756	17-Sep-87	4809047	28-Feb-89
28SP1355A	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION	US	77711	24-Jul-87	4810665	07-Mar-89
RD 17193	FABRICATION OF LARGE POWER SEMICONDUCTOR COMPOSITE BY WAFER INTERCONNECTION OF INDIVIDUAL DEVICES	US	947151	29-Dec-86	4816422	28-Mar-89
RD 17967	SEMICONDUCTOR DEVICE HAVING TURN-ON AND TURN-OFF CAPABILITI ES	US	36058	09-Apr-87	4816892	28-Mar-89

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RD 16136	INSULATED GATE SEMICONDUCTOR DEVICE WITH EXTRA SHORT GRID AND METHOD OF FABRICATION	US	25036	12-Mar-87	4821095	11-Apr-89
RD 17152	VERTICAL DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR (VDMOS) DEVICE INCL HI VOLT JUNCTION EXHIB INCREASE SAFE OP AREA	US	33952	03-Apr-87	4823176	18-Apr-89
RD 17842P	VERTICAL MOSFET WITH REDUCED BIPOLAR EFFECTS	US	14196	12-Feb-87	4837606	06-Jun-89
RD 17185	MONOLITHICALLY INTEGRATED INSULATED GATE SEMICONDUCTOR DEVICE	US	51424	19-May-87	4847671	11-Jul-89
RD 15457	LATERAL METAL-OXIDE-SEMICONDUCTOR CONTROLLED TRIACS	US	88353	24-Aug-87	4857977	15-Aug-89
RD 17298	MONOLITHICALLY INTEGRATED SEMICONDUCTOR DEVICE HAVING REVERSES CONDUCTING CAPAB & METHOD OF FABRICATION	US	51430	19-May-87	4857983	15-Aug-89
28-SP-1381	IMPROVED ISOLATION FOR TRANSISTOR DEVICES HAVING A PILOT STRUCTURE	US	32367	31-Mar-87	4860080	22-Aug-89
RD 18923	METHOD OF FABRICATING SELF-ALIGNED SEMICONDUCTOR DEVICES	US	220353	14-Jul-88	4883767	28-Nov-89
RD 17296	PROTECTIVE CLAMP FOR MOS GATED DEVICES	US	225320	28-Jul-88	4890143	26-Dec-89
RD 18425	CIRCUIT INCLUDING A COMBINED INSULATED GATE BIPOLAR TRANSISTOR MOSFET	US	254897	07-Oct-88	4901127	13-Feb-90
28-MT-0010	HERMETICALLY SEALED HOUSING WITH WELDING SEAL	US	232197	15-Aug-88	4901135	13-Feb-90
RD 18753	LOW NOISE, HIGH FREQUENCY SYNCHRONOUS RECTIFIER	US	186983	27-Apr-88	4903189	20-Feb-90
RD 15798	SYMMETRICAL BLOCKING HIGH VOLTAGE BREAKDOWN SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION	US	190903	06-May-88	4904609	27-Feb-90
XRCA82205	COMPLEMENTARY CIRCUIT AND STRUCTURE WITH COMMON SUBSTRATE	US	232243	15-Aug-88	4910563	20-Mar-90
RD 19134	HIGH BREAKDOWN VOLTAGE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION	US	358057	30-May-89	4927772	22-May-90
RD 18994	INSULATED GATE TRANSISTOR WITH VERTICAL INTEGRAL DIODE AND METHOD OF FABRICATION	US	243211	09-Sep-88	4933740	12-Jun-90
RD 19815P	COMPLEMENTARY CIRCUIT AND STRUCTURE WITH COMMON SUBSTRATE	US	411424	22-Sep-89	4937467	26-Jun-90

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
RD 16683	ASYMMETRICAL FIELD CONTROLLED THYRISTOR	US	756478	17-Jul-85	4937644	26-Jun-90
RD 17766	DIRECT-BONDED WAFERS HAVING A VOID FREE INTERFACE AND METHOD OF FABRICATION	US	240332	06-Sep-88	4939101	03-Jul-90
RD 19013	SEMICONDUCTOR DEVICES EXHIBITING MINIMUM ON RESISTANCE	US	07/239014	26-Aug-88	4941026	10-Jul-90
RD 16131	POWER TRANSISTOR STRUCTURE WITH HIGH SPEED INTEGRAL ANTIPAR	US	221482	19-Jul-88	4967243	30-Oct-90
RD 16132	POWER BIPOLAR TRANSISTOR DEVICE WITH INTEGRAL ANTISATURATION DIODE	US	220649	18-Jul-88	4969027	06-Nov-90
RD 20166	GATE ENHANCED RECTIFIER	US	07/492377	08-Mar-90	4969028	06-Nov-90
SE-368	HIGH BREAKDOWN ACTIVE DEVICE STRUCTURE WITH LOW SERIES RESISTANCE	US	253437	05-Oct-88	4975751	04-Dec-90
RD 17716	MOS-PILOT STRUCTURE FOR INSULATED GATE TRANSISTOR	US	329034	27-Mar-89	4980740	25-Dec-90
RD 13256	MOS PROTECTION DEVICE	US	308498	10-Feb-89	4980741	25-Dec-90
RD 18054	METAL OXIDE SEMICONDUCTOR GATED TURN-OFF THYRISTOR INCLUDIN	US	188888	02-May-88	4982258	01-Jan-91
RD 18033	POWER FIELD EFFECT DEVICES HAVING LOW GATE SHEET RESISTANCE	US	359811	01-Jun-89	4985740	15-Jan-91
RD 18594	INSULATED GATE BIPOLAR TRANSISTOR WITH IMPROVED LATCHUP CURRENT LEVEL AND SAFE OPERATING AREA	US	07/279392	02-Dec-88	4994871	19-Feb-91
RD 18544	FIELD CONTROLLED DIODE (FCD) HAVING MOS TRENCH GATES	US	07/416171	02-Oct-89	4994883	19-Feb-91
RD 16969	POWER FIELD EFFECT DEVICES HAVING SMALL CELL SIZE AND LOW CONTACT RESISTANCE AND METHOD OF FABRICATION	US	337684	13-Apr-89	4998151	05-Mar-91
RD 19918	SYMMETRICAL BLOCKING HI VOLTAGE BREAKDOWN SEMI DEVICE AND METHOD OF FABRICATION	US	07/435632	13-Nov-89	4999684	12-Mar-91
RD 19321	HI CURRENT HERMETIC PACKAGE INCL AN INTERNAL FOIL AND HAVING A LEAD EXTENDING THROUGH THE PACK LID AND PACK CHIP	US	07/375641	03-Jul-89	5018002	21-May-91
28-MT-0014	POWER MOSFET TRANSISTOR CIRCUIT	US	447330	07-Dec-89	5023692	11-Jun-91

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
28-MT-0019	HERMETICALLY SEALED DIE PACKAGE WITH FLOATING SOURCE	US	545218	26-Jun-90	5038197	06-Aug-91
RD 18802	SYMMETRICAL BLOCKING HIGH VOLTAGE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION	US	07/376073	06-Jul-89	5041896	20-Aug-91
28-MT-0016	POWER MOSFET TRANSISTOR CIRCUIT WITH ACTIVE CLAMP	US	07/609685	06-Nov-90	5079608	07-Jan-92
RD 19140	METHOD OF FABRICATING A FIELD EFFECT SEMICONDUCTOR DEVICE HAVING A SELF ALIGNED STRUCTURE	US	267757	01-Nov-88	5082795	21-Jan-92
SE-368	HIGH BREAKDOWN ACTIVE DEVICE STRUCTURE WITH LOW SERIES RESISTANCE	US	07/592308	03-Oct-90	5091336	25-Feb-92
28MT0013A	POWER MOSFET	US	07/609054	06-Nov-90	5095343	10-Mar-92
28-MT-0021	COVER WITH THROUGH TERMINALS FOR A HERMETICALLY SEALED ELECTRONIC PACKAGE	US	07/672997	21-Mar-91	5097319	17-Mar-92
RD 18934	HERMETIC PACKAGE HAVING A LEAD EXTENDING THROUGH AN APERTURE IN THE PACKAGE LID AND PACKAGED SEMICONDUCTOR CHIP	US	07/367525	16-Jun-89	5103290	07-Apr-92
28-SV-0056	POWER MOSFET AC POWER SWITCH EMPLOYING MEANS FOR PREVENTING CONDUCTION OF BODY DIODE	US	07/644569	23-Jan-91	5134321	28-Jul-92
28-MT-0018	HIGH CURRENT HERMETIC PACKAGE	US	07/517799	02-May-90	5148264	15-Sep-92
28-MT-0020	POWER VDMOSFET WITH SCHOTTKY ON LIGHTLY DOPED DRAIN OF LATERAL DRIVER FET	US	07/672243	20-Mar-91	5164802	17-Nov-92
28-MT-0032	POWER FET HAVING REDUCED THRESHOLD VOLTAGE	US	07/789901	12-Nov-91	5218220	08-Jun-93
28-MT-0030	MOSFET WITH SHIELDED CHANNEL	US	07/797054	25-Nov-91	5243211	07-Sep-93
RD 19906	INTEGRATED HEAT SINK FOR SEMICONDUCTOR MODULES	US	07/973603	09-Nov-92	5293070	08-Mar-94
28-MT-0052	DEVICE AND METHOD FOR IMPROVING CURRENT CARRYING CAPABILITY IN A SEMICONDUCTOR DEVICE	US	07/973709	09-Nov-92	5317184	31-May-94
28-MT-0031	ATOMIC LATICED LAYOUT	US	07/822732	21-Jan-92	5323036	21-Jun-94
28-MT-0048	SEMICONDUCTOR CHIP HAVING INTERDIGITATED GATE RUNNERS WITH GATE BONDING PADS	US	51832	26-Apr-93	5366932	22-Nov-94

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
28-MT-0055	METHOD OF FORMING MOS-GATED SEMICONDUCTOR DEVICES HAVING MESH GEOMETRY PATTERN	US	08/158444	29-Nov-93	5399892	21-Mar-95
28-MT-0037	METHOD OF DOPING A JFET REGION IN A MOS-GATED SEMICONDUCTOR DEVICE	US	08/246307	19-May-94	5422288	06-Jun-95
28-MT-0043	APPARATUS AND METHOD FOR INCREASING BREAKDOWN VOLTAGE RUGGEDNESS IN SEMICONDUCTOR DEVICES	US	08/173077	27-Dec-93	5424563	13-Jun-95
28-MT-0033	METHOD OF PACKAGING A SEMICONDUCTOR DEVICE	US	08/217801	06-Jan-94	5446316	29-Aug-95
XRCA83915	COMFET SWITCH AND METHOD	US	08/375714	20-Jan-95	5455442	03-Oct-95
28-MT-0041	FAST TURN ON SWITCH CIRCUIT WITH PARALLEL MOS CONTROLLED THYRISTOR AND SILICON CONTROLLED THYRISTOR AND SILICON CONTROLLED RECTIFIER	US	08/051839	26-Apr-93	5463344	31-Oct-95
28-MT-0055	METHOD OF FORMING MOS-GATED SEMICONDUCTOR DEVICES HAVING MESH GEOMETRY PATTERN	US	08/368612	04-Jan-95	5468668	21-Nov-95
28-MT-0034	PACKAGE FOR PARALLEL SUBELEMENT SEMICONDUCTOR DEVICES	US	08/177974	06-Jan-94	5473193	05-Dec-95
28-MT-0048	SEMICONDUCTOR CHIP HAVING INTERDIGITATED GATE RUNNERS WITH GATE BONDING PADS	US	08/276464	18-Jul-94	5497013	05-Mar-96
28-MT-0033	METHOD OF PACKAGING A SEMICONDUCTOR DEVICE	US	08/462856	05-Jun-95	5577656	26-Nov-96
28-MT-0039	METHOD AND DEVICE FOR ISOLATING PARALLEL SUB-ELEMENTS WITH REVERSE CONDUCTING DIODE REGIONS	US	08/223425	05-Apr-94	5594261	14-Jan-97
28-MT-0044	WAFER BONDING FOR POWER DEVICES	US	08/305435	07-Sep-94	5654226	05-Aug-97
SE-1146-TL	SHORT BURST DIRECT ACQUISITION DIRECT SEQUENCE SPREAD SPECTRUM RECEIVER	US	08/509590	31-Jul-95	5694417	02-Dec-97
SE-1180-TD	TRENCH MOS GATE DEVICE	US	08/636904	10-Apr-96	5770878	23-Jun-98
SE-1129-TL	LOW DISTORTION FEEDBACK IC AMPLIFIER AND METHOD	US	08/712562	11-Sep-96	5789982	04-Aug-98
SE-1203-PD	METHOD OF FORMING POWER SEMICONDUCTOR DEVICES WITH CONTROLLABLE INTEGRATED BUFFER	US	08/708712	05-Sep-96	5872028	16-Feb-99
SE-1284-TD	SELF-ALIGNED POWER FIELD EFFECT TRANSISTOR IN SILICON CARBIDE	US	08/884726	30-Jun-97	5877041	02-Mar-99

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SE-1295-PD	METHOD OF MAKING MOS-GATED SEMICONDUCTOR DEVICES	US	08/814842	11-Mar-97	5877044	02-Mar-99
SE-1055-PD	ASYMMETRIC SNUBBER RESISTOR	US	08/634371	18-Apr-96	5880513	09-Mar-99
SE-1246-PD	BIPOLAR SEMICONDUCTOR POWER CONTROLLING DEVICES WITH HETEROJUNCTION	US	08/885227	30-Jun-97	5894141	13-Apr-99
SE-1220-TD	METHOD FOR FABRICATING A POWER DEVICE	US	08/662118	12-Jun-96	5913130	15-Jun-99
SE-1358-PD	CIRCUIT AND METHOD FOR PROTECTING FROM OVERCURRENT CONDITIONS AND DETECTING AN OPEN ELECTRICAL LOAD	US	09/088198	01-Jun-98	5920452	06-Jul-99
SE-1236-PD	METHOD OF FABRICATING UMOS SEMICONDUCTOR DEVICES USING A SELF-ALIGNED, REDUCED MASK PROCESS	US	08/885921	30-Jun-97	5940689	17-Aug-99
SE-1320-PD	FABRICATION OF CONDUCTIVITY ENHANCED MOS-GATED SEMICONDUCTOR DEVICES	US	08/133030	12-Aug-98	5970343	19-Oct-99
SE-1143-PD	PROTECTION DEVICE FOR SOLID STATE SWITCHED POWER ELECTRONICS	US	08/944513	06-Oct-97	5995349	30-Nov-99
SE-1194-PD	A NOVEL TRENCH MOSFET PROCESS	US	08/885922	30-Jun-97	6037628	14-Mar-00
SE-1253-PD	IMPROVED LIFETIME CONTROL FOR SEMICONDUCTOR DEVICES	US	08/885878	30-Jun-97	6054369	25-Apr-00
SE-1370-PD	CURRENT LIMITED, THERMALLY PROTECTED, POWER DEVICE	US	09/203700	02-Dec-98	6055149	25-Apr-00
SE-1156-PD	SEMICONDUCTOR POWER PACK	US	09/040112	18-Mar-98	6060795	09-May-00
SE-1273-PD	HIGH VOLTAGE MOSFET STRUCTURE	US	09/108962	02-Jul-98	6066878	23-May-00
SE-1362-PD	POWER MODULE WITH LOWERED INDUCTANCE AND REDUCED VOLTAGE OVERSHOOTS	US	09/167203	06-Oct-98	6069403	30-May-00
SE-1403-PD	SEMICONDUCTOR TRENCH MOS DEVICES	US	09/255092	22-Feb-99	6077744	20-Jun-00
SE-1220-TD	METHOD FOR FABRICATING A POWER DEVICE	US	09/330437	11-Jun-99	6078077	20-Jun-00
SE-1267-PD	METHOD OF MAKING A MOS-GATED SEMICONDUCTOR DEVICE WITH A SINGLE DIFFUSION	US	08/885877	30-Jun-97	6080614	27-Jun-00

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
SE-1273-PD	HIGH VOLTAGE MOSFET STRUCTURE	US	08/966867	10-Nov-97	6081009	27-Jun-00
SE-1433-PD	SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS	US	09/107721	30-Jun-98	6104062	15-Aug-00
SE-1365-PD	METHOD OF MAKING SHALLOW WELL MOSFET STRUCTURE	US	09/145513	02-Sep-98	6107127	22-Aug-00
SE-1233-PD	ONE MASK POWER SEMICONDUCTOR FABRICATION PROCESS	US	08/861562	22-May-97	6110763	29-Aug-00
SE-1194-PD	A NOVEL TRENCH MOSFET PROCESS	US	08/885879	30-Jun-97	6110799	29-Aug-00
SE-1386-PD	METHODS OF FORMING POWER SEMICONDUCTOR DEVICES HAVING MERGED SPLIT-WELL BODY REGIONS THEREIN AND DEVICES FORMED THEREBY	US	09/092334	05-Jun-98	6121089	19-Sep-00
SE-1423-PD	LOW VOLTAGE DUAL-WELL MOS DEVICE HAVING HIGH RUGGEDNESS, LOW ON-RESISTANCE, AND IMPROVED BODY DIODE REVERSE RECOVERY	US	09/324553	03-Jun-99	6137139	24-Oct-00
SE-1362-PD	POWER MODULE WITH LOWERED INDUCTANCE AND REDUCED VOLTAGE OVERSHOOTS	US	09/334098	16-Jun-99	6140152	31-Oct-00
SE-1418-PD	ADVANCED METHODS FOR MAKING SEMICONDUCTOR DEVICES BY LOW TEMPERATURE DIRECT BONDING	US	09/036815	09-Mar-98	6153495	28-Nov-00
SE-1435-PD	SELF-SUPPORTING ULTRATHIN SILICON WAFER PROCESS	US	09/334835	17-Jun-99	6162702	19-Dec-00
SE-1496-PD	HIGH DENSITY MOS-GATED POWER DEVICE AND PROCESS FOR FORMING SAME	US	09/283531	01-Apr-99	6188105	13-Feb-01
SE-1356-PD	HEAT EXCHANGING CHASSIS AND METHOD	US	09/107273	30-Jun-98	6188575	13-Feb-01
SE-1414-PD	METHODS FOR MAKING SEMICONDUCTOR DEVICES BY LOW TEMPERATURE DIRECT BONDING	US	09/037723	09-Aug-00	6194290	27-Feb-01
RD 18593	FET, IGBT AND MCT STRUCTURES TO ENHANCE OPERATING CHARACTER	US	08/310041	22-Sep-94		
SE-1079-PD	A METHOD OF METALIZING A SEMICONDUCTOR POWER DEVICE CERAMIC MEMBER	US	08/759865	18-Apr-00		
SE-1047-PD	MEGASONIC PLL POWER GENERATOR	US	08/873173	11-Jun-97		
SE-1272-PD	SEMICONDUCTOR DEVICE GATE STRUCTURE FOR THERMAL OVERLOAD PROTECTION	US	08/885228	30-Jun-97		

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Docket No.	Title	Country	Apl #	Filing Date	Pat #	Issue Date
SE-1419-PD	DEVICES FORMABLE BY LOW TEMPERATURE DIRECT BONDING	US	09/036838	09-Mar-98		
SE-1180-TD	TRENCH MOS GATE DEVICE	US	09/096217	11-Jun-98		
SE-1190-PD	HIGH PERFORMANCE HEAT EXCHANGER AND METHOD	US	09/098517	17-Jun-98		
SE-1333-PD	CONDUCTIVITY ENHANCED MOS-GATED SEMICONDUCTOR DEVICES	US	09/114769	14-Jul-98		
SE-1382-PD	PROCESS FOR FORMING HIGH VOLTAGE JUNCTION TERMINATION EXTENSION OXIDE	US	09/167177	06-Oct-98		
SE-1503-PD	MOS-GATED DEVICE HAVING A BURIED GATE AND PROCESS FOR FORMING SAME	US	09/260411	01-Mar-99		
SE-1469-PD	IMPROVED POWER TRENCH MOS-GATED DEVICE AND PROCESS FOR FORMING SAME	US	09/283536	01-Apr-99		
SE-1416-PD	FAST TURN-OFF POWER SEMICONDUCTOR DEVICES	US	09/296472	22-Apr-99		
SE-1434-PD	POWER MOS DEVICE WITH INCREASED CHANNEL WIDTH AND PROCESS FOR FORMING SAME	US	09/303270	30-Apr-99		
SE-1387-PD	PROCESS FOR FORMING MOS-GATED DEVICES HAVING SELF-ALIGNED TRENCHES	US	09/307879	10-May-99		
SE-1512-PD	MOS-GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME	US	09/314323	19-May-99		
SE-1505-PD	TRENCH-GATED DEVICE HAVING TRENCH WALLS FORMED BY SELECTIVE EPITAXIAL GROWTH AND PROCESS FOR FORMING DEVICE	US	09/318334	25-May-99		
SE-1272-PD	SEMICONDUCTOR DEVICE GATE STRUCTURE FOR THERMAL OVERLOAD PROTECTION	US	09/338891	23-Jun-99		
SE-1491-PD	BACKMETAL DRAIN TERMINAL WITH LOW STRESS AND THERMAL RESISTANCE	US	09/339356	24-Jun-99		
SE-1395-PD	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A MULTIPLE PASS CONFIGURATION	US	09/344867	28-Jun-99		
SE-1517-PD	EDGE TERMINATION FOR SILICON POWER DEVICES	US	09/344868	28-Jun-99		
SE-1515-PD	POWER SEMICONDUCTOR MOUNTING PACKAGE CONTAINING BALL GRID ARRAY	US	09/345930	01-Jul-99		

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SE-1359-PD	PROCESS FOR FORMING VERTICAL SEMICONDUCTOR DEVICE HAVING INCREASED SOURCE CONTACT AREA	US	09/350575	09-Jul-99		
SE-1154-PD	DOUBLY GRADED JUNCTION TERMINATION EXTENSION (JTE) FOR EDGE PASSIVATION OF SEMICONDUCTOR DEVICES	US	09/358625	21-Jul-99		
SE-1465-PD	TECHNIQUE FOR MINIMIZING GATE CHARGE AND GATE TO DRAIN CAPACITANCE IN POWER MOS DEVICES SUCH AS DMOS, IGBTS AND MOSFETS	US	09/428616	27-Oct-99		
SE-1267-PD	METHOD OF MAKING A MOS-GATED SEMICONDUCTOR DEVICE WITH A SINGLE DIFFUSION	US	09/449487	29-Nov-99		
SE-1474-PD	EMITTER BALLAST RESISTOR WITH ENHANCED BODY EFFECT TO IMPROVE THE SHORT CIRCUIT WITHSTAND CAPABILITY OF POWER DEVICES	US	09/450872	29-Nov-99		
SE-1194-PD	A NOVEL TRENCH MOSFET PROCESS	US	09/498476	04-Feb-00		
SE-1556-PD	MOS-GATED DEVICE HAVING ALTERNATING ZONES OF CONDUCTIVITY	US	09/502712	11-Feb-00		
SE-1518-PD	POWER TRENCH TRANSISTOR DEVICE SOURCE REGION FORMATION USING SILICON SPACER	US	09/525182	14-Mar-00		
SE-1220-TD	METHOD FOR FABRICATING A POWER DEVICE	US	09/542561	04-Apr-00		
SE-1433-PD	SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS	US	09/551187	17-Apr-00		
SE-1190-PD	HIGH PERFORMANCE HEAT EXCHANGER AND METHOD	US	09/570009	12-May-00		
SE-1587-PD	SOFT RECOVERY POWER DIODE AND RELATED METHOD	US	09/603605	26-Jun-00		
SE-1522-PD	POWER MOS DEVICE WITH BURIED GATE	US	09/624533	24-Jul-00		
SE-1356-PD	HEAT EXCHANGING CHASSIS AND METHOD	US	09/649815	28-Aug-00		
SE-1356-PD	HEAT EXCHANGING CHASSIS AND METHOD	us	09/649837	28-Aug-00		
SE-1528-PD	POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY	US	09/654845	01-Sep-00		
SE-1395-PD	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A MULTIPLE PASS CONFIGURATION	US	09/663235	15-Sep-00		

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SE-1613-PD	INTEGRATED CIRCUIT DEVICE INCLUDING A DEEP WELL REGION AND ASSOCIATED METHODS	US	09/664024	19-Sep-00		
SE-1586-PD	SELF-ALIGNED PROCESS FOR FABRICATING POWER MOSFET WITH SPACER-SHAPED TERRACED GATE	US	09/665,850	20-Sep-00		
SE-1552-PD	MOS-GATED POWER DEVICE HAVING SEGMENTED TRENCH AND EXTENDED DOPING ZONE AND PROCESS FOR FORMING SAME	US	09/689939	12-Oct-00		
SE-1549-PD	PROCESS FOR CONTROLLING LIFETIME IN A P-I-N DIODE AND FOR FORMING DIODE WITH IMPROVED LIFETIME CONTROL	US	09/718219	21-Nov-00		
SE-1512-PD	MOS-GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME	US	09/726682	30-Nov-00		
SE-1434-PD	POWER MOS DEVICE WITH INCREASED CHANNEL WIDTH AND PROCESS FOR FORMING SAME	US	09/765177	18-Jan-01		
SE-1612-PD	QUASI-RESONANT CONVERTER	US	60/198692	20-Apr-00		
SE-1645-PD	A HIGHLY RUGGED DENSE TRENCH-GATED POWER MOSFET PRODUCED BY USING A FULLY SELF-ALIGNED BODY IMPLANT PROCESS	US	60/219858	20-Jul-00		
SE-1657-PD	CONTROLLING SILICON TRENCH PROFILES BY INCREMENTAL INCREASES IN OXYGEN FLOWS	US	60/234563	22-Sep-00		

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