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3-1	4-01				110
KUO-CHYUAN TZENG, TSE-LIANG Y	ING,	Name: Taiwa	n Semicon	ductor Manufact	ace 71
MIN-HSIUNG CHIANG, HSIAO-HUI T	-	Company			
CHUNG-WEI CHANG		i			
		Internal Addre	ess:		
Additional name(s) or conveying party(ies) attached	1? Yes X N	Þ			
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X Assignment Merger		City: Hsin-C		Zip:	
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Execution Date: 3/16/01			e(s) & addres	s(es) attached?	Yes X
4. Application number(s) or patent number	(a):	No			
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If this document is being filed together v	vith a new application	n, the execution d	ate of the a	pplication is: 3/16/0	<u>)1</u>
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ASSIGNMENT OF INVENTION  In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration,					
Kuo-Chyuan Tzeng Type or print name of ASSIGNOR	Tse-Liang Ying Type or print name of ASSIGNOR				
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Republic of China Nationality	Republic of China				
ASSIGNEE:					
Taiwan Semiconductor Manufacturing C 121 Park Ave. 3 Science-Based Industrial Park Hsin-Chu, Taiwan, R.O.C. Taiwan, R.O.C.	o. Ltd.				
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x the entire right, title and interest	, one of the following)				
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in and to any and all improvements which ar	e disclosed in the invention entitled:				
A Method For Improving Bit Line To Capa Etch-Back To Improve The Bit-Line-To-Ca	acitor Electrical Failures On DRAM Circuits Using A Wet				

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In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration,				
ASSIGNOR:				
Chung-Wei Chang Type or print name of ASSIGNOR  6F, No. 72-10, Lane 531,  Address Sec.   Knang-Fu Rd., Hsin-Chu  Republic of China  Nationality				
ASSIGNEE: Taiwan Semiconductor Manufacturing Co. Ltd.				
121 Park Ave. 3 Science-Based Industrial Park Hsin-Chu, Taiwan, R.O.C. Taiwan, R.O.C.  Nationality				
and the successors, assigns and legal representatives of the ASSIGNEE				
(complete one of the following)				
x the entire right, title and interest an undivided percent (%) interest for the United States and its territorial possessions (check the following box/f foreign rights are also to be assigned)  x and in all foreign countries				
in and to any and all improvements which are disclosed in the invention entitled:				
A Method For Improving Bit Line To Capacitor Electrical Failures On DRAM Circuits Using A Wet Etch-Back To Improve The Bit-Line-To-Capacitor Overlay Margins				

and which is found in					
(a) x U.S. patent application executed on even date herewith					
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IN WITNESS WHEREOF, I / We have signed this  Mar, 16, > >   (Dat	te of signing)				
WARNING Date of signing must be the same as the date of	execution of the application if item (a) was checked above.				
	Signature of Assignor(s)  The Diang Ying  Min - Haing Chiang  Haino - Hui Tang				
If ASSIGNOR is a legal entity complete the following information					
	Type or print the name of the above person authorized to sign on behalf of ASSIGNOR				
	Title				

Note: No witnessing, notarization or legalization is necessary, if the assignment is notarized or legalized then it will only be prima facie evidence (35 USC

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and which is found in	
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If ASSIGNOR is a legal entity complete the following information	rmation
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