11-21-2001

Form PTO-1595 (Rev. 03/01)
OMB No. 0651-0027 (exp. 5/31/2002)
Tab settings ⇨ ⇨ ⇨ ▼ ▼

RE(

101900052

U.S. DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

E.ON AG 11.21.01

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other Termination of security interest.

Execution Date: November 13, 2001

2. Name and address of receiving party(ies)

Name: MEMC Electronic Materials, Inc.

Internal Address: _____

Street Address: 501 Pearl Drive

City: St. Peters State: MO Zip: 63376

Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: _____

A. Patent Application No.(s)	B. Patent No.(s)
08/971,253	4,450,960

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Paul Shim

Internal Address: ~~Cleary, Gottlieb, Steen &~~ Hamilton

Street Address: One Liberty Plaza

City: New York State: N.Y. Zip: 10006

6. Total number of applications and patents involved: 256

7. Total fee (37 CFR 3.41).....$10,240.00

☒ Enclosed

☐ Authorized to be charged to deposit account

8. Deposit account number:

(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Name of Person Signing	Signature	Date
Brian Crist	Brian W. Crist	11/21/01

Total number of pages including cover sheet, attachments, and documents: 28

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

11/21/2001 6TDN11 00000033 08971253
01 FC:581 10240.00 DP

1

Additional Application Numbers and Patent Numbers for Item 4 on the Recordation Form Cover Sheet

Patent Application Numbers
08/971,253
08/991,799
09/082,906
09/270,366
09/332,745
09/344,003
09/344,036
09/344,709
09/352,980
09/366,850
09/370,349
09/372,897
09/379,383
09/385,108
09/416,998
09/419,151
09/430,654
09/438,551
09/475,320
09/481,080
09/489,481
09/495,563
09/502,340
09/503,566
09/505,269
09/506,105
09/507,811
09/521,288
09/521,525
09/535,759
09/543,192
09/543,194
09/566,890
09/568,356
09/568,751
09/596,493
09/607,389
09/607,391
09/608,302

Patent Numbers
4,450,960
4,608,096
4,622,082
4,666,532
5,668,330
4,851,358
4,868,133
5,178,720
5,288,366
5,340,437
5,373,807
5,376,890
5,377,451
5,408,951
5,417,767
5,422,316
5,439,523
5,445,679
5,488,924
5,516,730
5,518,549
5,550,374
5,571,373
5,573,680
5,578,284
5,582,642
5,588,993
5,592,295
5,593,494
5,593,498
5,593,505
5,605,487
5,622,568
5,626,159
5,628,823
5,632,666
5,653,799
5,656,078
5,665,159

Additional Application Numbers and Patent Numbers for Item 4 on the Recordation Form Cover Sheet

Patent Application Numbers	Patent Numbers
09/608,304	5,676,751
09/610,277	5,679,055
09/631,089	5,712,198
09/633,958	5,732,258
09/659,537	5,746,834
09/661,745	5,753,567
09/661,821	5,762,491
09/661,822	5,765,890
09/667,909	5,766,341
09/681,160	5,770,522
09/684,266	5,779,791
09/691,994	5,787,595
09/704,893	5,789,309
09/704,900	5,792,273
09/705,092	5,795,381
09/711,198	5,799,728
09/723,847	5,814,148
09/730,171	5,816,274
09/730,172	5,827,113
09/737,715	5,837,662
09/743,071	5,839,460
09/751,897	5,840,120
09/752,222	5,840,202
09/757,121	5,843,234
09/769,773	5,843,322
09/797,391	5,846,318
09/807,907	5,849,076
09/811,982	5,855,859
09/815,508	5,865,670
09/816,015	5,870,881
09/817,929	5,882,402
09/833,777	5,882,989
09/834,118	5,885,344
09/834,819	5,891,250
09/853,232	5,894,711
09/859,094	5,904,768
09/859,826	5,906,533
09/865,083	5,908,504
09/869,084	5,910,295
09/871,255	5,913,975
09/874,487	5,919,302

Additional Application Numbers and Patent Numbers for Item 4 on the Recordation Form Cover Sheet

Patent Application Numbers
09/892,002
09/896,945
09/928,559
09/929,585
09/970,404
09/972,608
09/682,677
60/245,610
60/249,854
60/252,715
60/226,783
60/257,646
60/258,296
60/258,414
60/259,000
60/259,362
60/264,415
60/273,980
60/280,035
60/280,680
60/283,103
60/285,180
60/300,208
60/300,364
60/301,767
60/302,907
60/308,521
60/309,645
60/312,573
60/315,846
60/325,622
60/325,660

Patent Numbers
5,919,303
5,919,311
5,922,127
5,935,328
5,942,032
5,964,953
5,968,263
5,974,680
5,975,998
5,990,014
6,006,736
6,006,738
6,015,335
6,019,838
6,026,963
6,030,887
6,039,801
6,039,807
6,053,974
6,057,170
6,086,678
6,089,285
6,093,913
6,100,167
6,112,738
6,114,245
6,120,350
6,129,048
6,135,863
6,164,299
6,168,961
6,171,391
6,177,279
6,179,950
6,180,220
6,183,553
6,187,089
6,189,546
6,190,631
6,191,010
6,197,111

Additional Application Numbers and Patent Numbers for Item 4 on the Recordation Form Cover Sheet

Patent Application Numbers

Patent Numbers
6,200,908
6,203,611
6,203,614
6,210,640
6,214,109
6,214,704
6,227,944
6,230,720
6,231,628
6,236,104
6,238,483
6,241,818
6,254,672
6,257,954
6,284,039
6,284,040
6,284,384
6,285,011
6,287,380
6,287,382
6,293,139

TERMINATION AGREEMENT

This TERMINATION AGREEMENT dated as of November 13, 2001, is made by MEMC Electronic Materials, Inc., a Delaware corporation ("MEMC") with principal offices at 501 Pearl Drive, St. Peters, Missouri, USA 63376 and E.ON AG ("E.ON"), with principal offices at E.ON - Platz 1, D-40479 Düsseldorf, Germany.

RECITALS

WHEREAS, in the Assignment of Security Interest in United States Patents between MEMC and E.ON, dated October 25, 2001 ("Patent Assignment), MEMC assigned and granted to E.ON, as Agent (as that term is defined in the Second Amended and Restated Security Agreement among MEMC, MEMC Pasadena, Inc. ("MEMC Pasadena") and E.ON, dated as of October 25, 2001 (as amended from time to time, the "Security Agreement"), a security interest in certain assets of MEMC, including without limitation, all of the MEMC's right, title and interest in and to the United States patents and patent applications set forth on Schedule A attached hereto, all patent applications of MEMC filed after October 23, 2001, all patents issuing from any of the foregoing, and any and all reissues, reexaminations, divisionals, continuations, continuations-in-part and extensions in all or in part of any of the foregoing (collectively, the "Patents") as set forth in greater detail in the Patent Assignment; and

WHEREAS, E.ON, as Agent, MEMC and MEMC Pasadena have agreed to terminate the Security Agreement and desire to terminate the Patent Assignment in connection with the Revolving Credit Agreement dated as of November 13, 2001 (the "Revolving Credit Agreement") among MEMC Electronic Materials, Inc., the Lenders (as defined therein) party thereto, Citicorp USA, Inc., as Administrative Agent (as defined therein) and Citicorp USA, Inc., as Collateral Agent (as defined therein), together with the Security Documents (as defined therein) attached as Exhibits to such Revolving Credit Agreement and (ii) the Indenture dated as of November 13, 2001 (the "Indenture"), among MEMC Electronic Materials, Inc., Citibank N.A., a national banking association, as Trustee (as defined therein) and Citicorp USA, Inc., as Collateral Agent (as defined therein), together with the Security Documents (as defined therein) attached as Exhibits to such Indenture; in each case, as such agreements and documents may be amended, supplemented or modified from time to time, E.ON desires to terminate the Patent Assignment.

NOW, THEREFORE, in consideration of good and valuable consideration the sufficiency of which is hereby acknowledged, the parties hereto agree as follows:

1. In conjunction with termination of the Security Agreement in accordance with Section 7.8 of the Security Agreement E.ON, as Agent, hereby terminates the Patent Assignment.

2. E.ON, as Agent, hereby (i) releases and forever waives all of its right, title and interest which E.ON, as Agent, has or may be entitled to by virtue of the Patent Assignment in and to all of the property, interests and rights covered thereby, including without limitation, the Patents (as set forth on Schedule A) encumbered thereby; and (ii) terminates the Patent Assignment and any and all security interests created therein.

3. E.ON, as Agent, makes no warranty of any kind, express or implied, including, without limitation, any warranty with respect to the Patents, except that E.ON, as Agent, warrants that all the interests terminated, released and discharged are free and clear of all liens, security interests, encumbrances, assignments, transfers and claims arising by, through or under E.ON, as Agent, but not otherwise.

4. E.ON, as Agent, hereby further states, affirms and declares that it no longer claims a lien on, security interest in or assignment of any of the property, interests and rights covered by the Patent Assignment. E.ON, as Agent, agrees to execute, acknowledge and deliver, or cause to be executed, acknowledged and delivered, such further instruments and take such further action as may be necessary or appropriate to terminate, release and discharge all liens, security interests, assignments and other encumbrances and interests granted or created by the Patent Assignment.

5. This Termination Agreement shall be binding on E.ON, as Agent, and shall inure to the benefit of MEMC and MEMC Pasadena, and their respective successors and assigns.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

MEMC ELECTRONIC MATERIALS, INC.

By _____
Name: James M. Stolze
Title: Executive Vice President,
Chief Financial Officer

By _____
Name: Kenneth L. Young
Title: Treasurer

E.ON AG, as Agent

By: _____
Name: Joseph Supp
Title: Attorney-in-Fact

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

MEMC ELECTRONIC MATERIALS, INC.

By _____
Name: James M. Stolze
Title: Executive Vice President,
Chief Financial Officer

By _____
Name: Kenneth L. Young
Title: Treasurer

E.ON AG, as Agent

By: _____
Name: Joseph Stipp
Title: Attorney-in-Fact

US PATENTS

SCHEDULE A

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
4,450,960	05/29/84	2002	89-8337	Johnson	Package
4,608,096	08/26/86	2003	89-8341/5307	Hill	Gettering
4,622,082	11/11/86	2004	89-8326	Dyson & Rossi	Conditioned Semiconductor Substrates
4,666,532	05/19/87	2004	89-8307	Korb, Reed & Shaw	Denuding Silicon Substrates with Oxygen and Halogen
4,668,330	05/26/87	2005	89-8348	Golden	Furnace Contamination
4,851,358	07/25/89	2008	89-12175-1-1	Huber	Semiconductor Wafer Fabrication with Improved Control of Internal Gettering Sites Using Rapid Thermal Annealing
4,868,133	09/19/89	2008	89-12175-1	Huber	Semiconductor Wafer Fabrication with Improved Control of Internal Gettering Sites Using RTA
5,178,720	01/12/93	2011	91-0100	Frederick	Method for Controlling Oxygen Content of Silicon Crystals Using a Combination Cusp Magnetic Field and Crystal and Crucible Rotation
5,288,366	02/22/94	2012	91-0950	Holder	Method for Growing Multiple Single Crystals And Apparatus For Use Therein
5,340,437	08/23/94	2013	93-0500	Erk & Vandamme	Process and Apparatus for Etching Semiconductor Wafers
5,373,807	12/20/94	2012	93-1050	Holder	Method for Growing Multiple Single Crystals and Apparatus Fo Use Therein
5,376,890	12/27/94	2013	93-0450	Keevil, Burgdorf, Ketterer & Wood	Capacitive Distance Measuring Apparatus Having Liquid Ground Contact
5,377,451	01/03/95	2013	92-0600	Leoni, Morganti & Vesco	Wafer Polishing Apparatus and Method
5,408,951	04/25/95	2013	94-1050	Tamida	Improved Method for Growing Silicon Crystal
5,417,767	05/23/95	2013	93-0550	Stinson	Wafer Carrier

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
5,422,316	06/06/95	2014	93-0900	Desai, Wisnieski & Golland	Semiconductor Wafer Polisher and Method
5,439,523	08/08/95	2014	93-0600	Yamaguchi	Device for Suppressing Particle Splash Onto a Semiconductor Wafer
5,445,679	08/29/95	2012	92-0650	Hansen & Banan	Plasma Cleaning of Polysilicon for Charging into a Czochralski Crystal Growing Process
5,488,924	02/06/96	2013	93-0750	Horvath, Jones & Polett	Hopper and Method For Use in Charging Semi-Conductor Source Material
5,516,730	05/14/96	2014	94-0700	Shive, Pirooz	Pre-thermal Treatment Cleaning Process
5,518,549	05/21/96	2015	94-1450	Lance Hellwig	Susceptor and Baffle Therefor
5,550,374	08/27/96	2014	94-0150	Holzer & Drescher	Method and Apparatus for Determining Interstitial Oxygen Content of Relatively Large Diameter Silicon Crystals by Infrared Spectroscopy
5,571,373	11/05/96	2014	93-0700	Krishna, Wisnieski, Illig	Method of Rough Polishing Semiconductor Wafers to Reduce Roughness
5,573,680	11/12/96	2014	94-0300	R. Shaw, J. Holzer	Apparatus and Method for Etching a Semiconductor Material Without Altering Flow Pattern Defect Distribution
5,578,284	11/26/96	2015	94-0600	Chandrasekhar & Kim	Process for Eliminating Dislocations in the Neck of a Silicon Single Crystal
5,582,642	12/10/96	2015	94-1900	Korb, Williams, Schrenker, Lauher	Apparatus and Method for Adjusting The Position of a Pull Wire of A Crystal Pulling Machine
5,588,993	12/31/96	2015	94-1650	Holder	Method for Preparing Molten Silicon Melt From Polycrystalline Silicon Charge
5,592,295	01/07/97	2015	94-1600	Stanton, Krause	Apparatus and Method for Semiconductor Wafer Edge Inspection

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
5,593,494	01/14/97	2015	94-1700	Robert Falster	Precision Controlled Precipitation of Oxygen in Silicon
5,593,498	01/14/97	2015	95-0800	Kimbel, Korb & Hall	Apparatus and Method for Rotating a Crucible of a Crystal Pulling Machine
5,593,505	01/14/97	2015	94-0900 & Chai	Erk, Bartram, Hollander	Apparatus and Method for Cleaning Semiconductor Wafers
5,605,487	02/25/97	2014	93-1400	Hileman, Walsh & Walsh	Semiconductor Wafer Polishing Apparatus and Method
5,622,568	04/22/97	2014	93-1000	Shive, Pirooz	Gettering of Metals from Solution
5,626,159	05/06/97	2015	96-1500	Erk, Bartram, Hollander & Chai	Apparatus and Method for Cleaning Semiconductor Wafers
5,628,823	05/13/97	2015	96-1150	Chandrasekhar & Kim	A Silicon Single Crystal Having liminated Dislocation in its Neck Crystal
5,632,666	05/27/97	2014	94-0550	Peratello, Leoni	Method and Apparatus for Automated Quality Control in Wafer Slicing
5,653,799	08/05/97	2015	94-1250	Robert Fuerhoff	System and Method for Controlling Growth of a Silicon Crystal
5,656,078	08/12/97	2015	94-1300	Fuerhoff	Non-Distorting Video Camera for Use With A System For Controlling Growth of a Silicon Crystal
5,665,159	09/09/97	2015	96-0300	Fuerhoff	System and Method for Controlling Growth of a Silicon Crystal
5,676,751	10/14/97	2016	94-1750	Banan, Korb & Kim	Rapid Cooling of CZ Silicon Crystal Growth System
5,679,055	10/21/97	2016	95-1900	Greene, Albrecht, Strittmatter & Hidalgo	Automated Wafer Lapping System
5,712,198	01/27/98	2014	95-2150	Pirooz, Shive	Pre-Heat Treatment Cleaning Process
5,735,258[5]	04/07/98	2016	95-2450	Okuno, Itoh & Horri	Cutting Maching WP01823
5,746,834	05/05/98	2016	95-1850	Hanley	Method and Apparatus for Purging Barrel Reactors

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
5,753,567	05/19/98	2012	94-0400	Hansen, Banan	Cleaning of Metallic Contaminants From the Surface of Polycrystalline Silicon
5,762,491	06/09/98	2015	95-0750	Williams, Luter	Solid Material Delivery System for a Furnace
5,765,890	06/16/98	2016	95-2400	Gaylord, Taylor	Device for Transferring a Semiconductor Wafer
5,766,341	06/16/98	2015	95-0800(DIV)	Kimble, Korb & Hall	Method for Rotating A Crucible of a Crystal Pulling Machine
5,770,522	06/23/98	2016	96-0200	Bronson	Polishing Block Heater
5,779,791	07/14/98	2016	95-2050	Korb, Falster, Holzer, Chandrasekhar, Ilic, Kim, Kimbel & Drafall	Process for Controlling Thermal History of Czochralski Grown Silicon
5,787,595	08/04/98	2016	95-1050	Desai, Adcock, Hall & Wisnieski	Method and Apparatus for Controlling Flatness of Polished Semiconductor Wafer
5,789,309	08/04/98	2016	96-0450	Hellwig	Method and System for Monocrystalline Epitaxial Deposition
5,792,273	08/11/98	2017	96-3100	Ries, Hellwig & Rossi	Secondary Edge Reflector for Horizontal Reactor
5,795,381	08/18/98	2016	95-0150	Holder	SiO Probe for Real-Time Monitoring and Control of Oxygen During Czochralski Growth of Single Crystal Silicon
5,799,728	09/01/98	2016	95-1450	Blume	Dehumidifier
5,814,148	09/29/98	2016	95-1950	Kim, Allen	Method for Preparing Molten Silicon Melt from Polycrystalline Silicon Charge
5,816,274	10/06/98	2017	96-1650	Bartram, Hollander	Apparatus for Cleaning Semiconductor Wafers
5,827,113	10/27/98	2016	95-2500 WP01824	Okuno, Itoh, Horii	Cutting Machine
5,837,662	11/17/98	2017	97-1000	Chai, Erk, Schmidt & Doane	Post-Lapping Cleaning Process for Silicon Wafers
5,839,460	11/24/98	2017	96-2250	Chai, Watson	Apparatus for Cleaning Semiconductor Wafers
5,840,120	11/24/98	2016	94-0750	Kim, Shaw, Schrenker	Apparatus and Method for Controlling Nucleation of Oxygen

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
5,840,202	11/24/98	2016	95-1750	& Chandrasekhar Walsh	Precipitates in Silicon Crystals Apparatus and Method for Shaping Polishing Pads
5,843,234	12/01/98	2016	95-1650	Finn, Hellwig	Method and Apparatus for Aiming A Barrel Reactor Nozzle
5,843,322	12/01/98	2016	96-1952	Chandler, Jr.	Process for Etching N, P, N+ and P+ Type Slugs and Wafers
5,846,318	12/08/98	2016	96-0250	Javidi	Method and System for Controlling Growth of a Silicon Crystal
5,849,076	12/15/98	2016	95-2300	Gaylord, Mueller	Cooling System and Method for Epitaxial Barrel Reactor
5,855,859	01/05/99	2014	93-1000(CIP)	Shive, Pirooz	Gettering Agent
5,865,670	02/02/99	2017	97-0350	Frank, Durkee, Bronson & Heim	Wafer Demount Apparatus
5,870,881	02/16/99	2017	96-2750	Rice, Suddarth, Edwards & Roberts	Box Closing Apparatus
5,882,402	03/16/99	2017	97-1650	Fuerhoff	Method and System for Controlling Growth of a Silicon Crystal
5,882,989	03/16/99	2017	94-0450	Falster	Process for the Preparation of Silicon Wafers Having a Controlled Distribution of Oxygen Precipitate Nucleation Centers
5,885,344	03/23/99	2017	96-0100	Kim, Chandrasekhar	Method and Apparatus for Non-Dash Neck Process for Single Crystal Silicon Growth
5,891,250	04/06/99	2018	97-2150	Lottes, Torack	Injector for Reactor
5,894,711	04/20/99	2017	97-0850	Davidson, Lunday, Lenk, Hampton, Anderson & Shive	Box Handling Apparatus and Method
5,904,768	05/18/99	2016	95-0100	Holder	Process and Apparatus for Controlling The Oxygen Content in Silicon Wafers Heavily Doped with Antimony or Arsenic
5,906,533	05/25/99	2016	95-0650/CONT	Harris, Hall	Radiant Polishing Block Heater

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
5,908,504	06/01/99	2015	95-0950	Hanley	Method for Tuning Barrel Reactor Purge System
5,910,295	06/08/99	2017	96-0350	DeLuca	Closed Loop Process for Producing Polycrystalline Silicon and Fumed Silica
5,913,975	06/22/99	2018	97-2900	Holder	Crucible and Method of Preparation Thereof
5,919,302	07/06/99	2017	98-0950	Falster, Holzer, Mutti, Markgraf, McQuaid, Johnson	Low Defect Density, Vacancy Dominated Silicon
5,919,303	07/06/99	2017	97-1050	Holder	Process for Preparing A Silicon Melt From a Polysilicon Charge
5,919,311	07/06/99	2016	94-0950	Shive, Malik	Control of SiO_2 Etch Rate Using Dilute Chemical Etchants in the Presence of A Megasonic Field
5,922,127	07/13/99	2017	97-1200	Luter, Ferry	Heat Shield For Crystal Puller
5,935,328	08/10/99	2017	96-0600	Cherko, Korb, Schrenker, Williams	Apparatus for Use in Crystal Pulling
5,942,032	08/24/99	2017	96-2200	Kim, Luter, Ferry, Braun, Ilic, Dioda, Tosi, Gobbo & Martini	Heat Shield Assembly and Method of Growing Vacancy Rich Single Crystal Silicon
5,964,953	10/12/99	2018	97-0200	Mettifogo	Post-Etching Alkaline Treatment Process
5,968,263	10/19/99	2018	96-1600	Grover & Kimbel	Open-Loop Method and System for Controlling Growth of Semiconductor Wafer
5,974,680	11/02/99	2016	93-0200(FWC)	Anderson & Wilson	Apparatus for Use in Cleaning Wafers
5,975,998	11/02/99	2017	97-0700	Olmstead	Wafer Processing Apparatus
5,990,014	11/23/99	2018	96-2300	Wilson, Lottes	In-Situ Wafer Cleaning Process
6,006,736 WPO1822	12/28/99	2016	95-2550	Suzuki, Kato, Takami Kawamura, Watanabe	Method for Washing Worked Silicon Ingot

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S & Kosako	TITLE
6,006,738	12/28/99	2017	96-1550 WP2130M004	Itoh & Tanaka	Method and Apparatus for Cutting an Ingot
6,015,335	01/18/00	2017	97-0100	Roberts	Apparatus for Dressing Inside Diameter Saws
6,019,838	02/01/00	2018	96-1700	Canella	Crystal Growing Apparatus with Melt-Doping Facility
6,026,963	02/22/00	2016	95-0550	Gray, Cooke	Moisture Barrier Bag Having Window
6,030,887	02/29/00	2017	97-0600	Desai, Vadnais & Standley	Flattening Process for Epitaxial Semiconductor Wafer
6,039,801	03/21/00	2018	98-0900	Holder, Johnson	Continuous Oxidation Process for Crystal Pulling Apparatus
6,039,807	03/21/00	2018	96-2900	Guarniero, Magon & Bonanno	Apparatus for Moving Exhaust Tube of Barrel Reactor
6,053,974	04/25/00	2017	97-1200(DIV)	Luter & Ferry	Heat Shield For Crystal Puller
6,057,170	05/02/00	2019	98-3900	Witte	Method and System of Measuring Waviness in Silicon Wafers
6,086,678	07/11/00	2019	98-0500	Wilson, Ries & Torack	Pressure Equalization System for Chemical Vapor Deposition Reactors
6,089,285	07/18/00	2018	97-1750	DeStefano, Eoff, Schulte, Anderson, Yau, Ruggeri, Baldwin, Badino	Method and System for Supplying Semiconductor Source Material
6,093,913	7/25/00	2018	97-0800	Schrenker & Luter	Electrical Resistance Heater for Crystal Growing Apparatus
6,100,167	08/08/00	2018	92-0350	Falster, Leoni, Bricchetti & Corradi	Process for the Removal of Copper From Polished Boron Doped Silicon Wafers
6,112,738	09/05/00	2019	98-3600	Witte, Ragan	Method of Slicing Silicon Wafers for Laser Marking
6,114,245	09/05/00	2017	96-2850(CONT)	Vandamme, Xin & Pei	Method of Processing Semiconductor Wafers

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
6,120,350	09/19/00	2019	98-5450	Zhou & Davis	Apparatus and Process for Reconditioning Polishing Pads
6,129,048	10/10/00	2018	97-2950	Sullivan	Improved Susceptor for Barrel Reactor
6,135,863	10/24/00	2019	98-3950	Zhang, Vogelgesang & Erk	Method of Conditioning Wafer Polishing Pads
6,164,299	12/26/00	2018	97-3000(DIV)	Sun & Adams	Ion Extraction Process for Single Side Wafers
6,168,961	01/02/01	2018	96-2050	Vaccari	Process for the Preparation of Epitaxial Wafers for Resistivity Measurements
6,171,391	01/09/01	2018	98-0450	Fuerhoff & Banan	Method and System for Controlling Growth of a Silicon Crystal
6,177,279	01/23/01	2018	97-3000	Sun & Adams	Ion Extraction Process and Apparatus for Single Side Wafers
6,179,950	01/30/01	2019	98-2000	Zhang, Vogelgesang, Potts & Erk	Polishing Pad and Process for Forming Same
6,180,220	01/30/01	2017	95-2350(CIP)	Falster, Cornara, Gambaro & Olmo	Ideal Oxygen Precipitating Silicon Wafers and Oxygen Out-Diffusion-Less Process Therefor
6,183,553	02/06/01	2018	97-1950	Holder, Joslin & Korb	Process and Apparatus for Preparation of Silicon Crystals with Reduced Metal Content
6,187,089	02/13/01	2019	97-3500	Phillips & Keltner	Tungsten Doped Crucible and Method for Preparing Same
6,189,546	02/20/01	2019	99-0450	Zhang, Brumer, Erk	Polishing Process for Manufacturing Dopant-Striation-Free Polished Silicon Wafers
6,190,631	02/20/01	2018	97-2700	Falster, Holzer, Cornara Gambaro, Olmo, Markgraf, Mutti, McQuaid & Johnson	Low Defect Density, Ideal Oxygen Precipitating Silicon
6,191,010	02/20/01	2019	98-3700	Falster	Ideal Oxygen Precipitating Silicon Wafers and Oxygen Out-Diffusion-Less Process Therefor

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
6,197,111	03/06/01	2019	98-4600	Ferry & Ishii	Heat Shield Assembly for Crystal Puller
6,200,908	03/13/01	2019	97-2550	Vandamme, Desai, Witte, & Xin	Process for Reducing Waviness in Semiconductor Wafers
6,203,611	03/20/01	2019	99-2450	Kimbel & Wyand, III	Method of Controlling Growth of a Semiconductor Crystal to Automatically Transition From Taper Growth to Target Diameter Growth
6,203,614	03/20/01	2019	98-5000	Cherko	Cable Assembly for Crystal Puller
6,210,640	04/03/01	2018	97-1150	Ruth & Schmidt	Collector for an Automated On-Line Bath Analysis System
6,214,109	04/10/01	2016	95-0100(DIV)	Holder	Apparatus for Controlling The Oxygen Content in Silicon Wafers Heavily Doped with Antimony or Arsenic
6,214,704	04/10/01	2019	98-1050	Xin	Method of Processing Semiconductor Wafers to Build in a Back Surface Damage
6,227,944	05/08/01	2019	98-1650	Xin, Yoshimura, Erk Vogelgesang & Hensiek	Method and Pressure Jetting Machine for Processing A Semiconductor Wafer
6,230,720	05/15/01	2020	99-0551	Yalamanchi, Myli & Shive	A Single-Operation Method of Cleaning Semi-Conductors After Final Polishing
6,231,628	05/15/01	2018	98-2200	Zavattari & Fragiacomo	System to Separate, Regenerate and Reuse Exhausted Glycol Based Slurry
6,236,104	05/22/01	2019	98-3050	Falster	Silicon on Insulator Structure From Low Defect Density Single Crystal Silicon
6,238,483	05/29/01	2019	99-0100	Cherko	Apparatus for Supporting A Semiconductor Ingot During Growth
6,241,818	06/05/01	2019	98-5850	Kimbel & Wyand III	Method and System of Controlling Taper in a Semiconductor Crystal Growth Process
6,254,672	07/03/01	2018	96-0050(CIP)	Flaster, Holzer, Markgraf, Mutti, McQuaid & Johnson	Low Defect Density Self-Interstitial Dominated Silicon

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
6,257,954	07/10/01	2020	99-2300	Ng, Walsh, Erk & Buese	Apparatus and Process for High Temperature Wafer Edge Polishing
6,284,039	09/04/01	2019	98-0700	Mule'Stagno, Fei Holzer, Korb & Falster	Epitaxial Silicon Wafers Substantially Free of Grown-In Defects
6,284,040	09/04/01	2019	98-1400	Holder & Sreedharamurthy	Process of Stacking and Melting Polycrystalline Silicon For High Quality Single Crystal Production
6,284,384	09/04/01	2019	98-3750	Wilson, Rossi & Yang	An Epitaxial Silicon Wafer with Intrinsic Gettering and a Method for the Preparation Thereof
6,285,011	09/04/01	2019	99-0600	Cherko	Electrical Resistance Heater for Crystal Growing Apparatus
6,287,380	09/11/01	2018	96-0050	Falster & Holzer	Low Defect Density Single Crystal Silicon
6,287,382	09/11/01	2018	97-2250	Cherko	Electrode Assembly for Electrical Resistance Heater Used in Crystal Growing Apparatus
6,293,139	09/25/01	2019	99-2100	Keller, & Whitman, Jr.	Method of Determining Performance Characteristics of Polishing Pads
08/971,253*		PEND	94-0200(FWC)	Shive, Pirooz	Cleaning Process for Hydrophobic Silicon Wafers
08/991,799*		PEND	96-0950	Davis & Smith	Process for the Control of NO_x Generated by Etching of Semiconductor Wafers
09/082,906*		PEND.	96-2700	Shive & Vitus	Process for the Removal of Copper and Other Metallic Impurities From Silicon
09/270,366*		PEND.	98-0950(CIP)	Falster, Holzer, Markgraf, Mutti, McQuaid & Johnson	Vacancy Dominated, Defect-Free Silicon
09/332,745*		PEND.	98-4200	Yang & Watkins	A Method for the Preparation of an Epitaxial Silicon Wafer With Intrinsic Gettering
09/344,003*		PEND.	98-2900	Schrenker & Luter	Crystal Puller for Growing Low Defect Density, Self-Interstitial Dominated Silicon

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/344,036*		PEND.	98-4900	Falster, Voronkov & Mutti	Process for Preparing Defect Free Silicon Crystals Which Allows for Variability in Process Conditions
09/344,709*		PEND.	98-4350	Falster, Korb	Process for Growth of Defect Free Silicon Crystals of Arbitrarily Large Diameters at Arbitrary Growth Rates Maximum Throughput
09/352,980*		PEND.	98-1950	Anderson	Process for Fabricating Semiconductor Wafers With External Gettering
09/366,850*		PEND.	98-0410	Falster	Non-Uniform Minority Carrier Lifetime Distributions in High Performance Silicon Power Devices
09/370,349*		PEND.	96-1600(DIV)	Grover & Kimbel	Open Loop Apparatus for Controlling Crystal Growth
09/372,897*		PEND	98-4450	Wyand, Fuerhoff & Johnson	Apparatus for Accurately Pulling a Crystal and Lifting a Crucible
09/379,383*		PEND.	98-3100	Falster	Non-Oxygen Precipitating Czochralski Silicon Wafers
09/385,108*		PEND.	98-1500	Falster, Binns & Korb	Thermally Annealed Wafers Having Improved Internal Gettering
09/416,998*		PEND	98-1450	Falster, Binns & Wang	Thermally Annealed, Low Defect Density Single Crystal Silicon
09/419,151*		PEND.	98-1350	Holder, Joslin, Sreedharamurthy & Lhamon	Method and System for Measuring Polycrystalline Chunk Size and Distribution in the Charge of a Czochralski Process
09/430,654*		PEND.	98-5900	Schmidt, Seilkop & Spohr	Apparatus for Cleaning Semiconductor Wafers
09/438,551*		PEND.	98-1250	Stefanescu & Erk	Etching Solution and Process for Etching Semiconductor Wafers
09/475,320*		PEND.	96-0050(DIV)	Falster, Holzer, Markgraf Mutti, McQuaid & Johnson	Low Defect Density Self-Interstitial Dominated Silicon
09/481,080*		PEND.	99-1550	Vasat, Stefanescu, & Hanley	Semiconductor Wafer Manufacturing Process
09/489,481*		PEND.	98-0900(CONT)	Holder & Johnson	Continuous Oxidation Process for Crystal Pulling Apparatus

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/495,563*		PEND.	98-5750	Mutti & Voronkov	Method for Controlling Growth of a Silicon Crystal to Minimize Growth Rate and Diameter Deviations
09/502,340*		PEND.	99-0900	Fuerhoff & Kimbel	Method and System for Controlling Diameter of a Silicon Crystal in a Locked Seed Lift Growth Process
09/503,566*		PEND.	00-0050	Holder	Process for Producing A Silicon Melt
09/505,269*		PEND.	99-3350	Ng, Xin, Erk, Harris, Jose, Hensiek, Hollander Buese & Negri	Process for Reducing Surface Variations for Polished Wafer
09/506,105*		PEND.	99-2150	Zhang, Ng & Erk	Semiconductor Wafer Manufacturing Process
09/507,811*		PEND.	99-1150	Ng & Teasley	Method for Wafer Processing
09/521,288*		PEND.	99-0052	Phillips, Keltner, Holder & Drafall	Barium Doping of Molten Silicon for Use in Crystal Growing Process
09/521,525*		PEND.	99-0051	Phillips, Keltner, Holder & Drafall	Doping of Molten Silicon For Use in Crystal Growing Process Strontium Doping of Molten Silicon for Use in Crystal Growing Process
09/535,759*		PEND.	98-1650(DIV)	Xin, Yoshimura, Erk Vogelgesang & Hensiek	Pressure Jetting Machine for Processing a Semiconductor Wafer
09/543,192*		PEND.	98-1800	Stefanescu, Pei, Erk & Doane	Method for the Detection of Processing-Induced Defects in a Silicon Wafer
09/543,194*		PEND.	97-3250	Erk, Stefanescu, Doane & Schmidt	Process for Etching a Silicon Wafer
09/566,890*		PEND.	99-3550	Yang, Standley	Modified Susceptor for Use in Chemical Vapor Deposition Process
09/568,356*		PEND.	99-2200	Cherko, Banan, Kulkarni	Method and Device for Feeding Arsenic Dopant into A Silicon Crystal Growing Process

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/568,751*		PEND.	99-2400	Banan, Kulkarni, Whitmer II	A Multi-Stage Arsenic Doping Process to Achieve Low Resistivity in Silicon Crystal Grown by Czochralski Method
09/596,493*		PEND.	98-2150	Kojima & Ishii	Process for Preparing Single Crystal Silicon Having Uniform Thermal History
09/607,389*		PEND.	98-4700	Torack, Ries	A Method and Apparatus for Forming an Epitaxial Silicon Wafer with a Denuded Zone
09/607,391*		PEND.	98-4250	Yang	A Method and Apparatus for Forming A Silicon Wafer with a Denuded Zone
09/608,302*		PEND.	98-4650	Wilson, Ries	Method and Apparatus for Forming a Silicon Wafer with a Denuded Zone
09/608,304*		PEND.	99-2250	Williams, Andrus, Kulage, Harrell	Non-Contaminating Gas-Tight Valve for Semiconductor Applications
09/610,277*		PEND.	98-3650	Basic & Illig	Polishing Mixture and Process for Reducing Incorporation of Copper Into Silicon Wafers
09/631,089*		PEND.	99-2850	Lu, Frank, Edwards	Method of Polishing a Semiconductor Wafer
09/633,532*		PEND.	00-2350	Zhang, Erk, Ragan, Kearns	Method for Processing a Semiconductor Wafer Using Double-Side Polishing
09/633,958*		PEND.	99-3650	Zhang, Xin, Erk	Method and Apparatus for a Wafer Carrier Having an Insert
09/659,537*		PEND.	97-1951	Holder, Joslin & Korb	Process and Apparatus for Preparation of Silicon Crystals With Reduced Metal Content
09/661,745*		PEND.	99-1750	McCallum, Alexander, Banan, Falster, Holzer, Johnson, Kim, Kimbel, Lu, Mutti, Voronkov, Mule'Stagno, & Libbert	Process for Suppressing the Nucleation and/or Growth of Interstitial Type Defects by Controlling the Cooling Rate Through Nucleation

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/661,821*		PEND.	99-1650	Mule'Stagno, Libbert & Holzer	Method for Producing Czochralski Silicon Free of Agglomerated Self-Intersitital Defects
09/661,822*		PEND.	99-1600	Mule'Stagno & Falster	Process for Detecting Agglomerated Intrinsic Point Defects by Metal Decoration
09/667,909*		PEND.	97-3351	Mabry & Rhodes	Radio Frequency Identification System and Method for Tracking Silicon Wafers
09/681,160*		PEND.	00-2150	Anderson, Schmidt, Teasley, Buese & Callahan	Method and Apparatus to Place Wafers Into and Out of Machine
09/684,266*		PEND.	00-0100	Ferry, Kimbel, McCAllum & Schrenker	Heat Shield Assembly for Crystal Pulling Apparatus
09/691,994*		PEND.	97-0451	Schrenker & Luter	Electrical Resistance Heater and Method for Crystal Growing Apparatus
09/704,893*		PEND.	95-2352	Falster, Cornara, Gambaro & Olmo	Ideal Oxygen Precipitating Epitaxial Silicon Wafers and Oxygen Out-Diffusion-Less Process Therefor
09/704,900*		PEND.	98-3701	Falster	Ideal Oxygen Precipitating Silicon Wafers and Oxygen Out-Diffusion-Less Process Therefor
09/705,092*		PEND.	97-2701	Falster, Holzer, Cornara, Gambaro, Olmo, Markgraf Mutti, McQuaid & Johnson	Low Defect Density, Ideal Oxygen Precipitating Silicon
09/711,198*		PEND.	98-5800	Fuerhoff, Banan, Holder	Method and Apparatus for Preparing Molten Silicon Melt From Polycrystalline Silicon Charge
09/723,847*		PEND.	99-3600	Ruprecht	Defect Classification Using Scattered Light Intensities at Various Angels
09/730,171*		PEND.	97-1151	Ruth & Schmidt	Process for Collecting and Analyzing the Content of a Liquid in an Automated On-line Bath Analysis System

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/730,172*		PEND.	97-1152	Ruth & Schmidt	Process for Collecting and Analyzing the Content of a Liquid in an Automated On-line Bath Analysis System
09/737,715*		PEND.	98-3051	Falster	Silicon on Insulator Structure From Low Defect Density Single Crystal Silicon
09/743,071		PEND.	98-4050 WP2461M022	Tomizawa, Kuroda & Nakamura	Process for Mapping Metal Contaminant Concentration on a Silicon Wafer Surface
09/751,897*		PEND.	00-0900	Ries	Semiconductor Wafer Holder
09/752,222*		PEND.	99-3850	Ries, Yang & Standley	An Epitaxial Silicon Wafer Free From Autodoping and Backside Halo and A Method and Apparatus for the Preparation Thereof
09/757,121*		PEND.	99-3950	Sreedharamurthy Banan, Holder & Ferry	Crystal Puller and Method for Growing Single Crystal Semiconductor Material
09/769,773*		PEND.	00-0400	Stefanescu, Brangenberg & Duly	Method and Apparatus for Reconditioning A Shipping Container
09/797,391*		PEND.	00-0700	Keller	Statistical Control Method for Proportions with Small Sample Sizes
09/807,907		PEND.	98-5250 WP2589M028	Iwamoto & Kurokawa	A Carrier for Cleaning a Silicon Wafer
09/811,982*		PEND.	00-3400	Phillips, Drafall, & McCallum	Crystal Puller and Method for Growing Monocrystalline Silicon Ingots
09/815,508*		PEND.	99-2250	Ferry, Schrenker & Banan	Heat Shield Assembly for Crystal Puller
09/816,015		PEND.	96-0052	Flaster, Holzer, Markgraf, Mutti, McQuaid & Johnson	Process for Producing Low Defect Density, Self-Interstitial Dominated Silicon Wherein V/G_O is Controlled by Controlling Heat Transfer at the Melt/Solid Interface
09/817,929*		PEND.	99-2600	Stanton	Method for Evaluating A Wafer Cleaning Operation

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/833,777*		PEND.	96-0051	Falster & Holzer	Low Defect Density Silicon And a Process for Producing Low Defect Density Silicon Wherein V/G_0 Is Controlled by Controlling Heat Transfer at the Melt/Solid Interface
09/834,118*		PEND.	00-2900	Iwamoto, Lenk, Schmidt, Spohr, Stanton	Method of Calibrating a Semiconductor Wafer Drying Apparatus
09/834,819*		PEND.	00-1750	Blume	System and Method for Reconditioning a Chiller
09/853,232*		PEND.	98-4901	Falster & Voronkov & Mutti	Process for Preparing Defect Free Silicon Crystals Which Allows for Variability in Process Conditions
09/859,094*		PEND.	98-3751	Wilson, Rossi & Yang	An Epitaxial Silicon Wafer With Intrinsic Gettering and a Method for The Preparation Thereof
09/859,826*		PEND.	99-0053	Phillips, Keltner, Holder & Drafall	Barium Doping of Molten Silicon for Use in Crystal Growing Proces
09/865,083*		PEND.	00-2300	Fei, Yang	A Method for Calibrating Nanotopographic Measuring Equipment
09/869,084[5] WP2766M033		PEND.	99-0200	Inaba, Ikeda & Yoshimura	Method for Storing Carrier for Polishing
09/871,255*		PEND.	99-1801	Falster, Voronkov	Process for Preparing Low Defect Density Silicon Using High Growth Rates
09/874,487		PEND.	98-0701	Mule'Stagno, Fei Holzer, Korb & Falster	Epitaxial Silicon Wafers Substantially Free of Grown-In Defects
09/892,002*		PEND.	00-3550	Lu, Banan, Tao, Ferry & Cherko	Crystal Puller and Method for Growing Monocrystalline Silicon Ingots
09/896,945*		PEND.	99-1100	Kulkarni, Erk, Schmidt	Process for Etching a Silicon Wafer
09/928,559*		PEND.	98-2350	Zhang, Erk, Xin	Method for Processing a Semiconductor Wafer Using Two-Stage Double-Side Polishing

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
09/929,585		PEND.	98-3101	Falster	Non-oxygen Precipitating Czochralski Silicon Wafers
09/970,404		PEND.	00-2950	Ng, Jose, Nensiek & Albrecht	Apparatus and Process for Producing Polished Semiconduct Wafers
09/972,608		PEND.	98-5401	Voronkov, Falster & Banan	Method for the Production of Low Defect Density Silicon
09/682,677		PEND.	01-1000	Albrecht, Hull & Vadnais	Polishing Apparatus, Polishing Head And Method

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
					US PROVISIONAL APPLICATIONS
60/245,610*		11/2001	99-1800	Falster, Voronkov	Process for Preparing Low Defect Density Silicon Using High Growth Rates
60/249,854*		11/2001	00-2750	Kommu, Wilson	High Throughput Epitaxial Growth by Chemical Vapor Deposition
60/252,715*		11/2001	98-5400	Voronkov, Falster, Banan	A Method for the Production of Low Defect Density Silicon
60/256,783*		12/2001	98-6050	Falster	Process for Reclaiming Semiconductor Wafers and Reclaimed Wafers
60/257,646*		12/2001	00-1100	Holder, McGuire, Burger	Process for Monitoring the Gaseous Environment of a Crystal Puller for Semiconductor Growth
60/258,296*		12/2001	99-1250	Sreedharamurthy, Banan, Holder	Apparatus and Process for the Preparation of Low-Iron Single Crystal Silicon Substantially Free of Agglomerated Intrinsic Point Defects
60/258,414*		12/2001	00-1050	Ries, Wilson, Standley Shive, Rossi	Semiconductor Wafer Manufacturing Process
60/259,000*		12/2001	99-1050	Mohr, Mule'Stagno Fei, Banan	Silicon Wafers Substantially Free of Oxidation Induced Stacking Faults
60/259,362		01/2002	00-1400	Falster, Voronkov, Mutti & Bonoli	Process for Preparing Single Crystal Silicon Having Improved Gate Oxide Integrity
60/264,415*		01/2002	01-0150	Kim, Kimbel Libbert & Banan	Low Defect Density Silicon Substantially Free of Oxidation Induced Stacking Faults
60/273,980[5]		03/2002	01-0100 WP3536M054	Kojima, Ishii	A Method for Growing a Single Crystal Silicon
60/280,035*		03/2002	00-0450	Vasat, Stefanescu, Torack & Wilson	Thermal Annealing Process for Producing Silicon Wafers With Improved Surface Characteristics

US PATENTS

PAT. OR * APPLN	GRANT DATE	EXP. YEAR	MEMC FILE #	INVENTOR(S	TITLE
60/280,680*		03/2002	99-2750	Grabbe, Doane	Solution Compositions and Process for Etching Silicon
60/283,103*		04/2002	00-1650	Binns	Control of Thermal Donor Formation in High Resistivity CZ Silicon
60/285,180*		04/2002	00-1600	Borgini, Gambaro, Ravani, Ries, Sacchetti & Standley	A Method for the Preparation of an Epitaxial Silicon Wafer with Intrinsic Gettering
60/300,208*		06/2002	01-1150	Falster	Process for Producing Silicon on Insulator Structure Having Intrinsic Gettering by Ion Implantation
60/300,364*		06/2002	01-1450	Binns	Silicon on Insulator Structure From High Resistivity CZ Silicon
60/301,767*		07/2002	98-4950	Kimbel, Johnson, Kim, McCallum, Alexander & Holzer	Process for Preparing Defect Free Silicon by Controlling the Average Axial Temperature
60/302,907*		07/2002	99-3450	Shive	Process for Making Wafers for Ion Implantation
[5]60/308,521		07/2002	00-3350 WP3421M051	Haga, Aoshima & Banan	A Single Crystal Plate of Silicon Epitaxial Wafer and The Method for Producing the Same
60/309,645		08/2002	99-0350	Philips, Keltner & Holder	Method of Eliminating Near-Surface Bubbles in Quartz Crucibles
60/312,573*		08/2002	00-1500	Javidi	Controlled Crown Growth Process for Czochralski Single Crystal Silicon
60/315,846*		08/2002	01-0300	Sreedharamurthy & Nithianathan	Process for Eliminating Neck Dislocations During Czochralski Crystal Growth
60/325,622		09/2002	01-0200	Kulkarni, Banan & Luers	Process for Preparing an Arsenic-Doped Single Crystal Silicon Using A Consumable Dopant Feeder
60/325,660		09/2002	01-0250	Kulkarni, Banan	Process for Preparing an Arsenic-Doped Single Crystal Silicon Using A Non-Consumable Dopant Feeder

CLEARY, GOTTLIEB, STEEN & HAMILTON

ONE LIBERTY PLAZA
NEW YORK, NY 10006-1470

2000 PENNSYLVANIA AVENUE, N.W.
WASHINGTON, DC 20006-1801

41, AVENUE DE FRIEDLAND
75008 PARIS

RUE DE LA LOI 23
1040 BRUSSELS

CITY PLACE HOUSE
55 BASINGHALL STREET
LONDON EC2V 5EH

TEMPORARY OPERATIONS CENTER AND
CENTRAL MAIL ADDRESS

THE CITIGROUP CENTER
153 EAST 53RD STREET
NEW YORK, NY 10022

VOICEMAIL ACCESS TO NY LAWYERS
(212) 572-5202

MAIN
(212) 572-5353

FACSIMILE
(212) 572-5399

MAIN TOWER
NEUE MAINZER STRASSE 52
60311 FRANKFURT AM MAIN

PIAZZA DI SPAGNA 15
00187 ROME

BANK OF CHINA TOWER
ONE GARDEN ROAD
HONG KONG

SHIN KASUMIGASEKI BUILDING
3-2, KASUMIGASEKI 3-CHOME
CHIYODA-KU TOKYO 100-0013

Writer's Direct Dial: (212) 572-5260

VIA COURIER

United States Patent and Trademark Office
Attention Customer Services Counter Crystal Gateway #4
3rd Floor
Box Assignment
FEE
1213 Jefferson Davis Highway
Arlington, VA 22202

November 21, 2001

Dear Commissioner:

Enclosed are the following items:

1. Recordation Form Cover Sheet for Patents
2. Termination Agreement relating to patents
3. A check for $10240.00 USD to cover the filing fees related to filing the Termination Agreement for recordation

Kindly date stamp the receipt copy of this cover letter as proof of receipt and return the date stamped receipt copy to us. Should you have any questions, please do not hesitate to contact me at my temporary telephone number (212) 572-5260. Thank you in advance for you assistance in this matter.

Sincerely,

Brian Crist

Enclosures