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(Rev 6-93)

12-20-2001



FR SHEET

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Patent and Trademark Office

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To the Honorable Commissioner of Patents and Trademarks

and the attached original document or copy thereof.

1. Name(s) of conveying party(ies):

- 1) DONGLIN ZHOU
- 2) YANN DESPREZ-LEGOARANT
- 3)
- 4)
- 5)
- 6)

12-5-01

Additional names of conveying parties attached? ☐ Yes ☒ No

2. Name and address of receiving party:

Name: STMICROELECTRONICS ASIA PACIFIC
(PTE) LTD.

Internal Address: _____

Street Address: 28 ANG MO KIOINDUSTRIAL PARK 2Postal Code & City: 569508 SINGAPORECountry SINGAPOREAdditional names & addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

- ☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other Employment Agreement, Disclosure

Execution Dates:

- 1) JANUARY 13, 1997 4) _____
- 2) AUGUST 23, 2001 5) _____
- 3) JANUARY 16, 1997 6) _____

4. Application number(s) or registration number(s):

If this document is being filed together with a new application,
the filing date of the application is _____.A. Patent Application No(s).
09/463,691

B. Patent No(s).

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Seed Intellectual Property Law Group PLLCInternal Address: DAVID V. CARLSONStreet Address: 701 Fifth Avenue, Suite 6300City: Seattle State: WA ZIP: 98104-7092

6. Total number of applications and patents involved.....

1

7. Total Fee (37 CFR 3.41): \$40

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9. Statement and signature.

*To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.*DAVID V. CARLSON

Name of Person Signing

Signature

Date

Dec 5, 2001

Total number of pages including cover sheet, attachments, and document: 21

ASSIGNMENT

WHEREAS, we, Donglin Zhou and Yann Desprez-LeGoarant (hereinafter referred to as ASSIGNORS), having post office addresses of Design Centre, STA Microelectronics, 52 Tao Hua Road, Fu Tian Fee Trade Zone, 518048 Shenzhen, People's Republic of China, and 12 Cactus Drive #05-01, Singapore 809688, respectively, are the joint inventors of an invention entitled "X-RAY PROTECTION CIRCUIT," as described and claimed in the specification of International Application Number PCT/SG97/00030, accorded an International Filing Date of 21 July 1997, for which an application for United States letters patent is sought.

WHEREAS, STMicroelectronics Asia Pacific (PTE) LTD. (hereinafter referred to as ASSIGNEE), a corporation of the country of Singapore having a place of business at 28 Ang Mo Kio Industrial Park 2, Singapore 569508, is desirous of acquiring the entire right, title and interest in and to the invention and in and to any letters patent that may be granted therefor in the United States.

NOW, THEREFORE, in exchange for good and valuable consideration, the receipt of which is hereby acknowledged, ASSIGNORS hereby sell, assign and transfer unto said ASSIGNEE the entire right, title and interest in and to said invention, said application and any and all letters patent which may be granted for said invention in the United States of America and its territorial possessions, and in any and all divisions, reissues and continuations thereof, said invention, application and all letters patent on said invention to be held and enjoyed by ASSIGNEE and its successors and assigns as fully and entirely as the same would have been held and enjoyed by ASSIGNORS had this assignment, transfer and sale not been made. ASSIGNORS hereby authorize and request the Commissioner of Patents and Trademarks to issue all letters patent on said invention to ASSIGNEE. ASSIGNORS agree to execute all instruments and documents required for the making and prosecution of applications for United States letters patent on said invention, for litigation regarding letters patent, or for the purpose of protecting title to said invention or letters patent therefor.

Date

Donglin Zhou

I certify that I know or have satisfactory evidence that the above person signed this instrument of his/her own free will, as a voluntary act for the uses and purposes mentioned in the instrument.

Witness _____

Date: _____

23 August 2001
Date

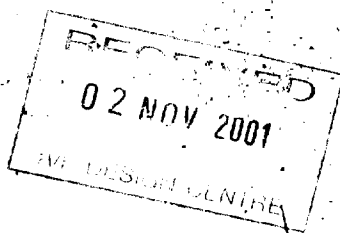
Yann Desprez-LeGoarant

I certify that I know or have satisfactory evidence that the above person signed this instrument of his/her own free will, as a voluntary act for the uses and purposes mentioned in the instrument.

Witness G H L O H

Date: 23 Aug 2001

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编号: 107

深圳市全员劳动合同制

劳动
合同
书

深圳市劳动局编制

甲方(单位)

名称: 深圳赛克微电子有限公司经济类型: 合资

地址: _____

电话: _____

法人代表: 李莫基联系人: 梁昆君

乙方(员工)

姓名: 周东林性别: 男 年龄: 21.31民族: 汉 籍贯: 浙江现住址: 广东深圳市身份证号码: 130302710131223

根据《广东省经济特区劳动条例》及其他有关法律法规的规定，甲乙双方本着平等、自愿、协商一致的原则，达成如下协议：

一、工作岗位和工种(工作)

甲方根据生产(工作)需要，聘用乙方在 生产 岗位从事 工种(工作)，担任 DE工程师 职务。

二、合同期限(试用期限)

(一) 合同期限

甲乙双方选择以下第 1 种形式确定本合同期限为：

1、3 年，合同期从一九九五 年 七月 十六 日起至 2000 年 七 月 十六 日止。

2、不定期，合同期从一九 年 月 日起①。

3、从一九 年 月 日起至
(工作)完成止。

(二) 试用期限

1、无试用期。

2、试用期为 3 个月②。

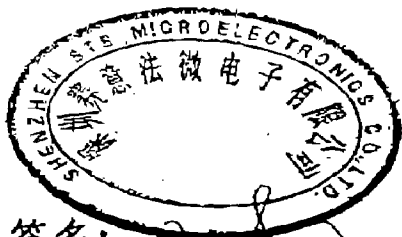
三、工作时间

乙方每日工作 8 小时，平均每周工作 44 小时 ③。甲方安排乙方加班加点每月不得超过 48 小时，或每次班后加点不得超过 4 小时。

加班加点超过前款时间限度的，按有关规定执行。

四、工资待遇和休假

(一) 工资



甲方盖章:

法定代表人签名:

乙方签名: 同东林

双方签订合同

时 间: 95 年 7 月 13 日

鉴证机关盖章:



时 间: 年 月 日

经双方同意, 本合同延期至 年 月 日

甲方盖章:

乙方签名:

法定代表人签名:

双方签订合同

时 间: 年 月 日

鉴证机关盖章:

L11



Total Page:1

Date: 13/Jan/97

From: Gee-Heng LOH

SGS-THOMSON

Fax# 4820240

To: Piero APOCELLI / Agrate

Copy: B MURARI

Our ref: 5-08-12

Subject: Patent Proposal - An X-ray protection Circuit

Inventor: ZHOU DongLin, Yann Desprez-Le Goarant.

I enclosed herewith above mentioned Patent Proposal for your consideration and follow-up.

Please feel free to contact me should you require any clarification.

Your faithfully,



GH LOH

Ang Mo Kio, ext 5540

PATENT

REEL: 012372 FRAME: 0729



PATENT PROPOSAL

5 - 08 - 12

*** CONFIDENTIAL ***

Descriptive Title of Invention:

AN XRAY PROTECTION CIRCUIT

Inventor(s):

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Tel: Fax:

4) First Name:

Family Name:

Private Address:

Employer: ST ☐ Corimme ☐ Site:

Other ☐ Address:

Group: Division: Cost-Center:

PATENT

REEL: 012372 FRAME: 0730

REEL: 012372 FRAME: 0731

1 - Category of the invention

Indicate one letter in the following list that better fits to the invention

- ☐ **D** - Device Silicon structure or part of it and its way of working
- ☒ **C** - Circuit Electric circuit, even if some of its parts are represented by blocks, and its working
- ☐ **S** - System Everything above circuit level, like architectures and methodologies; usually described with a block diagram
- ☐ **F** - Frontend Steps, methodology and manufacturing machines or tools to get to the product before its testing; typically silicon processes
- ☐ **B** - Backend Testing, Packaging, Bonding, Assembly and everything after testing

2 - Product Codes: STV 2128

Indicate the real-product codes in which the invention is or will be used - e.g. TDA123, U012, ...

3 - Product Classes

Indicate one or more words that better describe the products the invention applies to

- ☐ **A/D** Analog to digital converters
- ☐ **AGC** Automatic Gain Control systems
- ☐ **AMPLIFIER** Amplifiers architectures and circuits
- ☐ **ANALOG** Products for analogic applications; always used in combination with another word (for example CMOS ANALOG)
- ☐ **AUDIO** Every device, circuit or system Audio- or Radio- dedicated
- ☐ **AUTO** All the products for automotive applications (Ignition, Injection and Instrumentation)
- ☐ **BATTERY** Battery chargers and accessories
- ☐ **BCD** BCD technology
- ☐ **B/E** Everything in backend that is not Packaging or Testing
- ☐ **BICMOS** BICMOS technology
- ☐ **BIPOLAR** Bipolar technology and devices
- ☐ **CCD** CCD devices
- ☐ **CMOS** CMOS devices, circuits and technology
- ☐ **COMPUTER** Everything applies to Computers and is not included in GRAPHICS, PERIPHERAL and PROCESSORS which are defined below
- ☐ **D/A** Digital to analog converters
- ☐ **DESIGN** Products and methods to carry out design
- ☐ **DIODE** Diode devices
- ☐ **DISPLAYS** Circuits, devices and architectures for displays and monitors
- ☐ **DRAM** DRAM memory cells and circuits
- ☐ **DRIVERS** Circuits and systems to drive Hard-Disks and to interface with them
- ☐ **EPROM** EPROM memory cells and circuits
- ☐ **EEPROM** EEPROM memory cells and circuits
- ☐ **F/E** Everything in frontend which cannot be classified with other words of this list, such as machine and tools used in silicon processes

PATENT

REEL: 012372 FRAME: 0732

- ☐ **FILTER** Analog and digital filters
- ☐ **FLASH** FLASH memory cells and circuits
- ☐ **FUZZY** Fuzzy logic processors, architectures and methods
- ☐ **GRAPHICS** Graphic processors
- ☐ **HCMOS** HCMOS technology and devices
- ☐ **HPD** High Power Devices
- ☐ **IGBT** IGBT devices and technology
- ☐ **ISDN** ISDN protocols and relative circuits
- ☐ **LAMP** Lamp driver devices and circuits (Light Ballast)
- ☐ **LOGIC** All logic circuits (FLIP-FLOPs ...), families (TTL ...) and interfaces
- ☐ **MODEM** Circuits and systems for modems
- ☐ **MOS** MOS devices and technology
- ☐ **MOTORS** Everything deals with electric motors, such as drivers or regulators
- ☐ **MPEG** Everything deals with MPEG
- ☐ **NEURAL** Neural networks and their applications
- ☐ **NVRAM** NVRAM memories
- ☐ **PACKAGING** Packages and their manufacturing methods
- ☐ **PASSIVE** Passive devices (Resistors, Inductors, Capacitors)
- ☐ **PERIPHERAL** Peripheral controllers and interfaces
- ☐ **PIC** Power Integrated Circuits, such as integrated drivers and controllers of an output power stage
- ☐ **PLA** Devices, circuits and systems for Programmable Linear Arrays
- ☐ **POWER BIPOLAR** Power Bipolar transistors and technology
- ☐ **POWER MOS** Power MOS technology and devices
- ☐ **POWER ON RESET** Circuits or devices to initialize a system at switching on
- ☐ **POWER SUPPLY** Circuits and systems for supplying power, such as e.g. generators
- ☐ **PROCESSORS** Used together with Peripheral and Graphics to better specify Computer products classification
- ☐ **PROTECTION** Protection circuits, devices and systems (against overvoltages, overcurrents, ElectroStatic Discharge ...)
- ☐ **REGULATOR** Voltage regulators, stabilizers, elevators and every circuit that fixes a defined voltage
- ☐ **ROM** , ROM memory cells and circuits
- ☐ **SENSORS** Sensing devices and relative circuitry
- ☐ **SHADOW RAM** SHADOW RAM memories
- ☐ **SLIC** Telecom circuits and systems on the Central Office's side
- ☐ **SMART POWER** Smart Power applications
- ☐ **SRAM** SRAM memory cells and circuits
- ☐ **TESTING** methods, circuits and apparatuses for testing
- ☐ **TELEPHONE SET** Telecom circuits and systems on the Subscriber's side
- ☒ **TV** All circuits and devices for TV sets
- ☐ **VIPOWER** Products in VIPOWER technology or modifications to process steps
- ☐ **OTHERS**

PATENT

REEL: 012372 FRAME: 0733

PATENT PROPOSAL #: 5-08-12
COMPANY SECRET

January 13, 1997

 Title : **AN XRAY PROTECTION CIRCUIT**
ABSTRACT :


This patent describes the XRAY circuit in the video processor which is able to work with the parasitic spike generated by the ESD. This circuit and method are especially useful in the bistate circuit which has one safe state. The circuit uses a power on reset circuit which is sensible to the parasitic spike generated by the ESD and a RS-flip-flop to make the bistate circuit in the safe state after the parasitic spike generated by the ESD.

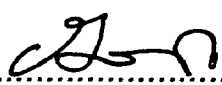
The circuit has the following advantages:

1. It can work with the parasitic spike generated by the ESD with low cost and can be integrated.
2. It also useful for the design of the bistate circuit with one safe state.

Distribution List :	Divisional R & D :	B. Murari	Copy # 1.....
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 PROPOSED BY : 
 Z.DL & Y.DLG

 WITNESS : 
 GEE-HENG LOH

 APPROVED BY : 
 (M SANTI)

 DATE : 16 JAN 97
 DEC 23th, 1996

INTRODUCTIONS:

The XRAY protection circuit is a circuit used in the video processor to prevent too high voltage on the EHT of the tube of the TV set. It consists in detecting the line flyback amplitude and disabling the horizontal output pulse when the amplitude of the flyback exceeds a certain limit. The horizontal output will be enabled again after a power OFF of the TV set.

The conventional XRAY circuit includes a bangap comparator with a 1.3 V threshold voltage and an analog d-latch (thyristor structure). The main problem of the conventional circuit is that the analog d-latch (thyristor structure) is easy to trigger by the parasitic spike generated by the ESD, so it will hold on the wrong state and can not automatically correct itself.

The new XRAY circuit that will be described later gives a solution to make the circuit working with the parasitic spike generated by the ESD with low additional cost and can be integrated. The method is also useful for the design of the bistate circuit with one safe state.

DESCRIPTION OF THE CONVENTIONAL CIRCUIT:

One of the conventional circuit is as shown in Fig 1.

The circuit includes a bangap comparator with a 1.3V threshold voltage and an analog d-latch (thyristor structure). When the voltage at the XRAY input exceeds the 1.3V threshold, the event will trigger an analog d-latch and the XRAY output will be high. The d-latch will memorize the XRAY detection, it can hold on until the supply voltage VCC is reduced to a voltage below 3V.

The main problem of this circuit is that the analog d-latch (thyristor structure) is easy to trigger by the parasitic spike generated by the ESD. The triggered state is not a safe state for the circuit since it can not automatically change to untriggered state if it is the wrong state. Thus the XRAY will hold on the-wrong state and can not correct itself automatically.

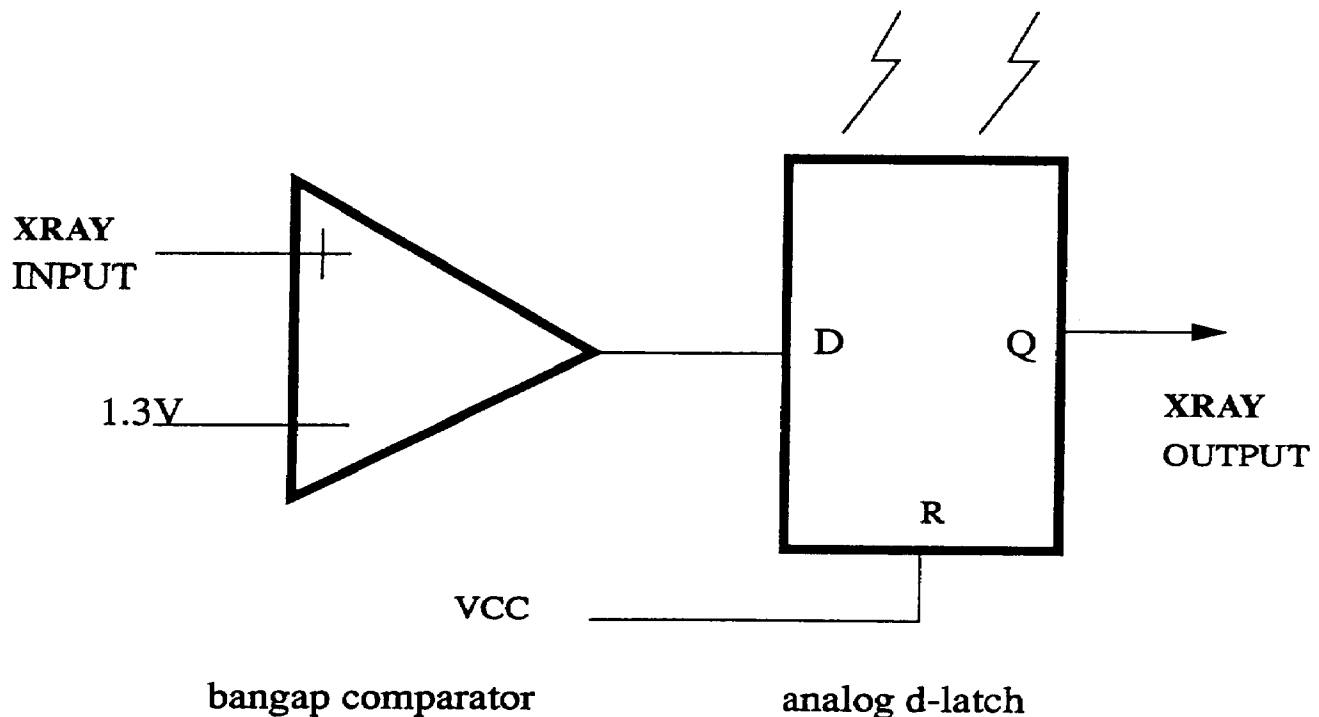


Fig 1: the conventional XRAY circuit

DESCRIPTION OF THE NEW CIRCUIT:

The new XRAY protection circuit includes a bangap comparator with a 1.3V threshold voltage, a power on reset circuit and a RS-flip-flop. The circuits is as shown in Fig 2.

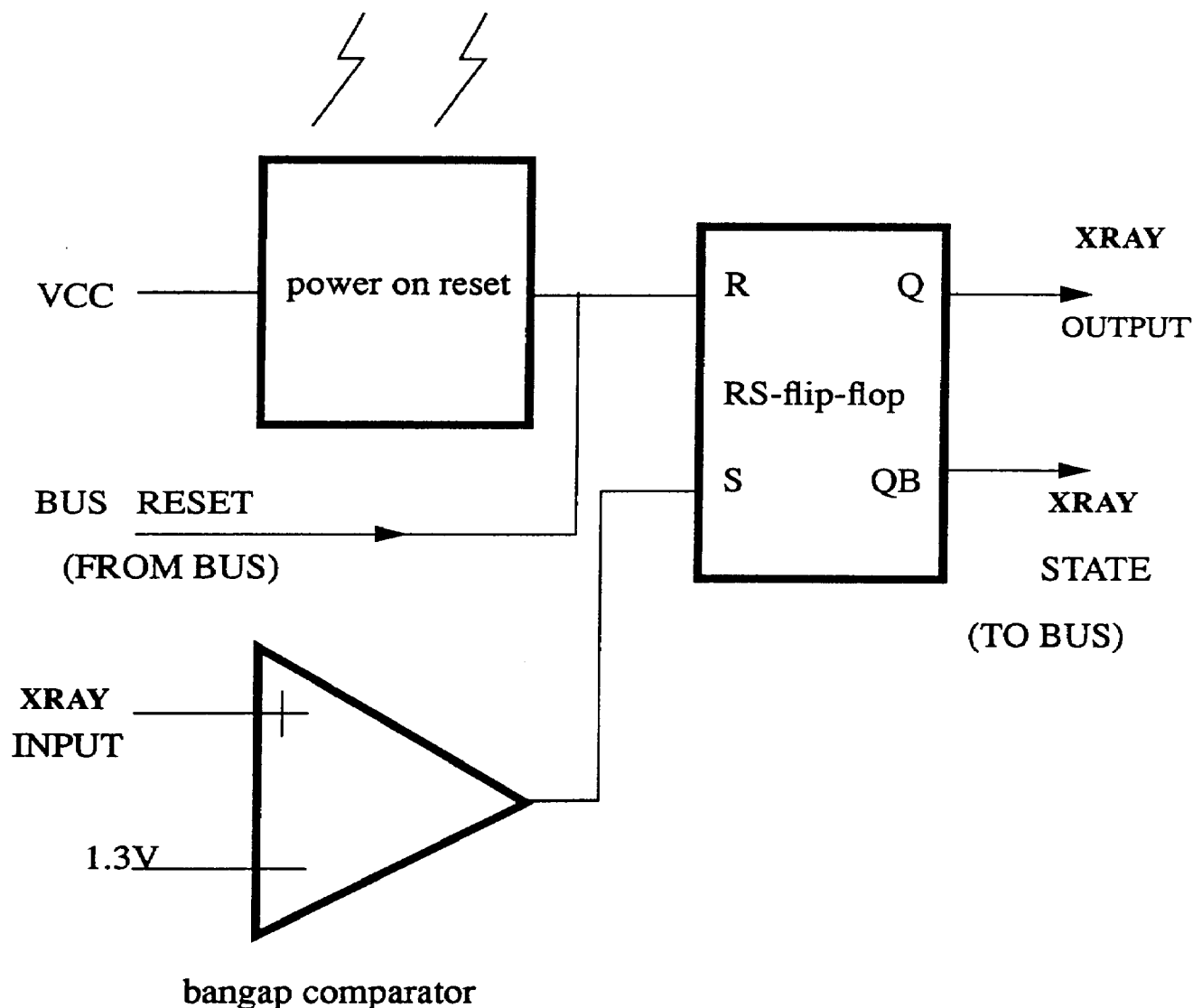


Fig 2: the new XRAY circuit

The improvements compared to the conventional circuit:

- a) The analog d-latch is replaced by the RS-flip-flop which will inhibit the S input if R and S inputs is triggered at the same time.
- b) An additional power on reset circuit is applied in this circuit which is sensible to the parasitic spike generated by the ESD, and it will make the XRAY into the safe state when the parasitic spike generated by the ESD comes.
- c) There is more gates delay for the power on reset circuit compared to the bangap comparator.
- d) There are two signal lines connected with the BUS which is the additional solution to recover the XRAY if it is wrongly triggered by the spike generated by the ESD.

The new circuit is described as following:

(1) During the power ramping up the power on reset circuit will reset the RS-flip-flop, so the XRAY is in the untriggered state. When the voltage at the XRAY input exceeds the 1.3V threshold, the event will trigger the RS-flip-flop and the XRAY will change into the triggered state. The RS-flip-flop will memorize the XRAY detection, it can hold on until the supply voltage VCC is reduced to a certain voltage so that the power on reset circuit will generate a reset signal.

(2) The power on reset circuit is as shown in the Fig 3.

Refer to Fig 3

$$I1=(VCC-2V_{be})/R$$

$$I2=(VCC- V_{be})/2R$$

Therefore,

- 1) when $VCC \leq V_{be}$, $I=0$
- 2) when $V_{be} < VCC < 3V_{be}$, $I>0$
- 3) when $VCC \geq 3V_{be}$, $I=0$

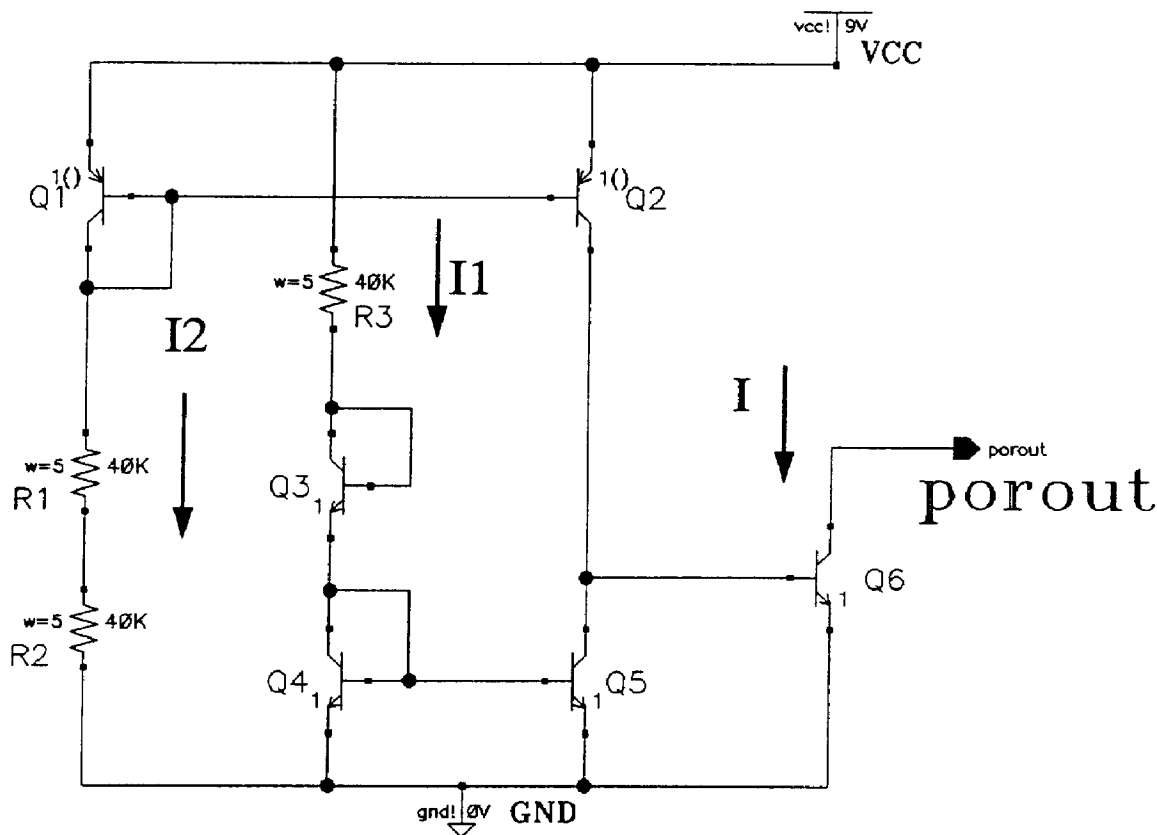


Fig 3: the power on reset circuit

This power on reset circuit is different from the general power on reset circuit. After the power ramping up, the general power on reset circuit has some output current; in this circuit, since $VCC > 3V_{be}$, so there is no output current. The transistor Q6 is blocked (collector is high impedance). When the parasitic spike generated by the ESD comes, Q6 is quite easy to trigger, this is proven by doing the simulation that during the spike of the supply voltage VCC, ground and substrate, the circuit is easy to give a current spike at I output.

(3) The RS-flip-flop circuit is as shown in the Fig 4.

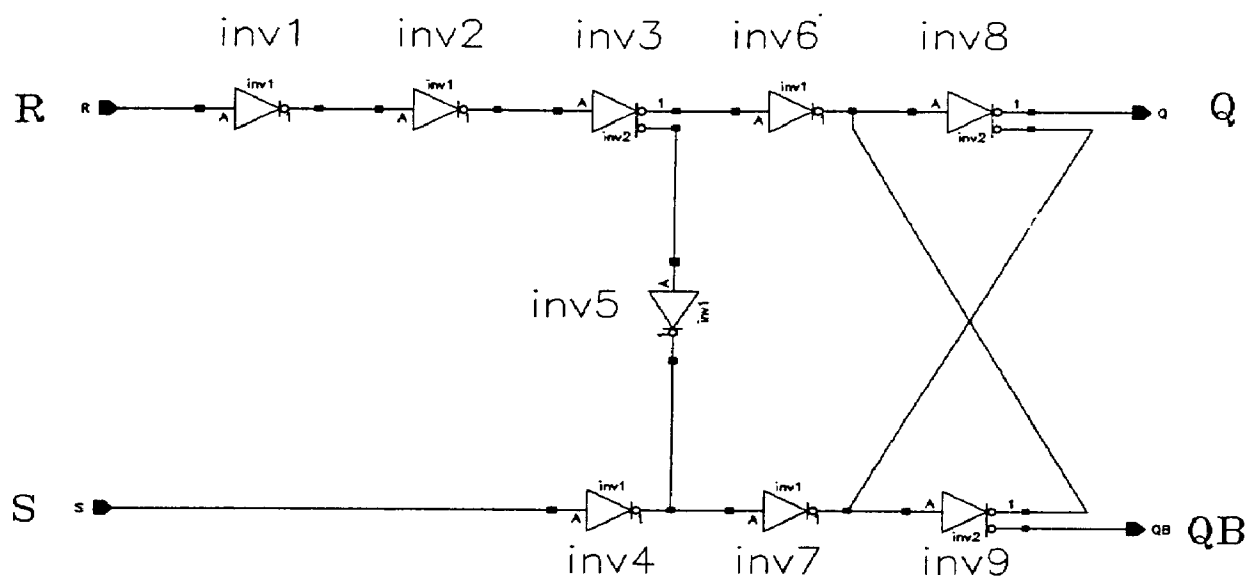


Fig 4: the RS-flip-flop circuit

The RS-flip-flop is different from ordinary RS-flip-flop. The inverter inv1, inv2 and inv5 are the additional components compared to the ordinary RS-flip-flop. If the circuit is triggered at the same time by both the R and S inputs, since the inverter inv5 exist, the result is $Q=0$ and $QB=1$. And since the R signal has two more gates delay, so after triggering, the circuit will keep in the untriggered state. So that means the S input will be inhibited if the R input and S input are triggered at the same time.

(4)The XRAY has two states: the triggered state and the untriggered state. The triggered state is not a safe state for the XRAY since it can not correct itself if it is the wrong state. The untriggered state is a safe state for the XRAY since it will immediately change into the triggered state if it is the wrong state. So if the XRAY is in the untriggered state before the parasitic spike generated by the ESD, it also should keep in the untriggered state after the parasitic spike generated by the ESD; if the XRAY is in the triggered state before the parasitic spike generated by the ESD, it

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can be either in the triggered or untriggered states since the untriggered state will be triggered immediately if the input voltage is still higher than 1.3 V.

(5) When the parasitic spike generated by the ESD comes, since the power on reset circuit is triggered, the RS-flip-flop will be reset and this will make the XRAY into the untriggered state whatever it is in the triggered or untriggered state before the parasitic spike generated by the ESD. Thus the XRAY circuit will be in the safe state. So this circuit can work with the parasitic spike generated by the ESD.

(6) The circuit also has two additional signal lines connected with the BUS. One is used to send the state of the RS-flip-flop to the BUS, another is used to reset the RS-flip-flop with the reset signal from the BUS. So the microcontroller can control the XRAY through the BUS. If the microcontroller detects the XRAY is in the triggered state, it can send the reset signal to the XRAY and detect the new state of the XRAY. If the XRAY is still in the triggered state, this means that the last triggering is the correct triggering; otherwise the last triggering is the wrong triggering. In this way, even the XRAY is wrongly triggered by the parasitic spike generated by the ESD, the microcontroller still can recover it. So this circuit can work with the parasitic spike generated by the ESD.

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COMPANY SECRET**CONCLUSION:**

This circuit is integrated in the STV2128 (video processor). The circuit was designed to fit the test of the parasitic spike generated by the ESD which is some customer's special requirement. In the simulation, this circuit is 10 times stronger than the conventional circuit when it works with the parasitic spike generated by the ESD.

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