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FORM PTO-1595 REC T U.S. DEPARTMENT OF COMMERCE
1-31-92 Patent and Trademark Office

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To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

The Chase Manhattan Bank, as Administrative Agent
(New York banking corporation)

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Name: General Semiconductor, Inc.
Internal Address:
Street Address: 10 Melville Park Road
City: Melville State: NY ZIP: 11747
Additional name(s) & addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other Termination and Release of Securiity Interest in Patent Rights
Execution Date: November 2, 2001

4. Application number(s) or patents number(s):

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s) **See Attached Continuation of Item 4**

B. Patent No.(s) **See Attached Continuation of Item 4**

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Robyn Greenberg, Esq.
Internal Address: Simpson Thacher & Bartlett
Street Address: 425 Lexington Avenue
City: New York State: New York ZIP: 10017

6. Total number of applications and patents involved: 57

7. Total fee (37 CFR 3.41): ..... $ 2,280.00
☒ Enclosed
☐ Authorized to be charged to deposit account

8. Deposit account number:

(Attached duplicate copy of this page if paying by deposit account)

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9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Robyn Greenberg, Esq. — Name of Person Signing
Robyn Greenberg — Signature
1/7/02 — Date

Total number of pages comprising cover sheet: 10

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Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents and Trademarks, Box Assignments
Washington, D.C. 20231

CONTINUATION OF ITEM FOUR FROM RECORDATION COVER SHEET

Application number(s) or patent number(s):

U.S. Patent No.	U.S. Patent No.	U.S. Patent Application No.
4,293,755	5,097,308	08/282,914
4,284,867	5,102,810	08/541,605
4,238,436	5,008,735	08/580,071
4,271,235	5,151,846	08/554,749
4,499,354	5,371,647	08/649,135
4,638,551	5,248,902	08/580,070
4,742,377	5,512,784	09/010,471
4,522,149	5,304,429	
4,564,885	5,324,685	
4,590,667	5,432,121	
4,659,400	5,571,329	
4,740,477	5,245,412	
4,891,685	5,528,079	
5,010,023	4,599,636	
4,859,621	5,360,509	
4,929,987	5,298,457	
4,789,886	5,342,805	
4,942,139	5,506,174	
4,987,476	5,484,097	
4,904,610	5,399,901	
4,829,406	5,814,874	
4,980,315	5,882,986	
5,166,769	5,930,660	
5,278,095	5,631,806	
4,921,158	5,635,414	

TERMINATION AND RELEASE OF SECURITY INTEREST IN PATENT RIGHTS

TERMINATION AND RELEASE dated as of November 2, 2001, from The Chase Manhattan Bank, a New York banking corporation, as Administrative Agent (the "Administrative Agent") for the banks (the "Banks") from time to time party to the Credit Agreement (as hereinafter defined), to General Semiconductor, Inc. (the "Borrower"), a Delaware corporation, located at 10 Melville Park Road, Melville, New York 11747-3113.

WITNESSETH:

WHEREAS, the Borrower is a party to the Credit Agreement, dated as of July 23, 1997, with the Administrative Agent, the Banks and the co-agents named therein (as amended, supplemented or otherwise modified from time to time, the "Credit Agreement");

WHEREAS, the Credit Agreement was amended by the Second Amendment dated as of June 22, 1999 (the "Second Amendment"), and, pursuant to the Second Amendment, the Borrower and certain subsidiaries (together, the "Grantors") agreed to execute and deliver the Guarantee and Collateral Agreement (as hereinafter defined);

WHEREAS, pursuant to that certain Guarantee and Collateral Agreement dated as of August 15, 1999, made by the Borrower in favor of the Administrative Agent (the "Guarantee and Collateral Agreement"), a security interest (the "Security Interest") was granted by the Grantors to the Administrative Agent in certain collateral, including the Patent Collateral (as hereinafter defined); and

WHEREAS, the Guarantee and Collateral Agreement was recorded in the Patent Division of the United States Patent & Trademark Office on November 12, 1999, at Reel 010388 and Frame 0894; and

WHEREAS, the Administrative Agent now desires to terminate and release the entirety of its security interest in the Patent Collateral;

NOW, THEREFORE, for good and valuable consideration including the satisfaction of all obligations, indebtedness and liabilities secured by the Patent Collateral pursuant to the Security Agreement, the receipt and adequacy of which are hereby acknowledged, and upon the terms set forth in this Termination and Release, the Administrative Agent hereby states as follows:

1. Patent Collateral: The term "Patent Collateral," as used herein, shall mean all of the Borrower's right, title and interest of every kind and nature as of the date hereof in the Patents (including, without limitation, those items listed on Schedule A hereto). The term "Patents" shall have the meaning provided by reference in the Conditional Assignment.

2. Release of Security Interest: The Administrative Agent, hereby terminates, releases and discharges its Security Interest in the Patent Collateral, and any right, title or interest of the Administrative Agent in such Patent Collateral shall hereby cease and become void.

3. Further Assurances: The Administrative Agent hereby agrees to duly execute, acknowledge, procure and deliver any further documents and to do such other acts as may be reasonably necessary to effect the release of the Security Interest contemplated hereby.

IN WITNESS WHEREOF, the undersigned has executed this Termination and Release by its duly authorized officer as of the date first above written.

THE CHASE MANHATTAN BANK

By: _____
Name: Robert A. Krasnow
Title: Vice President

STATE OF Illinois)
) ss.:
COUNTY OF Cook)

On this 2nd day of Nov., 2001, before me personally appeared Robert A. Krasnow to me known who, being by me duly sworn, did depose and say that he/she is Vice President of The Chase Manhattan Bank, described herein and which executed the foregoing instrument, and that he/she signed his/her name thereto pursuant to the authority granted by The Chase Manhattan Bank.

Deborah K. Welles
Notary Public

(Affix Seal Below)

"OFFICIAL SEAL"
DEBORAH K. WELLES
NOTARY PUBLIC, STATE OF ILLINOIS
MY COMMISSION EXPIRES 03/10/02

509265-0048-08725-NY02.2135181.2

Schedule A

U.S. Patents and Patent Applications

TITLE	REG. NO.	APP. NO.
Method of Cooling Induction-Heated Vapor Deposition Apparatus and Cooling Apparatus Therefor	4,293,755	
Chemical Vapor Deposition Reactor with Infrared Reflector	4,284,867	
Method of Obtaining Polycrystalline Silicon	4,238,436	
Method of Obtaining Polycrystalline Silicon and Workpiece Useful Therein	4,271,235	
Susceptor for Radiant Absorption Heater System	4,499,354	
Schottky Barrier Device and Method of Manufacture	4,638,551	
Schottky Barrier Device With Doped Composite Guard Ring	4,742,377	
Reactor and Susceptor for Chemical Vapor Deposition Process	4,522,149	
Rectifier with Slug Construction and Mold for Fabricating Same	4,564,885	
Method and Apparatus for Assembling Semiconductor Devices Such as Leds or Optodetectors	4,590,667	
Method for Forming High Yield Epitaxial Wafers	4,659,400	
Method for Fabricating a Rectifying P-N Junction Having Improved Breakdown Voltage Characteristics	4,740,477	
Rectifying P-N Junction Having Improved Breakdown Voltage Characteristics and Method for Fabricating Same	4,891,685	
Method for Fabricating a Rectifying Semiconductor Junction Having Improved Breakdown Voltage Characteristics	5,010,023	
Method for Setting the Threshold Voltage of a Vertical Power Mosfet	4,859,621	
Method for Setting the Threshold Voltage of a Power Mosfet	4,929,987	
Method and Apparatus for Insulating High Voltage Semiconductor Structures	4,789,886	

TITLE	REG. NO.	APP. NO.
Method of Fabricating a Brazed Glass Pre-Passivated Chip Rectifier	4,942,139	
Brazed Glass Pre-Passivated Chip Rectifier	4,987,476	
Wafer Level Process for Fabricating Passivated Semiconductor Devices	4,904,610	
Square Body Leadless Electrical Device	4,829,406	
Method of Making a Passivated P-N Junction in Mesa Semiconductor Structure	4,980,315	
Passivated Mesa Semiconductor and Method for Making Same	5,166,769	
Method for Making Passivated Mesa Semiconductor	5,278,095	
Brazing Material	4,921,158	
Method for Controlling the Switching Speed of Bipolar Power Devices	5,097,308	
Method for Controlling the Switching Speed of Bipolar Power Devices	5,102,810	
Packaged Diode for High Temperature Operation	5,008,735	
Surface Mountable Rectifier and Method for Fabricating Same	5,151,846	
Surge Protection Circuit Module and Method for Assembling Same	5,371,647	
Surface Mounting Diode	5,248,902	
Surge Protector Semiconductor Subassembly for 3-Lead Transistor Aotline Package	5,512,784	
Semiconductor Devices Having Copper Terminal Leads	5,304,429	
Method for Fabricating a Multilayer Epitaxial Structure	5,324,685	
Method for Fabricating a Multilayer Epitaxial Structure	5,432,121	
Gas Flow System for CVD Reactor	5,571,329	
Low Capacitance Silicon Transient Suppressor with Monolithic Structure	5,245,412	

TITLE	REG. NO.	APP. NO.
Hermetic Surface Mount Package for a Two Terminal Semiconductor Device	5,528,079	
Two Terminal Axial Lead Suppressor and Diode Bridge Device	4,599,636	
Low Cost Method of Fabricating Epitaxial Semiconductor Devices	5,360,509	
Method of Making Semiconductor Devices Using Epitaxial Techniques to Form SI/SI-GE Interfaces and Inverting the Material	5,298,457	
Method of Growing a Semiconductor Material by Epilaxy	5,342,805	
Automated Assembly of Semiconductor Devices Using a Pair of Lead Frames	5,506,174	
Fabrication of Hybrid Semiconductor Devices	5,484,097	
Semiconductor Devices Having a Mesa Structure and Method of Fabrication for Improved Surface Voltage Breakdown Characteristics	5,399,901	
Semiconductor Device Having a Shorter Switching Time with Low Forward Voltage	5,814,874	
Semiconductor Chips Having a Mesa Structure Provided by Sawing	5,882,986	
Method for Fabricating Diode with Improved Reverse Energy Characteristics	5,930,660	
Lead with Slits for Reducing Solder Overflow and Eliminating Air Gaps in the Execution of Solder Joints	5,631,806	
Low Cost Method of Fabricating Shallow Junction, Schottky Semiconductor Devices	5,635,414	
Containing Apparatus for Electronic Parts		08/282,914
Containing Apparatus for Electronic Parts		08/541,605
TVS FER with Optimized Placing of SI-GE Layers		08/580,071
Mesa Semiconductor Structure with Depressed Region		08/554,749
Planar P-N Junction Structure with Multilayer Passivation		08/649,135
Method & Apparatus for Injection Molding of...		08/580,070

TITLE	REG. NO.	APP. NO.
Epitaxial-Type Semiconductor with Improved Resistance to Transient...		09/010,471