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Expires 06/30/99
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Conveyance Type

☑ Assignment ☐ Security Agreement

☐ License ☐ Change of Name

☐ Merger ☐ Other

U.S. Government
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☐ Departmental File ☐ Secret File

Conveying Party(ies)

☐ Mark if additional names of conveying parties attached

Name (line 1) Intersil Corporation
Execution Date Month Day Year 04/06/2001

Name (line 2) 7585 Irvine Center Drive, Suite 100

Second Party
Name (line 1) Irvine, California 92618
Execution Date Month Day Year

Name (line 2)

Receiving Party

☐ Mark if additional names of receiving parties attached

Name (line 1) Fairchild Semiconductor Corporation

Name (line 2)

Address (line 1) 82 Running Hill Road

Address (line 2) MS35-4E

Address (line 3) South Portland | ME | 04106
City | State/Country | Zip Code

☐ If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative is attached. *(Designation must be a separate document from Assignment.)*

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name

Address (line 1)

Address (line 2)

Address (line 3)

Address (line 4)

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FORM PTO-1619B
Expires 06/30/99
OMB 0651-0027

U.S. Department of Commerce
Patent and Trademark Office
PATENT

Correspondent Name and Address

Area Code and Telephone Number: (716) 262-3640

Name: Thomas R. FitzGerald, Esq.
Address (line 1): Jaeckle Fleischmann & Mugel, LLP
Address (line 2): 39 State Street
Address (line 3): Rochester, New York 14614-1310
Address (line 4):

Pages

Enter the total number of pages of the attached conveyance document including any attachments. # 9

Application Number(s) or Patent Number(s)

☐ Mark if additional numbers attached

Enter either the Patent Application Number or the Patent Number (DO NOT ENTER BOTH numbers for the same property).

Patent Application Number(s)			Patent Number(s)		
~~09/767,092~~					
60/271,832					

If this document is being filed together with a new Patent Application, enter the date the patent application was: Month Day Year

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned.

PCT ______ PCT ______ PCT ______
PCT ______ PCT ______ PCT ______

Number of Properties

Enter the total number of properties involved. # 2

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): $ 80.00

Method of Payment: Enclosed ☑ Deposit Account ☐

Deposit Account
(Enter for payment by deposit account or if additional fees can be charged to the account.)
Deposit Account Number: # 10-0223

Authorization to charge additional fees: Yes ☑ No ☐

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Thomas R. FitzGerald, Esq.		January 17, 2002
Name of Person Signing	Signature	Date

PATENT AND PATENT APPLICATION ASSIGNMENT

WHEREAS, INTERSIL CORPORATION, a Delaware corporation having its principal office at 7585 Irvine Center Drive, Suite 100, Irvine, California 92618, USA, is the owner of the entire right, title, and interest in and to the US and foreign patents and patent applications listed in Exhibit A attached hereto;

AND WHEREAS, FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation having its principal office at 82 Running Hill Road, South Portland, Maine 04106, USA, is desirous of acquiring the entire right, title, and interest in and to said US and foreign patents and patent applications listed in Exhibit A attached hereto;

NOW THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, INTERSIL CORPORATION does hereby sell, assign, and transfer to FAIRCHILD SEMICONDUCTOR CORPORATION, and its successors and assigns, the entire right, title, and interest in and to the patents and patent applications listed in Exhibit A, including all reissues, divisions, continuations, continuations-in-part, and extensions thereof, to be held and enjoyed by FAIRCHILD SEMICONDUCTOR CORPORATION as fully and entirely as it would have been held and enjoyed by INTERSIL CORPORATION if this sale and assignment had not been made, including all claims, demands and rights of recovery that FAIRCHILD SEMICONDUCTOR CORPORATION has or may have in profits and damages for past and future infringements, if any, and all rights to compromise, sue for, and collect such profits and damages. Any official whose duty it is to issue patents, is hereby requested to issue any and all patents of the patents and patent applications listed in Exhibit A to FAIRCHILD SEMICONDUCTOR CORPORATION, its successors and assigns.

IN WITNESS WHEREOF, INTERSIL CORPORATION has caused this assignment to be signed by its officer duly authorized to execute this agreement on behalf of INTERSIL CORPORATION.

INTERSIL CORPORATION

By: ________________

Name: PAUL BERNKOPF

Title: ASST. SECRETARY

Date: 4/6/01

State of FLORIDA)
County of BREVARD)

On 06 April 2001, before me, personally appeared Paul A. Bernkopf, known to me to be the person who signed this instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the entity upon behalf of which he/she acted, executed the instrument.

#CC976119

Notary Public

Exhibit A

Pat#	Apl#	Status	Country	Title
	09/767,092	Pending	US	LOW VOLTAGE DUAL-WELL TRENCH MOS DEVICE
	60/271,832	Pending	US	PBSG DEPOSITION AND PLANARIZATION FOR DENS TRENCH MOSFET APPLICATIONS

EXHIBIT A

Pat #	Apl #	Status	Country	Title
4975751	253437	Granted	US	HIGH BREAKDOWN ACTIVE DEVICE STRUCTURE WITH LOW SERIES RESISTANCE
5091336	07/592308	Granted	US	HIGH BREAKDOWN ACTIVE DEVICE STRUCTURE WITH LOW SERIES RESISTANCE
4651179	749091	Granted	US	LOW RESISTANCE GALLIUM ARSENIDE FIELD EFFECT TRANSISTOR
4750666	853255	Granted	US	METHOD OF FABRICATING GOLD BUMPS ON IC'S AND POWER CHIPS
4441117	287497	Granted	US	MONOLITHICALLY MERGED FET AND BIPOLAR JUNCTION TRANSISTOR
4749886	916869	Granted	US	REDUCED PARALLEL EXCLUSIVE OR AND EXCLUSIVE NOR GATE
4857977	88353	Granted	US	LATERAL METAL-OXIDE-SEMICONDUCTOR CONTROLLED TRIACS
4847671	51424	Granted	US	MONOLITHICALLY INTEGRATED INSULATED GATE SEMICONDUCTOR DEVICE
4980740	329034	Granted	US	MOS-PILOT STRUCTURE FOR INSULATED GATE TRANSISTOR
4985740	359811	Granted	US	RESISTANCE
4901127	254897	Granted	US	CIRCUIT INCLUDING A COMBINED INSULATED GATE BIPOLAR TRANSISTOR MOSFET
4933740	243211	Granted	US	INSULATED GATE TRANSISTOR WITH VERTICAL INTEGRAL DIODE AND METHOD OF FABRICATION
4561008	870484	Granted	US	BALLASTED, GATE CONTROLLED SEMICONDUCTOR DEVICE
4532534	415486	Granted	US	MOSFET WITH PERIMETER CHANNEL
4631564	664027	Granted	US	GATE SHIELD STRUCTURE FOR POWER MOS DEVICE
4684413	784726	Granted	US	METHOD FOR INCREASING THE SWITCH SPEED OF A SEMI DEVICE BY NEUTRON IRRADIATION
4901135	232197	Granted	US	HERMETICALLY SEALED HOUSING WITH WELDING SEAL
5095343	07/609054	Granted	US	POWER MOSFET
5023692	447330	Granted	US	POWER MOSFET TRANSISTOR CIRCUIT
5079608	07/609685	Granted	US	POWER MOSFET TRANSISTOR CIRCUIT WITH ACTIVE CLAMP
5148264	07/517799	Granted	US	HIGH CURRENT HERMETIC PACKAGE
5038197	545218	Granted	US	HERMETICALLY SEALED DIE PACKAGE WITH FLOATING SOURCE
4427993	209001	Granted	US	THERMAL STRESS RELIEVING BIMETALLIC PLATE
4700460	924865	Granted	US	BIDIRECTIONAL VERTICAL POWER MOS DEVICE AND FABRICATION METHOD
4644637	567116	Granted	US	INSULATED GATE SEMICONDUCTOR DEVICE WITH IMPROVED SHORTING REGION AND METHOD OF MAKING
4743952	482075	Granted	US	RESISTANCE
4646117	678530	Granted	US	POWER SEMICONDUCTOR DEVICES WITH INCREASED TURN-OFF CURRENT RATINGS
4904609	190903	Granted	US	SYMMETRICAL BLOCKING HIGH VOLTAGE BREAKDOWN SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION
4783690	892739	Granted	US	POWER SEMICONDUCTOR DEVICE WITH MAIN CURRENT SECTION AND EMULATION CURRENT SECTION
4982258	188888	Granted	US	METAL OXIDE SEMICONDUCTOR GATED TURN-OFF THYRISTOR INCLUDIN
	08/310041	Pending	US	FET, IGBT AND MCT STRUCTURES TO ENHANCE OPERATING CHARACTER
4903189	186983	Granted	US	LOW NOISE, HIGH FREQUENCY SYNCHRONOUS RECTIFIER
4641164	868633	Granted	US	MET
4581626	28576	Granted	US	INSULATED GATE TURNOFF THYRISTORS AND TRANSISTORS
4500609	245764	Granted	US	METHOD FOR PRODUCING EUTECTICS AS THIN FILMS
4341594	238726	Granted	US	METHOD OF RESTORING SEMICONDUCTOR DEVICE PERFORMANCE
4417385	406731	Granted	US	SELF ALIGNED, MINIMUM MASK PROC FOR MFG INSULATED GATE SEMI DEVICES WITH INTEGRAL SHORTS
4663547	257080	Granted	US	COMPOSITE CIRCUIT FOR POWER SEMICONDUCTOR SWITCHING
4980741	308498	Granted	US	MOS PROTECTION DEVICE
4506282	455174	Granted	US	NORMALLY OFF SEMICONDUCTOR DEVICE WITH LOW ON-RESISTANCE AN
4641174	510520	Granted	US	PINCH RECTIFIER
4500898	395761	Granted	US	EUTECTIC
4443931	392870	Granted	US	METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH A BASE REGION HAVING A DEEP PORTION

EXHIBIT A

Pat #	Apl #	Status	Country	Title
4430792	406738	Granted	US	SELF ALIGNED MINIMAL MASK PROCESS EMPLOY 2-STEP ETCH FOR MFG INSUL GATE SEMICONDUCTORS
4523111	473089	Granted	US	NORMALLY-OFF, GATE-CONTROLLED ELECTRICAL CIRCUIT WITH LOW ON-RESISTANCE
4739387	497339	Granted	US	SCR HAVING HIGH GATE SENSITIVITY AND HIGH DV/DT RATING
4466176	502834	Granted	US	SELF ALIGNED MINIMAL MASK PROCESS FOR MFG INSULATED GATE SEMI DEVICES WITH INTEGRAL SHORTS
4571815	650315	Granted	US	VERTICAL CHANNEL FIELD CONTROLLED DEVICE EMPLOYING A RECESS
4967243	221482	Granted	US	POWER TRANSISTOR STRUCTURE WITH HIGH SPEED INTEGRAL ANTIPAR
4969027	220649	Granted	US	POWER BIPOLAR TRANSISTOR DEVICE WITH INTEGRAL ANTISATURATION DIODE
4821095	25036	Granted	US	INSULATED GATE SEMICONDUCTOR DEVICE WITH EXTRA SHORT GRID AND METHOD OF FABRICATION
4645957	685632	Granted	US	NORMALLY OFF SEMICONDUCTOR DEVICE WITH LOW ON-RESISTANCE AND CIRCUIT ANALOGUE
4598461	693643	Granted	US	SELF ALIGNED POWER MOSFET WITH INTERGRAL SOURCE-BASE SHORT AND METHODS FOR MAKING
4587712	692073	Granted	US	VERTICAL CHANNEL FIELD CONTROLLED DEVICE EMPLOYING A RECESSED GATE STRUCTURE AND METHOD FOR MAKING
4656493	698498	Granted	US	BIDIRECTIONAL HIGH SPEED POWER MOSFET DEVICES WITH DEEP LEVEL RECOMBINATION CENSORS IN BASE REGION
4937644	756478	Granted	US	ASYMMETRICAL FIELD CONTROLLED THYRISTOR
4823176	33952	Granted	US	(VDMOS) DEVICE INCL HI VOLT JUNCTION EXHIB INCREASE SAFE OP AREA
4801986	33940	Granted	US	VERTICAL DOUBLE DIFFUSED METAL OXIDE SEMI (VDMOS) DEVICE WITH INCREASED SAFE OP AREA AND METHOD
4720308	843346	Granted	US	METHOD FOR PRODUCING HIGH ASPECT RATIO HOLLOW DIFFUSED REGI
4816422	947151	Granted	US	FABRICATION OF LARGE POWER SEMICONDUCTOR COMPOSITE BY WAFER INTERCONNECTION OF INDIVIDUAL DEVICES
4801985	51359	Granted	US	IMPROVED MONLITHICALLY INTEGRATED SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATION
4769744	851275	Granted	US	SEMICONDUCTOR CHIP PACKAGES HAVING SOLDER LAYERS OF ENHANCED DURABILITY
4890143	225320	Granted	US	PROTECTIVE CLAMP FOR MOS GATED DEVICES
4857983	51430	Granted	US	MONOLITHICALLY INTEGRATED SEMICONDUCTOR DEVICE HAVING REVERSES CONDUCTING CAPAB & METHOD OF FABRICATION
4646129	872792	Granted	US	HERMETIC POWER CHIP PACKAGES
4799095	69806	Granted	US	METAL OXIDE SEMICONDUCTOR GATED TURN OFF THYRISTOR
4939101	240332	Granted	US	DIRECT-BONDED WAFERS HAVING A VOID FREE INTERFACE AND METHOD OF FABRICATION
4837606	14196	Granted	US	VERTICAL MOSFET WITH REDUCED BIPOLAR EFFECTS
4782379	40693	Granted	US	SEMICONDUCTOR DEVICE HAVING RAPID REMOVAL OF MAJORITY CARRI
4816892	36058	Granted	US	SEMICONDUCTOR DEVICE HAVING TURN-ON AND TURN-OFF CAPABILITI ES
4809047	98756	Granted	US	INSULATED-GATE SEMICONDUCTOR DEVICE WITH IMPROVED BASE-TO SOURCE ELECTRODE SHORT & METHOD OF FAB SAID SHORT
4883767	220353	Granted	US	METHOD OF FABRICATING SELF-ALIGNED SEMICONDUCTOR DEVICES
4677452	767052	Granted	US	POWER FIELD-EFFECT TRANSISTOR STRUCTURES
4597822	717364	Granted	US	METHOD FOR MAKING SILICON WAFERS
4505029	501745	Granted	US	SEMICONDUCTOR DEVICE WITH BUILT UP LOW RESISTANCE CONTACT
4809045	781381	Granted	US	INSULATED GATE DEVICE
4682195	781383	Granted	US	IMPROVED INSULATED GATE DEVICE
4641162	807597	Granted	US	CURRENT LIMITED INSULATED GATE DEVICE
4794432	7034	Granted	US	MOSFET STRUCTURE WITH SUBSTRATE COUPLED SOURCE
4803533	913785	Granted	US	IGT AND MOSFET DEVICES HAVING REDUCED CHANNEL WIDTH
4810665	77711	Granted	US	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION

EXHIBIT A

Pat #	Apl #	Status	Country	Title
4860080	32367	Granted	US	IMPROVED ISOLATION FOR TRANSISTOR DEVICES HAVING A PILOT STRUCTURE
4345266	236220	Granted	US	TRANSISTOR HAVING IMPROVED TURN OFF TIME AND SECOND BREAKDOWN CHARACERISTICS
4999684	07/435632	Granted	US	SYMMETRICAL BLOCKING HI VOLTAGE BREAKDOWN SEMI DEVICE AND METHOD OF FABRICATION
5041896	07/376073	Granted	US	SYMMETRICAL BLOCKING HIGH VOLTAGE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION
4941026	07/239014	Granted	US	SEMICONDUCTOR DEVICES EXHIBITING MINIMUM ON RESISTANCE
5082795	267757	Granted	US	METHOD OF FABRICATING A FIELD EFFECT SEMICONDUCTOR DEVICE HAVING A SELF ALIGNED STRUCTURE
5018002	07/375641	Granted	US	HI CURRENT HERMETIC PACKAGE INCL AN INTERNAL FOIL AND HAVING A LEAD EXTENDING THROUGH THE PACK LID AND PACK CHIP
5164802	07/672243	Granted	US	POWER VDMOSFET WITH SCHOTTKY ON LIGHTLY DOPED DRAIN OF LATERAL DRIVER FET
5097319	07/672997	Granted	US	COVER WITH THROUGH TERMINALS FOR A HERMETICALLY SEALED ELECTRONIC PACKAGE
4969028	07/492377	Granted	US	GATE ENHANCED RECTIFIER
4937467	411424	Granted	US	COMPLEMENTARY CIRCUIT AND STRUCTURE WITH COMMON SUBSTRATE
4460913	316660	Granted	US	FAST SWITCHING TRANSISTOR
4420765	268284	Granted	US	MULTI-LAYER PASSIVANT SYSTEM
4374455	351250	Granted	US	METHOD FOR MANUFACTURING A VERTICAL, GROOVED MOSFE
4455565	234834	Granted	US	VERTICAL MOSFET WITH AN ALIGNED GATE ELECTRODE AND
4433008	377197	Granted	US	DOPED-OXIDE DIFFUSION OF PHOSPHORUS USING BOROPHOS
4344985	248208	Granted	US	METHOD OF PASSIVATING A SEMICONDUCTOR DEVICE WITH
4586240	748940	Granted	US	VERTICAL IGFET WITH INTERNAL GATE AND METHOD FOR MAKING SAME
4549926	553305	Granted	US	METHOD FOR GROWING MONOCRYSTALLINE SILICON ON A MA
4578142	608544	Granted	US	METHOD FOR GROWING MONOCRYSTALLINE SILICON THROUGH
4639762	605427	Granted	US	MOSFET WITH REDUCED BIPOLAR EFFECTS
4605948	637027	Granted	US	SEMICONDUCTOR STRUCTURE FOR ELECTRIC FIELD DISTRIBUTION
4584028	653559	Granted	US	NEUTRALIZATION OF ACCEPTOR LEVELS IN SILICON BY AT
4639754	705371	Granted	US	VERTICAL MOSFET WITH DIMINISHED BIPOLAR EFFECTS
4661199	797126	Granted	US	METHOD TO INHIBIT AUTODOPING IN EPITAXIAL LAYERS
4910563	232243	Granted	US	COMPLEMENTARY CIRCUIT AND STRUCTURE WITH COMMON SUBSTRATE
5243211	07/797054	Granted	US	MOSFET WITH SHIELDED CHANNEL
5323036	07/822732	Granted	US	ATOMIC LATICED LAYOUT
5218220	07/789901	Granted	US	POWER FET HAVING REDUCED THRESHOLD VOLTAGE
4994883	07/416171	Granted	US	FIELD CONTROLLED DIODE (FCD) HAVING MOS TRENCH GATES
5293070	07/973603	Granted	US	INTEGRATED HEAT SINK FOR SEMICONDUCTOR MODULES
5422288	08/246307	Granted	US	METHOD OF DOPING A JFET REGION IN A MOS-GATED SEMICONDUCTOR DEVICE
5463344	08/051839	Granted	US	FAST TURN ON SWITCH CIRCUIT WITH PARALLEL MOS CONTROLLED THYRISTOR AND SILICON CONTROLLED THYRISTOR AND SILICON CONTROLLED RECTIFIER
5366932	51832	Granted	US	SEMICONDUCTOR CHIP HAVING INTERDIGITATED GATE RUNNERS WITH GATE BONDING PADS
5497013	08/276464	Granted	US	SEMICONDUCTOR CHIP HAVING INTERDIGITATED GATE RUNNERS WITH GATE BONDING PADS
5317184	07/973709	Granted	US	DEVICE AND METHOD FOR IMPROVING CURRENT CARRYING CAPABILITY IN A SEMICONDUCTOR DEVICE
5455442	08/375714	Granted	US	COMFET SWITCH AND METHOD
5594261	08/223425	Granted	US	METHOD AND DEVICE FOR ISOLATING PARALLEL SUB-ELEMENTS WITH REVERSE CONDUCTING DIODE REGIONS
5424563	08/173077	Granted	US	APPARATUS AND METHOD FOR INCREASING BREAKDOWN VOLTAGE RUGGEDNESS IN SEMICONDUCTOR DEVICES
5399892	08/158444	Granted	US	METHOD OF FORMING MOS-GATED SEMICONDUCTOR DEVICES HAVING MESH GEOMETRY PATTERN

EXHIBIT A

Pat #	Apl #	Status	Country	Title
5468668	08/368612	Granted	US	METHOD OF FORMING MOS-GATED SEMICONDUCTOR DEVICES HAVING MESH GEOMETRY PATTERN
5654226	08/305435	Granted	US	WAFER BONDING FOR POWER DEVICES
5880513	08/634371	Granted	US	ASYMMETRIC SNUBBER RESISTOR
	08/494394	Pending	US	MEGASONIC PLL POWER GENERATOR
5789982	08/712562	Granted	US	LOW DISTORTION FEEDBACK IC AMPLIFIER AND METHOD
5694417	08/509590	Granted	US	SHORT BURST DIRECT ACQUISITION DIRECT SEQUENCE SPREAD SPECTRUM RECEIVER
5770878	08/636904	Granted	US	TRENCH MOS GATE DEVICE
	09/096217	Pending	US	TRENCH MOS GATE DEVICE
5913130	08/662118	Granted	US	METHOD FOR FABRICATING A POWER DEVICE
6078077	09/330437	Granted	US	METHOD FOR FABRICATING A POWER DEVICE
	09/542561	Pending	US	METHOD FOR FABRICATING A POWER DEVICE
	09/358625	Pending	US	DOUBLY GRADED JUNCTION TERMINATION EXTENSION (JTE) FOR EDGE PASSIVATION OF SEMICONDUCTOR DEVICES
	09/098517	Pending	US	HIGH PERFORMANCE HEAT EXCHANGER AND METHOD
	09/570009	Pending	US	HIGH PERFORMANCE HEAT EXCHANGER AND METHOD
6110799	08/885879	Granted	US	A NOVEL TRENCH MOSFET PROCESS
6037628	08/885922	Granted	US	A NOVEL TRENCH MOSFET PROCESS
	09/498476	Pending	US	A NOVEL TRENCH MOSFET PROCESS
5872028	08/708712	Granted	US	METHOD OF FORMING POWER SEMICONDUCTOR DEVICES WITH CONTROLLABLE INTEGRATED BUFFER
6110763	08/861562	Granted	US	ONE MASK POWER SEMICONDUCTOR FABRICATION PROCESS
5940689	08/885921	Granted	US	METHOD OF FABRICATING UMOS SEMICONDUCTOR DEVICES USING A SELF-ALIGNED, REDUCED MASK PROCESS
6054369	08/885878	Granted	US	IMPROVED LIFETIME CONTROL FOR SEMICONDUCTOR DEVICES
5894141	08/885227	Granted	US	BIPOLAR SEMICONDUCTOR POWER CONTROLLING DEVICES WITH HETEROJUNCTION
	08/885228	Pending	US	SEMICONDUCTOR DEVICE GATE STRUCTURE FOR THERMAL OVERLOAD PROTECTION
	09/338891	Pending	US	SEMICONDUCTOR DEVICE GATE STRUCTURE FOR THERMAL OVERLOAD PROTECTION
6081009	08/966867	Granted	US	HIGH VOLTAGE MOSFET STRUCTURE
6066878	09/108962	Granted	US	HIGH VOLTAGE MOSFET STRUCTURE
5877041	08/884726	Granted	US	CARBIDE
5877044	08/814842	Granted	US	METHOD OF MAKING MOS-GATED SEMICONDUCTOR DEVICES
5970343	08/133030	Granted	US	FABRICATION OF CONDUCTIVITY ENHANCED MOS-GATED SEMICONDUCTOR DEVICES
	09/114769	Pending	US	CONDUCTIVITY ENHANCED MOS-GATED SEMICONDUCTOR DEVICES
6188575	09/107273	Granted	US	HEAT EXCHANGING CHASSIS AND METHOD
	09/649815	Pending	US	HEAT EXCHANGING CHASSIS AND METHOD
	09/649837	Pending	us	HEAT EXCHANGING CHASSIS AND METHOD
5920452	09/088198	Granted	US	CIRCUIT AND METHOD FOR PROTECTING FROM OVERCURRENT CONDITIONS AND DETECTING AN OPEN ELECTRICAL LOAD
	09/350575	Pending	US	PROCESS FOR FORMING VERTICAL SEMICONDUCTOR DEVICE HAVING INCREASED SOURCE CONTACT AREA
6069403	09/167203	Granted	US	POWER MODULE WITH LOWERED INDUCTANCE AND REDUCED VOLTAGE OVERSHOOTS
6140152	09/334098	Granted	US	POWER MODULE WITH LOWERED INDUCTANCE AND REDUCED VOLTAGE OVERSHOOTS
6107127	09/145513	Granted	US	METHOD OF MAKING SHALLOW WELL MOSFET STRUCTURE
6055149	09/203700	Granted	US	CURRENT LIMITED, THERMALLY PROTECTED, POWER DEVICE
	09/167177	Pending	US	PROCESS FOR FORMING HIGH VOLTAGE JUNCTION TERMINATION EXTENSION OXIDE
	09/307879	Pending	US	PROCESS FOR FORMING MOS-GATED DEVICES HAVING SELF-ALIGNED TRENCHES
6121089	09/092334	Granted	US	METHODS OF FORMING POWER SEMICONDUCTOR DEVICES HAVING MERGED SPLIT-WELL BODY REGIONS THEREIN AND DEVICES FORMED THEREBY

EXHIBIT A

Pat #	Apl #	Status	Country	Title
	09/344867	Pending	US	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A MULTIPLE PASS CONFIGURATION
	09/663235	Pending	US	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A MULTIPLE PASS CONFIGURATION
6077744	09/255092	Granted	US	SEMICONDUCTOR TRENCH MOS DEVICES
	09/037723	Pending	US	METHODS FOR MAKING SEMICONDUCTOR DEVICES BY LOW TEMPERATURE DIRECT BONDING
	09/296472	Pending	US	FAST TURN-OFF POWER SEMICONDUCTOR DEVICES
6153495	09/036815	Granted	US	ADVANCED METHODS FOR MAKING SEMICONDUCTOR DEVICES BY LOW TEMPERATURE DIRECT BONDING
	09/036838	Pending	US	DEVICES FORMABLE BY LOW TEMPERATURE DIRECT BONDING
6137139	09/324553	Granted	US	LOW VOLTAGE DUAL-WELL MOS DEVICE HAVING HIGH RUGGEDNESS, LOW ON-RESISTANCE, AND IMPROVED BODY DIODE REVERSE RECOVERY
6104062	09/107721	Granted	US	SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS
	09/551187	Pending	US	SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS
6162702	09/334835	Granted	US	SELF-SUPPORTING ULTRATHIN SILICON WAFER PROCESS
	09/303270	Pending	US	POWER MOS DEVICE WITH INCREASED CHANNEL WIDTH AND PROCESS FOR FORMING SAME
	09/765177	Pending	US	POWER MOS DEVICE WITH INCREASED CHANNEL WIDTH AND PROCESS FOR FORMING SAME
	09/450872	Pending	US	EMITTER BALLAST RESISTOR WITH ENHANCED BODY EFFECT TO IMPROVE THE SHORT CIRCUIT WITHSTAND CAPABILITY OF POWER DEVICES
	09/339356	Pending	US	BACKMETAL DRAIN TERMINAL WITH LOW STRESS AND THERMAL RESISTANCE
6188105	09/283531	Granted	US	HIGH DENSITY MOS-GATED POWER DEVICE AND PROCESS FOR FORMING SAME
	09/260411	Pending	US	MOS-GATED DEVICE HAVING A BURIED GATE AND PROCESS FOR FORMING SAME
	09/318334	Pending	US	TRENCH-GATED DEVICE HAVING TRENCH WALLS FORMED BY SELECTIVE EPITAXIAL GROWTH AND PROCESS FOR FORMING DEVICE
	09/314323	Pending	US	MOS-GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME
	09/726682	Pending	US	MOS-GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME
	09/345930	Pending	US	POWER SEMICONDUCTOR MOUNTING PACKAGE CONTAINING BALL GRID ARRAY
	09/525182	Pending	US	POWER TRENCH TRANSISTOR DEVICE SOURCE REGION FORMATION USING SILICON SPACER
	09/624533	Pending	US	POWER MOS DEVICE WITH BURIED GATE
	09/654845	Pending	US	POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY
	09/718219	Pending	US	PROCESS FOR CONTROLLING LIFETIME IN A P-I-N DIODE AND FOR FORMING DIODE WITH IMPROVED LIFETIME CONTROL
	09/689939	Pending	US	MOS-GATED POWER DEVICE HAVING SEGMENTED TRENCH AND EXTENDED DOPING ZONE AND PROCESS FOR FORMING SAME
	09/502712	Pending	US	MOS-GATED DEVICE HAVING ALTERNATING ZONES OF CONDUCTIVITY
	09/665,850	Pending	US	SELF-ALIGNED PROCESS FOR FABRICATING POWER MOSFET WITH SPACER-SHAPED TERRACED GATE
	09/603605	Pending	US	SOFT RECOVERY POWER DIODE AND RELATED METHOD
	60/198692	Pending	US	QUASI-RESONANT CONVERTER
	09/664024	Pending	US	INTEGRATED CIRCUIT DEVICE INCLUDING A DEEP WELL REGION AND ASSOCIATED METHODS

EXHIBIT A

Pat #	Apl #	Status	Country	Title
	60/219858	Pending	US	PRODUCED BY USING A FULLY SELF-ALIGNED BODY IMPLANT PROCESS
4994871	07/279392	Granted	US	INSULATED GATE BIPOLAR TRANSISTOR WITH IMPROVED LATCHUP CURRENT LEVEL AND SAFE OPERATING AREA
5134321	07/644569	Granted	US	POWER MOSFET AC POWER SWITCH EMPLOYING MEANS FOR PREVENTING CONDUCTION OF BODY DIODE
4634473	773772	Granted	US	METHOD FOR FABRICATING A RADIATION HARDENED OXIDE HAVING STRUCTURAL DAMAGE
4998151	337684	Granted	US	POWER FIELD EFFECT DEVICES HAVING SMALL CELL SIZE AND LOW CONTACT RESISTANCE AND METHOD OF FABRICATION
4587713	582601	Granted	US	METHOD FOR MAKING VERTICAL MOSFET WITH REDUCED BIPOLAR EFFECTS
4648174	698495	Granted	US	METHOD OF MAKING HIGH BREAKDOWN VOLTAGE SEMICONDUCTOR DEVICE
4927772	358057	Granted	US	HIGH BREAKDOWN VOLTAGE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION
4675978	773771	Granted	US	METHOD FOR FABRICATING A RADIATION HARDENED OXIDE
6080614	08/885877	Granted	US	METHOD OF MAKING A MOS-GATED SEMICONDUCTOR DEVICE WITH A SINGLE DIFFUSION
	09/449487	Pending	US	METHOD OF MAKING A MOS-GATED SEMICONDUCTOR DEVICE WITH A SINGLE DIFFUSION
	60/234563	Pending	US	CONTROLLING SILICON TRENCH PROFILES BY INCREMENTAL INCREASES IN OXYGEN FLOWS
5103290	07/367525	Granted	US	HERMETIC PACKAGE HAVING A LEAD EXTENDING THROUGH AN APERTURE IN THE PACKAGE LID AND PACKAGED SEMICONDUCTOR CHIP
5446316	08/217801	Granted	US	METHOD OF PACKAGING A SEMICONDUCTOR DEVICE
5577656	08/462856	Granted	US	METHOD OF PACKAGING A SEMICONDUCTOR DEVICE
5473193	08/177974	Granted	US	PACKAGE FOR PARALLEL SUBELEMENT SEMICONDUCTOR DEVICES
	08/759865	Pending	US	A METHOD OF METALIZING A SEMICONDUCTOR POWER DEVICE CERAMIC MEMBER
5995349	08/944513	Granted	US	PROTECTION DEVICE FOR SOLID STATE SWITCHED POWER ELECTRONICS
6060795	09/040112	Granted	US	SEMICONDUCTOR POWER PACK

Exhibit A

Pat#	Apl#	Status	Country	Title
4545109	459756	Granted	US	METHOD OF MAKING A GALLIUM ARSENIDE FIELD EFFECT TRANSISTOR
4516143	579229	Granted	US	SELF-ALIGNED POWER MOSFET WITH INTEGRAL SOURCE BASE SHORT A
4567641	650314	Granted	US	METHOD OF FABRICATING SEMI-CONDUCTOR DEVICE HAVING A DIFFUSED REGION OF REDUCED LENGTH
	449321	Pending	US	LATERAL INSULATED GATE RECTIFIER STRUCTURES
	449322	Pending	US	BIDIRECTIONAL INSULATED GATE RECTIFIER STRUCTURES AND METHOD
	464161	Granted	US	BIDIRECTIONAL INSULATED GATE RECTIFIER STRUCTURES AND METHOD
4862242	807612	Granted	US	SEMICONDUCTOR WAFER WITH AN ELECTRICALLY ISOLATED SEMICONDUCTOR
	726749	Pending	US	INSULATED GATE SEMICONDUCTOR DEVICE
4516143	579229	Granted	US	SELF-ALIGNED POWER MOSFET WITH INTEGRAL SOURCE-BASE SHORT AND METHODS OF MAKING
4595428	567708	Granted	US	METHOD FOR PRODUCING HIGH ASPECT RATIO HOLLOW DIFFUSED REGIONS IN A SEMICONDUCTOR BODY AND DIODE PRODUCED THEREBY
4546375	439563	Granted	US	VERTICAL IGFET WITH INTERNAL GATE AND METHOD FOR MAKING SAME
	09/829,634	Pending	US	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A MULTIPLE PASS CONFIGURATION
	09/799,845	Pending	US	POWER TRENCH TRANSISTOR DEVICE SOURCE REGION FORMATION USING SILICON SPACER
	09/839,374	Pending	US	QUASI-RESONANT CONVERTER
	09/815,672	Pending	US	EDGE TERMINATION FOR SILICON POWER DEVICES
	09/844,347	Pending	US	POWER MOSFET AND METHOD FOR FORMING SAME USING A SELF-ALIGNED BODY IMPLANT
	08/310,041	Pending	US	FET, IGBT AND MCT STRUCTURES TO ENHANCE OPERATING CHARACTER
5577656	462856	Granted	US	METHOD OF PACKAGING A SEMICONDUCTOR DEVICE
	09/731,169	Pending	US	MOS-GATED POWER DEVICE WITH DOPED POLYSILICON BODY AND PROCESS FOR FORMING SAME