

05-28-2002

Form PTO-1595

(Rev. 03/01)

5-24-02 RE

OMB No. 0651-0027 (exp. 5/31/2002)

Tab settings ⇌ ⇌ ⇌ ▼

102101603 ▼ ▼ ▼

U.S. DEPARTMENT OF COMMERCE  
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

## 1. Name of conveying party(ies):

IN-CHIP SYSTEMS, INC.

## 2. Name and address of receiving party(ies)

Name: DR. TUSHAR GHEEWALA

Internal Address: \_\_\_\_\_

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

## 3. Nature of conveyance:



Assignment



Merger



Security Agreement



Change of Name



Other \_\_\_\_\_

Street Address: 501 CASTANO CORTE

City: LOS ALTOS

State: CA

Zip: 94022

Execution Date: MAY 17, 2002

Additional name(s) & address(es) attached? ☐ Yes ☒ No

## 4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: \_\_\_\_\_

A. Patent Application No.(s)

SEE SCHEDULE 1 ATTACHED.

B. Patent No.(s)

5723883

SEE ACHEDULE 1 ATTACHED.

Additional numbers attached? ☒ Yes ☐ No

## 5. Name and address of party to whom correspondence concerning document should be mailed:

Name: JACKIE LEE

Internal Address: ACCESS INFORMATION SERVICES, INC.

Street Address: 1773 WESTERN AVENUE

City: ALBANY State: NY Zip: 12203

## 6. Total number of applications and patents involved: 10

7. Total fee (37 CFR 3.41).....\$ 400.00



Enclosed



Authorized to be charged to deposit account

## 8. Deposit account number:

(Attach duplicate copy of this page if paying by deposit account)

## DO NOT USE THIS SPACE

## 9. Statement and signature.

*To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.*

Jackie Lee

Name of Person Signing

Jackie Lee

Signature

5-22-02

Date

Total number of pages including cover sheet, attachments, and documents: 6

05/28/2002 GTOM11 00000187 5723883

Mail documents to be recorded with required cover sheet information to:

Commissioner of Patents & Trademarks, Box Assignments  
Washington, D.C. 20231

01 FC:581

400.00 OP

02 FC:584

120.00 OP

PATENT  
REEL: 012735 FRAME: 0281

**Schedule 1  
to Patent Security Agreement**

**IN-CHIP SYSTEMS, INC.**

**PATENTS**

Patent No.	Issue Date	Country	Title
5723883	3/3/98	U.S.	Gate Array Cell Architecture & Routing Scheme
5923059	7/13/99	U.S.	Integrated Circuit Cell Architecture & Routing Scheme
5898194	4/27/99	U.S.	Integrated Circuit Cell Architecture & Routing Scheme
5923060	7/13/99	U.S.	Reduced Area Gate Array Cell Design Based on Shifted Placement of Alternate Rows of Cells
6091090	7/18/00	U.S.	Power & Signal Routing Technique for Gate Array Design

**PATENT APPLICATIONS**

Case No.	Application No.	Country	Date	Filing Title
14737-000300	60/027387	U.S.	09/27/96	Reduced Area Gate Array Cell Design Based on Shifted Placement of Alternate Rows of Cells
14737-000400	60/027448	U.S.	09/27/96	New Power and Signal Routing Technique to Achieve a Higher Density Core Cell for CMOS Gate Array Applications
14737-001000	09/351767	U.S.	07/12/99	Dual-Height Cell with Variable Width Power Rail Architecture
14737-001100	09/588804	U.S.	06/06/00	Routing Driven, Metal Programmable Integrated Circuit Architecture with Multiple Types of Core Cells
14737-001200	09/588802	U.S.	06/06/00	Gate Array Architecture Using Elevated Metal Levels for Customization

**PATENT SECURITY AGREEMENT**

**(Patents and Patent Applications)**

WHEREAS, In-Chip Systems, Inc. (herein referred to as the "**Debtor**") owns the Patent Collateral (as defined below);

WHEREAS, pursuant to a Security Agreement dated as of May 17, 2002 (as amended and/or supplemented from time to time, the "**Security Agreement**") between the Debtor and the GHEEWALA 1990 REVOCABLE TRUST, Reeta Gheewala and Tushar Gheewala, Co-Trustees (together with his successors and assigns, the "**Grantee**"), the Debtor has granted and/or is granting to the Grantee a continuing security interest in personal property of the Debtor, including all right, title and interest of the Debtor in, to and under the Patent Collateral (as defined below), to secure the Debtor's Secured Obligations (as defined in the Security Agreement);

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Debtor grants to the Grantee, to secure the Debtor's Secured Obligations, a continuing security interest in all of the Debtor's right, title and interest in, to and under the following (all of the following items or types of property being herein collectively referred to as the "**Patent Collateral**"), whether now owned or existing or hereafter acquired or arising:

(i) each Patent (as defined in the Security Agreement) owned by the Debtor which is the subject of an application or has been issued or registered, including, without limitation, each Patent referred to in Schedule 1 hereto; and

(i) all proceeds of and revenues from the foregoing, including, without limitation, all proceeds of and revenues from any claim by the Debtor against third parties for past, present or future infringement of any Patent owned by the Debtor (including, without limitation, any Patent identified in Schedule 1 hereto).

The Debtor irrevocably constitutes and appoints the Grantee and any officer or agent thereof, with full power of substitution, as its true and lawful attorney-in-fact with full power and authority in the name of the Debtor or in the Grantee's name, from time to time, in the Grantee's discretion, so long as any Event of Default (as defined in the Security Agreement) shall have occurred, to take with respect to the Patent Collateral any and all appropriate action which the Debtor might take with respect to the Patent Collateral and to execute any and all

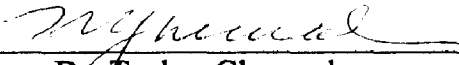
documents and instruments which may be necessary or desirable to carry out the terms of this Patent Security Agreement and to accomplish the purposes hereof.

Except to the extent expressly permitted in the Security Agreement, the Debtor agrees not to sell, license, exchange, assign or otherwise transfer or dispose of, or grant any rights with respect to, or mortgage or otherwise encumber, any of the Patent Collateral.

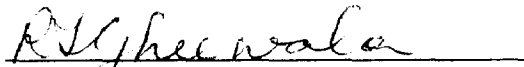
The foregoing security interest is granted in conjunction with the security interests granted by the Debtor to the Grantee pursuant to the Security Agreement. The Debtor acknowledges and affirms that the rights and remedies of the Grantee with respect to the security interest in the Patent Collateral granted hereby are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein.

IN WITNESS WHEREOF, the parties have caused this Agreement to be executed themselves or by their respective representatives thereunto duly authorized the day and year first above written.

**IN-CHIP SYSTEMS, INC.**

By:   
Name: Dr. Tushar Gheewala  
Title: President and Chief  
Executive Officer

**GHEEWALA 1990 REVOCABLE  
TRUST, Reeta Gheewala and Tushar  
Gheewala, Co-Trustees**

By:   
Reeta Gheewala, Co-Trustee

By:   
Dr. Tushar Gheewala, Co-Trustee

**Schedule 1  
to Patent Security Agreement**

**IN-CHIP SYSTEMS, INC.**

**PATENTS**

Patent No.	Issue Date	Country	Title
5723883	3/3/98	U.S.	Gate Array Cell Architecture & Routing Scheme
5923059	7/13/99	U.S.	Integrated Circuit Cell Architecture & Routing Scheme
5898194	4/27/99	U.S.	Integrated Circuit Cell Architecture & Routing Scheme
5923060	7/13/99	U.S.	Reduced Area Gate Array Cell Design Based on Shifted Placement of Alternate Rows of Cells
6091090	7/18/00	U.S.	Power & Signal Routing Technique for Gate Array Design

**PATENT APPLICATIONS**

Case No.	Application No.	Country	Date	Filing Title
14737-000300	60/027387	U.S.	09/27/96	Reduced Area Gate Array Cell Design Based on Shifted Placement of Alternate Rows of Cells
14737-000400	60/027448	U.S.	09/27/96	New Power and Signal Routing Technique to Achieve a Higher Density Core Cell for CMOS Gate Array Applications
14737-001000	09/351767	U.S.	07/12/99	Dual-Height Cell with Variable Width Power Rail Architecture
14737-001100	09/588804	U.S.	06/06/00	Routing Driven, Metal Programmable Integrated Circuit Architecture with Multiple Types of Core Cells
14737-001200	09/588802	U.S.	06/06/00	Gate Array Architecture Using Elevated Metal Levels for Customization