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102120878

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2/27/02

1. Name of conveying party(ies):
PRASAN K. PAI

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3. Nature of conveyance:
☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☑ Other AFFIDAVIT OF INVENTION MADE WHILE EMPLOYED

Execution Date: FEB 22 '02

2. Name and address of receiving party(ies)
Name: CONEXANT SYSTEMS, INC.
Internal Address:
Street Address: 4311 JAMBOREE ROAD
City: Newport Beach State: CA Zip: 92660-3095
Additional name(s) & address(es) attached? ☐ Yes ☑ No

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is:
A. Patent Application No.(s) 10/004,909
B. Patent No.(s)
Additional numbers attached? ☐ Yes ☑ No

5. Name and address of party to whom correspondence concerning document should be mailed:
Name: FRANCISCO A. RUBIO-CAMPOS
Internal Address:
SONNENSCHEIN NATH & ROSENTHAL
Street Address: P.O. BOX 061080
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City: CHICAGO State: IL Zip: 60606

6. Total number of applications and patents involved: 1
7. Total fee (37 CFR 3.41).....$ 40.00
☑ Enclosed
☐ Authorized to be charged to deposit account
8. Deposit account number:
19-3140 Fee Pd

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9. Signature.

VINCENT P. TASSINARI
Name of Person Signing

Signature

FEBRUARY 27, 2002
Date

Total number of pages including cover sheet, attachments, and document: 11

Mail documents to be recorded with required cover sheet information to:
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: Hiok-Nam TAY
ATTORNEY DOCKET NO.: 50047050-0004
SERIAL NO.: 10/004,909 GROUP ART UNIT: 2816
FILED: November 2, 2001 EXAMINER:
TITLE: **SWITCHED CAPACITOR COMPARATOR NETWORK**

AFFIDAVIT OF INVENTION MADE WHILE EMPLOYED

I, **Prasan K. Pai**, (herein after 'I', 'my', or 'Affiant'), upon information and belief do solemnly and sincerely declare and say as follows:

That at the time Hiok-Nam Tay was employed by Conexant Systems, Inc., my relationship to Hiok-Nam Tay was that of supervisor in that Hiok-Nam Tay reported directly to me.

That I have reviewed and understand the contents of the Conexant Systems, Inc. Employment Agreement signed by Hiok-Nam Tay on November 22, 1999. I understand that by signing this Employment Agreement, Hiok-Nam Tay agreed to, among other things, assign to Conexant Systems, Inc. all inventions made during his employment with Conexant Systems, Inc. subject to the requirements of law.

That I have reviewed and understand the contents of the above-identified patent application, including the claims.

That I have firsthand knowledge of the facts that the invention of the above-identified patent application was made by Hiok-Nam Tay during the employment of Hiok-Nam Tay by Conexant Systems, Inc.

That the attached eight page invention disclosure statement was prepared by Hiok-Nam Tay during the employment of Hiok-Nam Tay by Conexant Systems, Inc. and was submitted by Mr. Tay to Conexant Systems, Inc. during the employment of Hiok-Nam Tay by Conexant Systems, Inc.

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name/Title: Prasan K. Pai, Director, Technology Planning

Signature: Prasan Kumar Pai

Date: Feb. 22, 2002

Post Office Address:

Conexant Systems, Inc.
4311 Jamboree Road, M/S E08-802
Newport Beach, California 92660-3095
United States of America

INDIVIDUAL ACKNOWLEDGEMENT
COUNTY OF ORANGE, STATE OF CALIFORNIA

On the ____ day of _____ 2002 before me personally appeared **Prasan K. Pai** known to me or proved to me on the basis of satisfactory evidence to be the individual described in and who acknowledged the foregoing instrument and swore and acknowledged that he executed the same as his free act and deed.

Notary Public: _____

My Commission Expires _____

See California All-purpose Acknowledgement dated 2/22/02

CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

State of California

County of Orange

On February 22, 2002 (Date) before me, Robert C. Winder, Notary Public (Name and Title of Officer (e.g., "Jane Doe, Notary Public"))

personally appeared Prasan Pai (Name(s) of Signer(s))

~~☐ personally known to me~~

☒ proved to me on the basis of satisfactory evidence

to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/~~her/their~~ authorized capacity(~~ies~~), and that by his/~~her/their~~ signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

ROBERT C. WINDER
Commission # 1279930
Notary Public - California
Orange County
My Comm. Expires Mar 31, 2005

WITNESS my hand and official seal.

Robert C. Winder
Signature of Notary Public

OPTIONAL

Though the information below is not required by law, it may prove valuable to persons relying on the document and could prevent fraudulent removal and reattachment of this form to another document.

Description of Attached Document

Title or Type of Document: Affidavit of Invention Made While Employed

Document Date: 2/22/02 Number of Pages: 1

Signer(s) Other Than Named Above: None

Capacity(ies) Claimed by Signer(s)

Signer's Name: Prasan Pai

☒ Individual
~~☐ Corporate Officer~~
~~Title(s):~~
~~☐ Partner — ☐ Limited ☐ General~~
~~☐ Attorney-in-Fact~~
~~☐ Trustee~~
~~☐ Guardian or Conservator~~
~~☐ Other:~~

RIGHT THUMBPRINT OF SIGNER
Top of thumb here

Signer Is Representing:

Signer's Name:

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Title(s):
☐ Partner — ☐ Limited ☐ General
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Signer Is Representing:

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Docket No.: 00CXT0610I
Ranking: NEED INFO

1. Title of Innovation

Switched-capacitor Comparator Network

2. Division/platform Information

Personal Imaging Division

3. Innovator(s)

Name	Innovator Information	
Hiok-Nam Tay	Personal Information : Home Address : 6 Mount Vernon State : CA Phone : 7148386207 Country of Domicile : US	City : Irvine Zip : 92620 Fax : Citizenship : US
	Conexant Contact Information : Address : 4311 Jamboree RoadP. O. Box C, State : CA Phone : 949-483-5947 Email : hioknam.tay@conexant.com Mail Code : K03-350	City : Newport Beach Zip : 92660-3095 Fax : Dept. : 039-871- Supervisor : Mr. Prasan Pal

4. Problem Solved

Conventional flash ADC uses a resistor string with multiple taps or multiple single-tap resistor strings, each tap being at a unique threshold voltage and connected to a comparator. For example, a 2-bit flash ADC requires 3 comparators and thus either a 3-tap resistor string or 3 single-tap resistor strings. A 1.5-bit flash ADC (such as used in pipeline ADCs) requires 2 comparators and thus either a 2-tap resistor string or 3 single-tape resistor strings.

Two low-impedance DC reference voltage sources are required to drive the terminals of those resistors. For high speed comparator operation, the resistor values need to be small to reduce settling time of the kick-back transients when the comparators are simultaneously switched into the comparison phase.

There are 3 problems associated with the above:

1. 2 reference voltages need be used. These need to have low impedance, so typically each requires a large off-chip capacitor, thus taking up extra pins as well as incur more board space and component cost.
2. High power consumption. DC current is drawn across all the resistors. The power consumption is especially

high for high-speed operation, because the resistor values are smaller.
3. Cross-coupling among multiple comparators through the shared reference voltages.

The problems are classical.

5. Previous Solutions

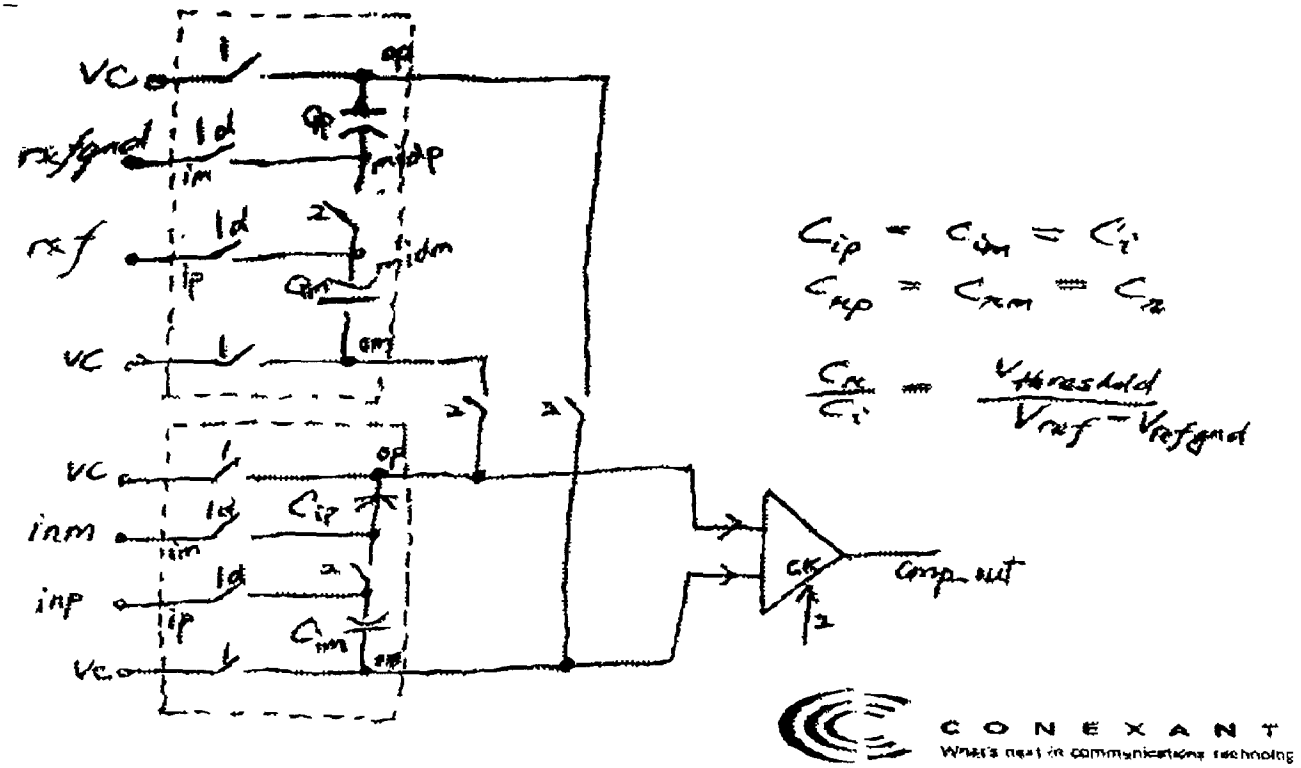
I do not know of any prior solution.

6. Solution

The central idea of this invention is to use capacitor charge sharing to perform arithmetic subtraction between the sampled input signal level and a fraction of the reference level.

During sampling phase, input signal is sampled onto a pair of differential input sampling capacitors. At the same time, reference voltage is sampled onto a similar pair of differential sampling capacitors. The capacitance ratio of the input sampling capacitors to the reference capacitors is equal to the ratio of the desired comparator threshold level to the reference level. During comparison phase, both pairs of capacitors are connected together in cross-coupled fashion, so that charge sharing occurs. The resultant voltage after settling is effectively the difference between the input voltage and the threshold voltage.

To cancel the effect of switch charge injection, during sampling phase the top plates of those capacitors are connected to their respective signals, whereas the bottom plates are connected to a common-mode reference node (named VC), typically connected to a big capacitor off-chip to bypass the sampling transients. During comparison phase, the top plates of the input-sampling capacitors are disconnected from the common-mode reference VC and another switch turns on to short out both top plates, and similarly the reference capacitors. Furthermore, the bottom plates of each pair are disconnected from VC and subsequently bottom plates of different capacitor pairs are connected in cross-coupled fashion.



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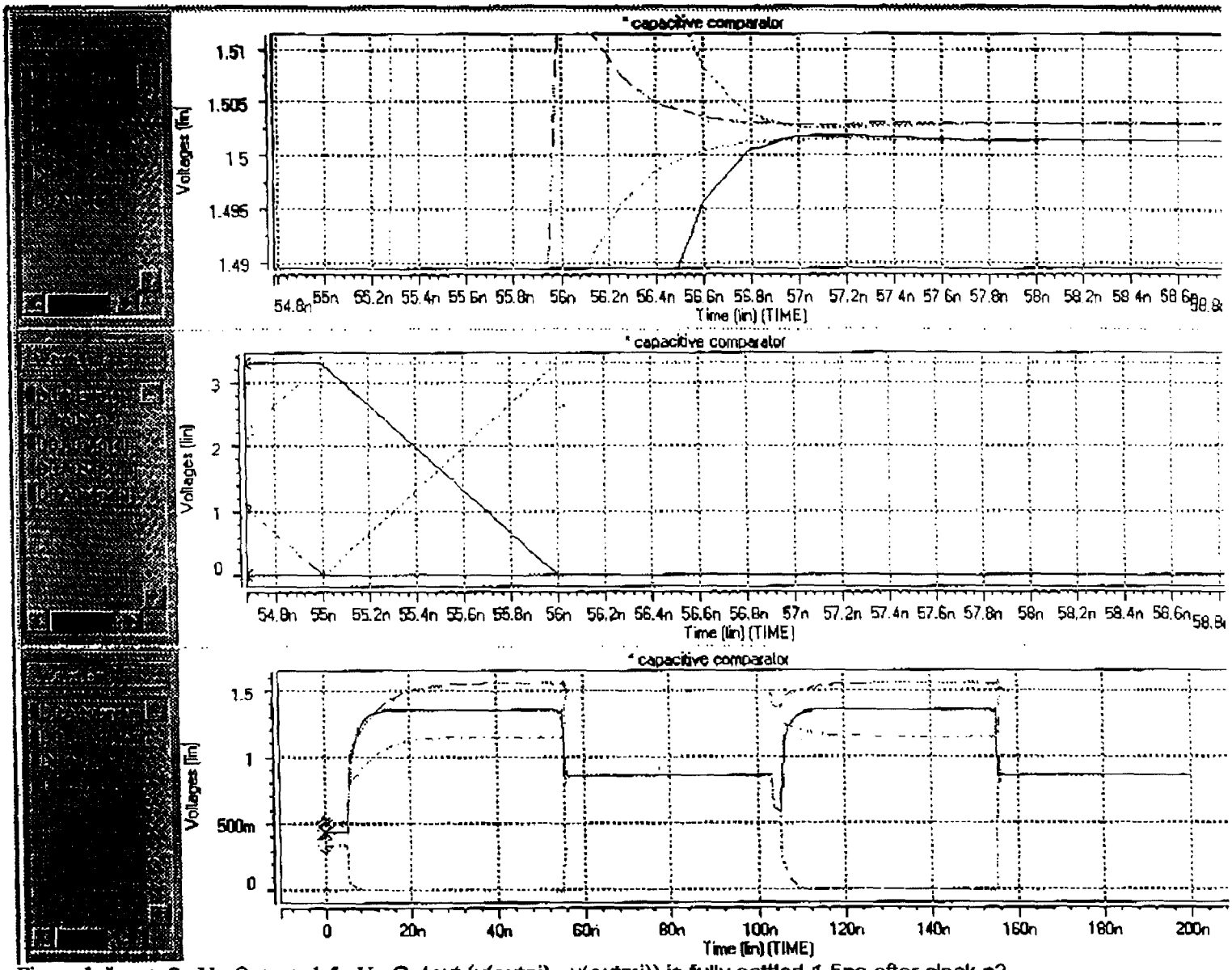


Figure 1 Input -2mV. Output -1.5mV. Output (v(outpi) - v(outmi)) is fully settled 1.5ns after clock p2.

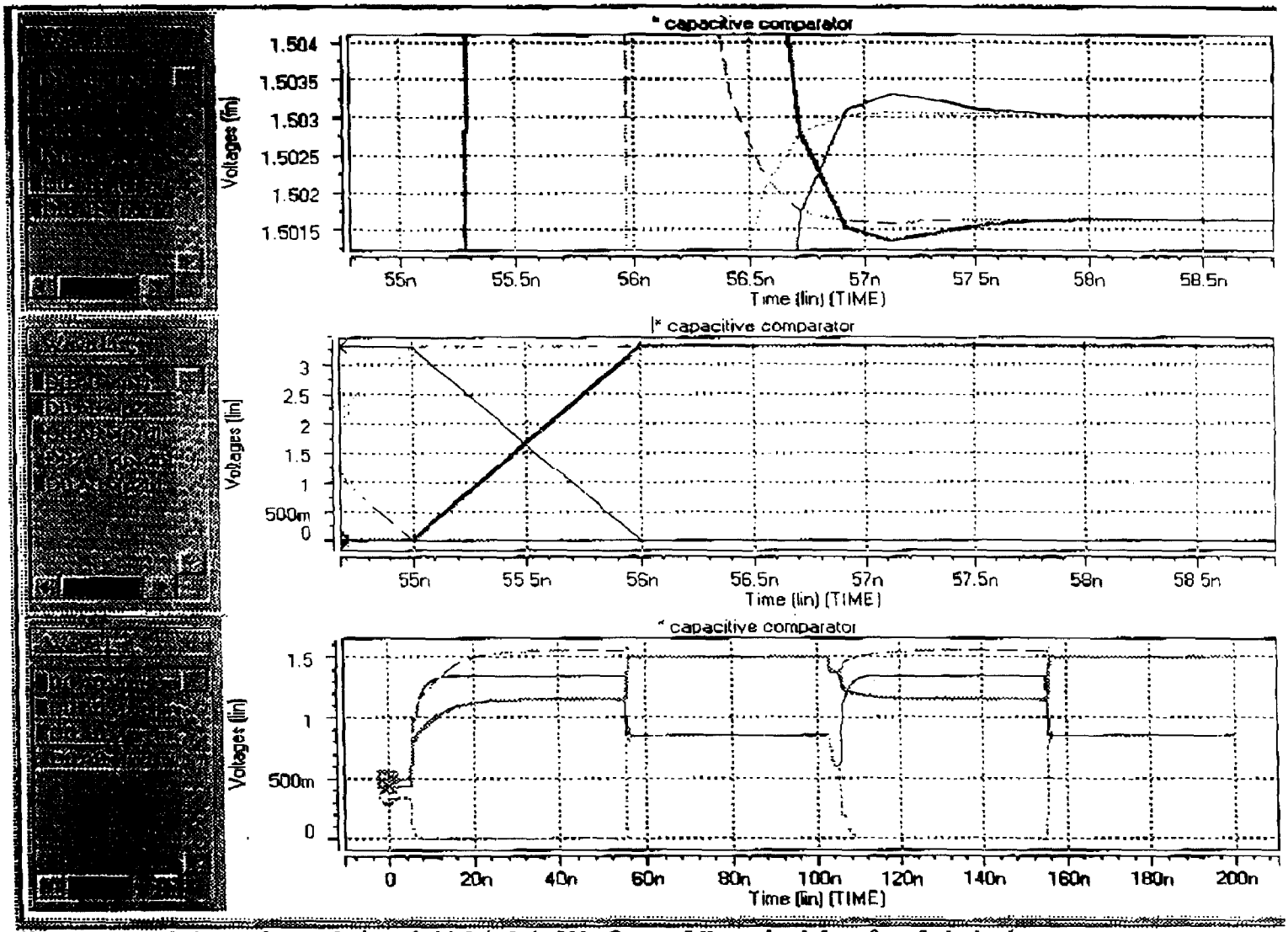


Figure 2 Input is 2mV. Output during p2=high is 1.5mVd. Output fully settles 1.5ns after p2 clock edge.

7. Differences/Advantages Over Previous Solutions

1. Only one single reference voltage need be used.
2. Low power. No need to use low-resistance resistor between two DC reference voltages to generate arbitrary threshold voltage. Especially important for high-speed comparators such as those used in 40MSps pipeline ADCs.
3. No cross-coupling among multiple comparators through the shared reference voltages (as when used in a multi-bit flash ADC) as in the case of resistor-divider threshold generation for conventional comparators, because the switched-capacitor network is disconnected from the reference signal during comparison phase.

8. Status of Innovation

In design If "Other", please specify

9. Product or program in which innovation will be used:

Products Used :	Technology Used :
Digital Imaging	CMOS Imager
If other, please specify :	**If other, please specify :**

Additional Information :	

10. Has anyone disclosed or does anyone plan to disclose your innovation outside the Company?

○ Yes ● No ○ Don't Know

11. Has anyone proposed or does anyone plan to propose a product or program to a customer which includes your innovation?

● Yes ○ No ○ Don't Know

12. Innovator signature(s): (Do not use black ink)

_____ **Date :** _____
(HIOK-NAM TAY)

Qtr Evaluated: 3Q00
Group: Personal Imaging Division
Technology:
Sub Technology 1:
Sub Technology 2:

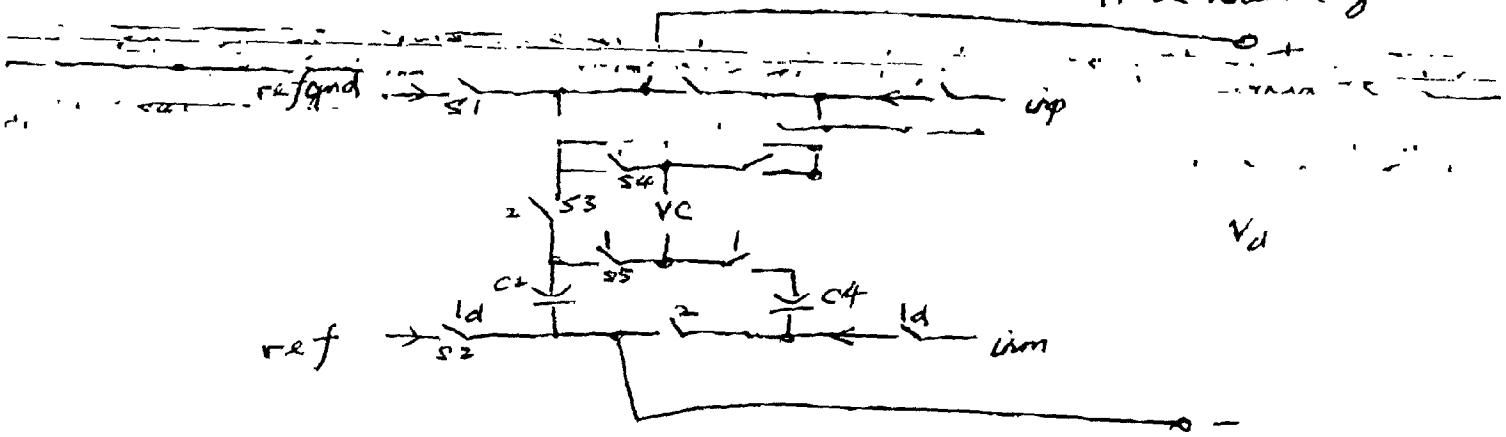
Products:
Innovation Block:

Entered: Hiok-Nam Tay @ 06/04/2000 08:17:50 PM
Modified: James K Dawson @ 11/27/2000 03:13 PM

Capacitive Network for 1-bit Comparator

June 1, 2000

Hiok Nam Tay

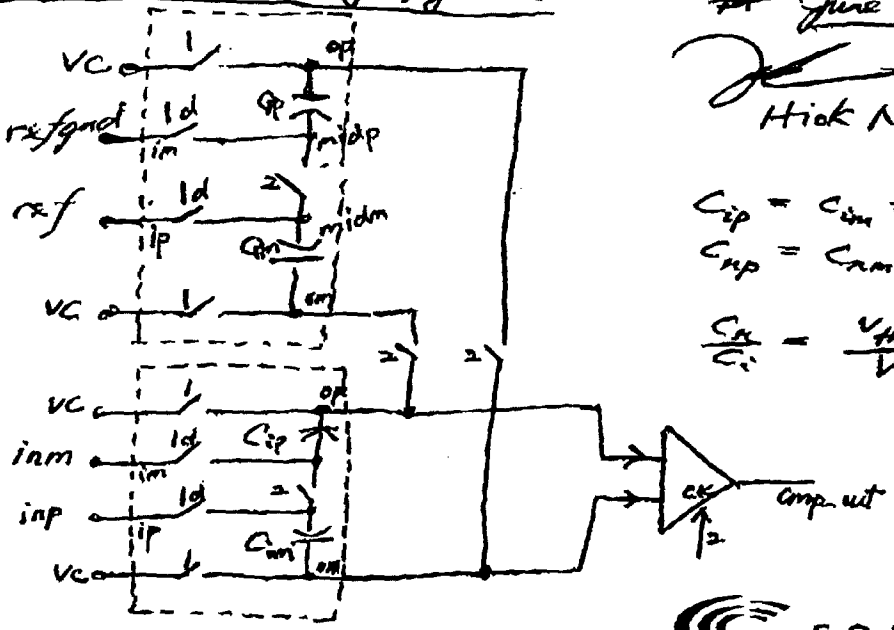


A problem above is ~~that~~ charge injection into C1 & C2 and C3 & C4. This can be avoided by shorting out the terminals of the caps and connected to refgnd & ref.

New Version insensitive to Charge Injection

~~June~~ June 03, 2000

Hiok Nam Tay



$C_{ip} = C_{im} = C_1$

$C_{np} = C_{nm} = C_2$

$$\frac{C_2}{C_1} = \frac{V_{threshold}}{V_{ref} - V_{refgnd}}$$

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