05-17-2002

Form PTO-1595 (Rev. 03/01)
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RE(102093946

U.S. DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):
SONICblue Incorporated

5-10-02

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)
Name: S3 Graphics Co., Ltd.
Internal Address:

Street Address: Charles Adams, Ritchie & Duckworth
Zephyr House, Mary Street, P.O. Box 709
Grand Cayman, British West Indies

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:
☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other

Execution Date: January 3, 2001

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)

B. Patent No.(s)
6,052,133

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:
Name: Susan Yee
Internal Address: Carr & Ferrell LLP

Street Address: 2225 East Bayshore Road, Suite 200

City: Palo Alto State: CA Zip: 94303

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41).....$ 40
☒ Enclosed
☒ Authorized to be charged to deposit account

8. Deposit account number:
06-0600

(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Susan Yee, Reg. No. 41,388 — Name of Person Signing
Susan Yee — Signature
5/1/02 — Date

Total number of pages including cover sheet, attachments, and documents: 8

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

ASSIGNMENT OF PATENT APPLICATIONS AND DISCLOSURES

WHEREAS, SONICblue Incorporated, a corporation organized and existing under the laws of the state of Delaware, successor in interest to S3 Incorporated, ("Assignor") and having an office and place of business at 2841 Mission College Boulevard, Santa Clara, CA 95054, is the owner of the inventions and patent applications and disclosures listed in Schedule 1 annexed hereto and made a part hereof; and

WHEREAS, S3 Graphics Co., Ltd., a corporation organized and existing under the laws of the Cayman Islands, having a registered office at Charles Adams, Ritchie & Duckworth, Zephyr House, Mary Street, P.O. Box 709, Grand Cayman, British West Indies ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the inventions and patent applications and disclosures listed in Schedule 1 annexed hereto, in the United States of America, and in its colonies, territories, and dependencies, and also in all countries foreign to the United States of America.

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN:

Be it know that for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the aforesaid Assignor has sold, assigned, and transferred, and by these presents does hereby sell, assign, and transfer unto said Assignee the full and exclusive right, title, and interest in and to the aforesaid inventions and patent applications and disclosures in the United States of America, and in its colonies, territories, and dependencies, and also in all countries foreign to the United States of America, the same to be held and enjoyed by said Assignee for its own use, and for the use of its successors, assigns, or other legal representatives to the end of the term or terms for which said Letters Patent may be granted as fully and entirely as the same would have been held and enjoyed by Assignor if this Assignment had not been made.

Assignor hereby authorizes Assignee, and wherever the same is permitted by law, its successors, to apply for a patent or patents directly in its own name, upon the aforesaid inventions, and the Assignor also assigns, sells, transfers, and sets over unto said Assignee and its successors all priority rights in the aforesaid inventions.

Assignor further covenants to execute all additional instruments and to do all things necessary for carrying out the purpose of this instrument, at the expense of said

Assignee and its successors.

This assignment is effective January 3, 2001.

SONICblue Incorporated
Signed at Palo Alto CA,
this 3 day of January, 2001

By: _____
Name: Kenneth Potashner
Title: President and Chief Executive Officer

casenum	count	sequ	title	status	issue_date	patent_num
CR0001	US	1.2	Method and Apparatus for Producing Perception of High Quality Grayscale Shading on Digitally Commanded Displays	issued	3/8/94	5,293,159
CR0002	US	1.1	Image Memory Controller for Controlling Multiple Memories and Method of Operation	issued	8/31/93	5,241,642
CR0003	US	1.2	Video Window Generator with Scalable Video	issued	3/28/95	5,402,513
CR0004	US	1.2	VGA Controller Circuitry	issued	12/3/96	5,581,279
CR0005	US	1.2	Video Processor w/ Multiple Streams of Video Data in Real-time	issued	8/8/95	5,440,683
CR0005	EP	1.2	Digital Video Editing Processing Unit	issued	12/16/98	558208
CR0005	JP	1.2	Digital Video Editing Processing Unit	pending		
CR0006	US	1.1	Integrated Video Scaling and Sharpening Filter	issued	6/6/95	5,422,827
CR0007	US	1.1	Process for Producing Shaded Colored Images Using Dithering Techniques	issued	5/26/98	5,757,347
CR0008	US	1.2	System and Method for the Mixing of Graphics and Video Signals	Issued	3/30/99	5,889,499
CR0009	US	2.1	Video Processing Apparatus, Systems, and Methods	issued	4/29/97	5,625,379
CR0010	US	1.1	Shared Memory for Split-panel LCD Display Systems	issued	7/16/96	5,537,128
CR0011	US	1.1	Variable Pixel Depth and Format for Video Windows	issued	3/4/97	5,608,864
CR0011	EP	1.1	Variable Pixel Depth and Format for Video Windows	pending		
CR0011	JP	1.1	Variable Pixel Depth and Format for Video Windows	pending		
CR0011	KR	1.1	Variable Pixel Depth and Format for Video Windows	issued	11/29/99	245309
CR0012	US	1.1	Method and Apparatus for Expanding and Centering VGA Text and Graphics	issued	5/28/96	5,521,614
CR0013	US	1.1	Video Processing Apparatus, Systems, and Methods	issued	10/13/98	5,821,918
CR0014	US	1.1	Brightness Control for Liquid Crystal Displays	issued	3/31/98	5,734,362
CR0015	US	1.1	Optimum Implementation of X-Y Clipping on Pixel Boundary	issued	9/16/97	5,668,941
CR0016	US	1.1	Method and Apparatus for Upscaling Video Images in a Graphics Controller Chip	pending		
CR0016	US	1.2	Method and Apparatus for Upscaling Video Images in a Graphics Controller Chip	issued	9/5/00	6,115,507
CR0017	US	1.1	Method and Apparatus for Upscaling Video Images when Pixel Data Used for Upscaling a Source Video Image are Unavailable	issued	12/30/97	5,703,618
CR0017	EP	1.1	Apparatus for Image Scaling Using Interpolation	pending		
CR0017	JP	1.1	Method and Apparatus for Upscaling Video Images when Pixel Data Used for Upscaling a Source Video Image are Unavailable	pending		
CR0017	TW	1.1	Method and Apparatus for Upscaling Video images when Pixel Data Used for Upscaling a Source Video Image are Unavailable	allowed		
CR0018	US	1.1	Controller for Processing Different Pixel Data Types Stored in the Same Display Memory by Use of Tag Bits (as amended)	issued	10/27/98	5,828,383
CR0020	US	1.1	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	issued	12/21/99	6,005,546
CR0020	EP	1.1	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	pending		
CR0020	JP	1.1	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	pending		
CR0020	TW	1.1	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	pending	5/6/00	110483
CR0020	US	1.2	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	pending		
CR0021	US	1.1	Register Set Reordering for a Graphics Processor Based Upon the Type of Primitive to be Rendered	issued	8/11/98	5,793,386
CR0021	EP	1.1	Register Set Reordering for a Graphics Processor Based Upon Type of Primitive to be Rendered	pending		
CR0021	JP	1.1	Register Set Reordering for a Graphics Processor Based Upon Type of Primitive to be Rendered	pending		
CR0021	TW	1.1	Register Set Reordering for a Graphics Processor Based Upon Type of Primitive to be Rendered	issued	7/16/98	093478
CR0022	US	1.1	Object Referenced Memory Mapping	issued	5/26/98	5,758,128
CR0022	EP	1.1	Memory Mapping Method and Apparatus	pending		
CR0022	JP	1.1	Object Referenced Memory Mapping	pending		
CR0022	TW	1.1	Object Referenced Memory Mapping	pending		
CR0023	US	1.1	Apparatus, Systems, and Methods for Controlling Data Overlay in Multimedia Data Processing and Display Systems Using Mask Techniques	issued	11/2/99	5,977,960
CR0024	US	1.1	Instruction Format for Ensuring Safe Execution of Display List	issued	2/23/99	5,875,295
CR0024	TW	1.1	Instruction Format for Ensuring Safe Execution of Display List	pending		
CR0025	US	2.1	Software-based Dithering Method and Apparatus Using Ramp Probability Logic	issued	12/28/99	6,008,796
CR0025	TW	1.1	Improved Dithering Method and Apparatus Using Ramp Probability Logic	pending		
CR0025	US	1.1	Dithering Method and Apparatus Using Ramp Probability Logic	issued	7/11/00	6,088,016
CR0026	US	1.1	Method for Triangle Subdivision in Computer Graphics Texture Mapping to Eliminate Artifacts in High Perspective Polygons	issued	11/24/98	5,841,443

CR0027	US	1.1	Method and Apparatus for Adjusting Graphics Processing Procedures Based on a Selectable Speed/quality Gauge	issued	11/2/99	5,977,983
CR0028	US	1.1	Method and Apparatus for Shortening Display List Instructions	issued	6/6/00	6,072,508
CR0028	PCT	1.1	Method and Apparatus for Shortening Display List Instructions	pending		
CR0029	US	1.1	Method and Apparatus for Programming a Graphics Subsystem Register Set	issued	2/22/00	6,028,613
CR0029	PCT	1.1	Method and Apparatus for Programming a Graphics Subsystem Register Set	pending		
CR0030	US	1.1	Method for Emulating Video Port Manager Interface	pending		
CR0031	US	1.1	Variable Band Size Compositing Buffer Method and Apparatus	issued	11/10/98	5,835,104
CR0032	US	1.1	Opposing Directional Fill Calculators in a Graphics Processor	issued	10/31/00	6141020
CR0033	US	1.1	Parallel Architecture for Graphics Primitives Decomposition	preparation		
CR0033	US	1.0	Parallel Architecture for Graphics Primitives Decomposition	pending		
CR0034	US	1.1	Graphics Primitives Decomposition Using Edge Functions and Recursive Tile Subdivision	preparation		
CR0034	US	1.0	Graphics Primitives Decomposition Using Edge Functions and Recursive Tile Subdivision	pending		
EX0028	US	1.1	Debug and Video Queue for Multi-processor Chip	issued	12/8/98	5,848,264
EX0032	US	1.1	Multiplier with Selectable Booth Encoders for Performing 3D Graphics Interpolations with two Multiplies in a Single Pass through the Multiplier	issued	8/10/99	5,935,198
EX0032	GB	1.1	Multiplier for Performing 3D Graphics Interpolations	pending		
EX0032	DE	1.1	Multiplier for Performing 3D Graphics Interpolations	pending		
EX0032	JP	1.1	Multiplier for Performing 3D Graphics Interpolations	Pending		
S30001	US	2.1	Open High-Speed Bus for Computer System	issued	5/14/96	5,517,626
S30008	US	1.1	Improved Data Retrieval from Sequential-Access Memory Device	issued	5/16/95	5,416,749
S30009	US	1.2	Method and Apparatus for Correction of Video Tearing Associated with a Video Graphics Shared Frame Buffer, as Displayed on a Graphics Monitor	issued	6/9/98	5,764,240
S30014	US	1.1	Grayscale Shading for Liquid Crystal Display Panels	issued	7/7/98	5,777,590
S30014	JP	1.1	Grayscale Shading for Liquid Crystal Display Panels	pending		
S30015	US	1.1	Decompression of MPEG Compreseed Data in a Computer System	issued	7/7/98	5,778,096
S30015	US	2.1	Method and Apparatus for Decompression of MPEG Compressed Data in a Computer System	issued	6/30/98	5,774,676
S30016	US	1.1	Correction of Interlaced Flicker Associated with Noninterlaced-to-Interlaced Video Conversion	issued	6/8/99	5,910,820
S30016	JP	1.1	Correction of Interlaced Flicker Associated with Noninterlaced-to-Interlaced Video Conversion	pending		
S30017	US	1.1	Video Decoder Engine	issued	10/6/98	5,818,967
S30019	US	1.1	Frame Reconstruction for Video Data Compression	issued	5/26/98	5,757,670
S30020	US	1.1	Multifunction Controller and Method for a Computer Graphics Display System	issued	4/14/00	6,052,133
s30020	US	1.2	Multifunction Controller and Method for a Computer Graphics Display System	pending		
S30022	US	1.1	Closed-Captioning Processing Architecture for Providing Text Data During Multiple Fields of a Video Frame	issued	3/16/99	5,883,675
S30022	JP	1.1	Closed-Captioning Processing Architecture	pending		
S30023	US	1.1	Index and Storage System for Data Provided in the Vertical Blanking Interval	issued	6/22/99	5,914,719
S30023	DE	1.1	Index and Storage System for Data Provided in the Vertical Blanking Interval	pending		
S30023	JP	1.1	Index and Storage System for Data Provided in the Vertical Blanking Interval	pending		
S30024	US	1.1	Dual Image Computer Display Controller	issued	11/2/93	5,977,933
S30024	TW	1.1	Dual Image Computer Display Controller	pending		
S30027	US	1.1	Virtual Address Access to Tiled Surfaces	allowed		
S30027	CA	1.1	Virtual Address Acess to Tiled Surfaces	pending		
S30027	EP	1.1	Virtual Address Acess to Tiled Surfaces	pending		
S30028	US	1.1	Pixel Reordering for Improved Texture Mapping	issued	12/22/98	5,852,451
S30028	CA	1.1	Pixel Reordering for Improved Texture Mapping	pending		
S30028	EP	1.1	Pixel Reordering for Improved Texture Mapping	pending		
S30031	US	1.1	System and Method for a Fast Carry/Sum Select Adder	issued	12/22/98	5,852,568
S30031	EP	1.1	System and Method for a Fast Carry/ Sum Select Adder	pending		
S30031	JP	1.1	System and Method for a Fast Carry/Sum Select Adder	pending		
S30031	CA	1.1	System & Method for a Fast Carry/Sum Select Adder	pending		
S30032	US	1.1	System and Method for Simultaneous Flicker Filtering and Overscan Compensation	issued	11/23/99	5,990,965

S30032	CA	1.1	Flicker Filtering and Overscan Compensation	pending		
S30032	JP	1.1	System and Method for Simultaneous Flicker Filtering and Overscan Compensation	pending		
S30032	KR	1.1	Flicker Filtering and Overscan Compensation	pending		
S30032	EP	1.1	Flicker Filtering and Overscan Compensation	pending		
S30033	US	1.1	Block-and-Band-Oriented Traversal in Three-Dimensional Triangle Rendering	issued	8/31/99	5,945,997
S30033	PCT	1.1	Block-and-Band-Oriented Traversal in Three-Dimensional Triangle Rendering	Pending		
S30033	CA	1.1	Block-and-Band-Oriented Traversal in Three-Dimensional Triangle Rendering	pending		
S30033	JP	1.1	Block-and-Band-Oriented Traversal in Three-Dimensional Triangle Rendering	pending		
S30034	US	1.1	System and Methods for 2-tap/3-tap Flicker Filtering	issued	7/4/00	6,084,568
S30034	EP	1.1	System and Methods for 2-tap/3-tap Flicker Filtering	pending		
S30034	JP	1.1	System and Methods For 2-Tap/3-Tap Flicker Filtering.	pending		
S30034	CA	1.1	System and Methods for 2-tap/3-tap Flicker Filtering	pending		
S30035	US	1.1	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	issued	9/21/99	5,956,431
S30035	PCT	1.1	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	pending		
S30035	US	1.2	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	pending		
S30035	US	1.3	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	pending		
S30035	US	1.4	System and Method for Fixed-Rate Block-Based Image 3-D Compression with Inferred Pixel Values	preparation		
S30035	KR	1.1	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	pending		
S30037	US	1.1	Integrated DRAM with High Speed Interleaving	issued	1/5/99	5,856,947
S30037	PCT	1.1	Integrated DRAM with High Speed Interleaving	pending		
s30037	TW	1.1	Integrated DRAM With High Speed Interleaving	pending		
S30037	CA	1.1	Integrated DRAM With High Speed Interleaving	pending		
s30037	KR	1.1	Integrated DRAM With High Speed Interleaving	pending		
S30037	EP	1.1	Integrated DRAM with High Speed Interleaving	pending		
S30044	US	1.0	Ratio Engine for Graphic Interpolation	pending		
S30044	US	1.1	System and Method for Rasterizing Primitives Using Direct Interpolation	pending		
S30045	US	1.1	High DC Current and Stagger Power/Ground Pad	issued	2/29/00	6,031,258
S30047	US	1.1	System and Method for a Self-Adjusting Data Strobe	issued	9/7/99	5,948,083
S30048	US	1.1	Computer Processor and Method for Data Streaming	Issued	9/28/99	5,958,038
S30048	JP	1.1	Computer Processor and Method for Data Streaming	pending		
S30048	CA	1.1	Computer Processor and Method for Data Streaming	pending		
S30049	US	1.0	Efficient X, Y Based Level of Detail Scheme for Mipmapped Texturing	pending		
S30049	US	1.1	Efficient X, Y Based Level of Detail Scheme for Mipmapped Texturing	pending		
S30050	US	1.0	Trilinear Texture Filtering with Optimized Memory Access ("One-Level Trilinear")	pending		
S30050	US	1.1	Trilinear Texture Filtering with Optimized memory Access ("One-Level Trilinear")	pending		
S30050	PCT	1.1	Trilinear Texture Filtering with Optimized memory Access ("One-Level Trilinear")	pending		
S30051	US	1.0	Double Buffered Graphics and Video Accelerator Having a Write Blocking memory Interface and Method of Doing the Same	pending		
S30051	US	1.1	Double Buffered Graphics and Video Accelerator Having a Write Blocking memory Interface and Method of Doing the Same	issued	10/3/00	6128026
S30051	PCT	1.1	Double Buffered Graphics and Video Accelerator having a Write Blocking Memory Interface and Method of Doing the Same	pending		
S30052	US	1.0	Computer System and Method for Efficiently Communicating Peripheral Device Status	pending		
S30052	US	1.1	Communicating the Status of a Peripheral Device Controller to a Host Processor	pending		
S30052	PCT	1.1	Communicating the Status of a Peripheral Device Controller to a Host Processor	pending		
S30053	US	1.0	Device and Method for Blending True Colors and Fog Colors to Generate Display Colors	pending		
S30053	US	1.1	Device and Method for Blending True Colors and Fog Colors to Generate Display Colors	pending		
S30057	US	1.1	System and Method for Mapping Textures onto Surfaces of Computer-Generated Objects	pending		
S30057	US	2.1	System and Method for Mapping Textures onto Surfaces of Computer-Generated Objects	pending		
S30057	US	3.1	System and Method for Mapping Textures onto Surfaces of Computer-Generated Objects	pending		
S30059	US	1.1	Out of Order Dispatch Unit for Graphics Primitives	pending		

S30060	US	1.1	Real Time DRAM Eliminating A Performance Penalty for Crossing a Page Boundary (as amended)	issued	12/28/99	6,009,019
S30060	PCT	1.1	Real Time DRAM Page Boundary Adjustment	pending		
S30061	US	1.1	System and Method for Copy Protecting Computer Graphics	pending		
S30064	US	1.1	Adaptive Dynamic Aperture Correction	allowed		
S30065	US	1.1	Flat-Panel Display Controller with Improved Dithering and Frame Rate Control	issued	12/28/99	6,008,794
S30066	US	1.1	Programmable Delay Timing Calibrator for High Speed Data Interface	allowed		6,041,419
S30066	CA	1.1	Programmable Delay timing Calibrator for High Speed Data Interface	pending		
S30071	US	1.1	AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals on an Integrated Circuit Ship	allowed		
S30071	PCT	1.1	AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals On an Integrated Circuit Chip	pending		
S30071	JP	1.1	AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals On an Integrated Circuit Chip	pending		
S30071	KR	1.1	AGP/DDR Interfaces For Full Swing And Reduced Swing (SSTL) Signals On An Integrated Circuit Chip	Pending		
S30072	US	1.1	Non-Stalled Requesting Texture Cache System and Method	issued	1/4/00	6,011,565
S30072	EP	1.1	Non-Stalled Requesting Texture Cache System and Method	pending		
S30072	CA	1.1	Non-Stalled Requesting Texture Cache System and Method	pending		
S30072	JP	1.1	Non-Stalled Requesting Texture Cache System and Method	pending		
S30073	US	1.1	A System and Method for Performing Dithering with a Graphics Unit Having an Oversampling Buffer	Allowed		
S30074	US	1.1	A System and Method for Performing Blending Using an Over Sampling Buffer	issued	11/7/00	6144365
S30075	US	1.1	A Device to Control Two Synchronous Command Streams	pending		
S30083	US	1.1	State Parser for a Multistage Graphics Pipeline	pending		
S30084	US	1.1	An Improved Self Burn-In Apparatus and Method for Semiconductor Devices	pending		
S30085	US	1.1	Span-Based Z Buffer	preparation		
S30085	US	1.0	Span-Based Z Buffer	pending		
S30087	US	1.1	Removal of Interpolation Atrifacts in a Non-Interlaced Video Stream	pending		
S30088	US	1.1	Z-Buffer Based Interpenetrating Object Detection for Antialiasing	pending		
S30089	US	1.1	Method and Apparatus for Interpolative, Adaptive Illumination in 3D Graphics	pending		
S30090	US	1.1	Timing and Control for Deinterlacing and Enhancement of Non-Deterministically Arriving Interlaced Video Data	allowed	3/7/00	6,034,733
s30090	US	1.2	Timing and Control for Deinterlacing and Enhancement of Non-Deterministically Arriving Interlaced Video Data	pending		
S30091	US	1.1	Image Stretching with Color Key Edge Removal In Streams	pending		
S30097	US	1.1	Apparatus and Method for Gray-Scale and Brightness Display Control	pending		
S30098	US	1.1	Method for Implementing Resistance, Capacitance, and/or Inductance in an Integrated Circuit	pending		
S30098	TW	1.1	Method for Implementing Resistance, Capacitance, and/or Inductance in an Integrated Circuit	pending		
S30099	US	1.1	4:1 Z-Buffer Compression	pending		
S30100	US	1.1	Command Reordering for out of Order Bus Transfer	pending		
S30100	PCT	1.1	Command Reordering for out of Order Bus Transfer	pending		
S30101	US	1.1	Fast and Cheap Correct Resolution Conversion for Digital Numbers	preparation		
S30102	US	1.1	Optimized Illumination Computation	preparation		
S30103	US	1.1	Logarithm-Based Illumination Computation	preparation		
S30104	US	1.1	Logarithm-Based Level-of-Detail Computation	preparation		
S30105	US	1.1	Shadow Rendering System and Method	pending		
S30105	US	1.0	One Pass Shadow Algorithm for Hardware Graphics	pending		
S30106	US	1.1	System for Low Miss Rate Replacement of Texture Cache Lines	pending		
S30108	US	1.1	System and Method for Implementing a Two-Layer Z Range Buffer	pending		
S30108	PCT	1.1	System and Method For Implementing A Two Layer Z Range	pending		
S30109	US	1.1	Parametrized Median Set De-Interlacing System	pending		
S30111	US	1.1	Multichip Module Packaging Process for Known Good Die Burn-In	pending		
S30111	JP	1.1	Multichip Module Packaging Process for Known Good Die Burn-In	pending		
S30111	KR	1.1	Multichip Module Packaging Process for Known Good Die Burn-In	pending		
S30111	TW	1.1	Multichip Module Packaging Process for Known Good Die Burn-In	pending		

S30111	EP	1.1	Multichip Module Packaging Process For Known Good Die Burn-In	Pending
S30112	US	1.1	Direct Evaluation of Multi-Pixel Multi-Texture Rendering	pending
S30113	US	1.1	A Multi-Stage Fixed Cycle Pipelined Lighting Equation Evaluator	pending
S30113	TW	1.1	A Multi-Stage Fixed Cycle Pipelined Lighting Equation Evaluator	pending
S30113	PCT	1.1	Multi-Stage Fixed Cycle Pipe-Lined Lighting Equation Evaluator	pending
S30114	US	1.1	A Token Based Vertex Buffer Management Scheme in the Geometry Pipe of a 3D Graphical Subsystem	pending
S30115	US	1.1	Non-Flushing Atomic Operation in a Burst Mode Transfer Data Storage Access Environment	pending
S30115	PCT	1.1	Non-Flushing Atomic Operation in a Burst Mode Transfer Data Storage Access Environment	pending
S30116	US	1.1	Macroblock Tiling Format for MPEG Motion Compensation	pending
S30116	US	1.2	Macroblock Tiling Format for MPEG Motion Compensation	pending
S30117	US	1.1	Method and Apparatus for Managing Cache Data	preparation
S30117	US	1.0	Method and Apparatus for Managing Cache Data	pending
S30118	US	1.1	Synchronizing a Two-Level Cache in a Graphics Processing System	Pending
S30118	PCT	1.1	SYNCHRONIZED TWO-LEVEL GRAPHICS PROCESSING CACHE	pending
S30119	US	1.1	Dynamic Allocation of Texture Cache Memory	pending
S30119	US	1.0	A Multi-Stage Fixed Cycle Pipelined Lighting Equation Evaluator	pending
S30119	PCT	1.1	DYNAMIC ALLOCATION OF TEXTURE CACHE MEMORY	pending
S30120	US	1.1	Selective Super-sampling/Adaptive Anti-Aliasing of Complex 3D Data	Pending
S30121	US	1.1	A Matched Texture Filter Design for Rendering Mult-Rate Data Samples	preparation
S30138	US	1.1	Multiple Hardware Overlay System for a Computer Display	preparation
				preparation

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Execution Date: January 3, 2001

2. Name and address of receiving party(ies)

Name: S3 Graphics Co., Ltd.

Internal Address: _____

Street Address: Charles Adams, Ritchie & Duckworth
Zephyr House, Mary Street, P.O. Box 709

Grand Cayman, British West Indies

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4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:_____

A. Patent Application No.(s)

B. Patent No.(s)
6,052,133

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Susan Yee

Internal Address: Carr & Ferrell LLP

Street Address: 2225 East Bayshore Road, Suite 200

City: Palo Alto State: CA Zip: 94303

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41).....$ 40

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