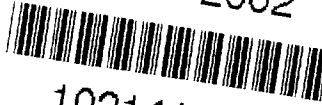


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Correspondent Name and Address

Area Code and Telephone Number 617-248-7604

Name John D. Lanza

Address (line 1) Testa, Hurwitz & Thibault, LLP

Address (line 2) High Street Tower

Address (line 3) 125 High Street

Address (line 4) Boston, MA 02110

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6

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Patent Application Number(s)

09/548,530

Patent Number(s)

Patent Cooperation Treaty (PCT)

Enter PCT application number
only if a U.S. Application Number
has not been assigned.

PCT

PCT

PCT

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Number of Properties

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1

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Fee Amount for Properties Listed (37 CFR 3.41):

\$ 40.00

Method of Payment:

Enclosed ☒Deposit Account ☐

Deposit Account

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Deposit Account Number

20-0531

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INTELLECTUAL PROPERTY ASSIGNMENT

THIS INTELLECTUAL PROPERTY ASSIGNMENT ("*Assignment*"), effective as of the 22nd day of February 2002 ("*Effective Date*"), by and between Stratus Technologies International, S.A r.l. a company organized under the laws of Luxembourg ("*Assignor*") and Stratus Technologies Bermuda Ltd., a company organized under the laws of Bermuda ("*Assignee*").

WHEREAS, Assignor is the exclusive owner of all right, title and interest in and to certain intellectual property;

WHEREAS, Assignor agrees to assign to Assignee the entirety of Assignor's right, title and interest in and to such intellectual property; and

WHEREAS, Assignee agrees to accept the entirety of Assignor's right, title and interest in and to such intellectual property;

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, Assignor does hereby assign, transfer and convey to Assignee and its successors, assigns and nominees forever, without any restrictions, reservations or limitations, any and all of Assignor's entire worldwide right, title and interest in and to all intellectual property rights of any kind or nature owned, held or used in connection with Assignor's business as of the date hereof, including without limitation:

1. All of its patents, inventions, discoveries, technology, know-how and trade secrets, including without limitation the patents and patent applications listed on Schedule A annexed hereto;
2. All of its trademarks, trade names, service marks, service names, brand names, domain names, logos and other source indicators in the United States and all foreign countries, including without limitation the registrations and applications for the foregoing listed on Schedule B annexed hereto, together with the goodwill of Assignor's business appertaining thereto and/or symbolized thereby;
3. All of its copyrights and copyrightable works (including software, databases and related items), including without limitation the copyright registrations and applications listed on Schedule C annexed hereto;
4. All rights, priorities and privileges of Assignor provided under the laws of the United States and all applicable nations, including without limitation the nations listed on Schedules A-C, or any multinational law, compact, treaty, protocol, convention or organization, with respect to the foregoing rights;
5. All rights to sue at law or in equity for any infringement, impairment or other unauthorized use or conduct in derogation of the foregoing rights occurring prior to the Effective Date, including the right to receive all proceeds and damages therefrom; and

6. Any and all rights to obtain renewals, reissues, re-examinations, divisions, extensions or other legal protections pertaining to the foregoing rights (the rights in sections 1-6, collectively "*Assigned Rights*").

Assignee, its successors and assigns, shall hold the rights to the Assigned Rights for and during the existence of the term and life of such Assigned Rights, as fully and as entirely as the same would have been held and enjoyed by Assignor had this Assignment not been made.

This Assignment is effective as of the Effective Date. Assignor shall, without further consideration, comply with a reasonable request by Assignee, at Assignee's expense, to execute promptly any additional documents provided by Assignee and to take promptly any further action necessary to protect, secure and vest good, valid and marketable title to the Assigned Rights in Assignee in all relevant nations, including without limitation the nations listed on Schedules A-C.

The parties agree that the assignment of each item on Schedules A-C shall be construed as separable and divisible from the assignment of every other item. The unenforceability or invalidity of this Assignment with respect to any one item shall not limit its enforceability or validity, in whole or in part, with respect to any other item.

This Assignment may be signed in one or more counterparts, each of which shall be an original and all of which shall be considered one and the same agreement, and shall become effective when one or more such counterparts have been signed by each party and received by the other party.

This Assignment shall be governed by, and construed and interpreted in accordance with, the law of the State of New York.

IN WITNESS WHEREOF, the undersigned have caused this Assignment to be duly executed and delivered as of the date first above written.

STRATUS TECHNOLOGIES INTERNATIONAL,
S.À.R.L.

By: 

Name: Zahid Zakiuddin

Title: Officer

STRATUS TECHNOLOGIES BERMUDA LTD.

By: _____

Name:

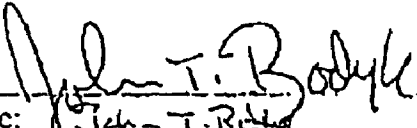
Title:

IN WITNESS WHEREOF, the undersigned have caused this Assignment to be duly executed and delivered as of the date first above written.

STRATUS TECHNOLOGIES INTERNATIONAL,
S.A.R.L.

By: _____
Name:
Title:

STRATUS TECHNOLOGIES BERMUDA LTD.

By:  _____
Name: John T. Boyle
Title: Director

Patent Information

	PATENT APPLICATIONS FILED	FILING DATE	APPLICATION NUMBERS
	TITLE		
1	Fault-Tolerant Computer System With Voter Delay Buffer	April 13, 2000	09/548,528
2	Hot Plug Switch Mechanism	April 13, 2000	09/548,529
3	Method And System For Upgrading Fault-Tolerant Systems	April 13, 2000	09/548,527
4	System And Method For Operating A System With Redundant Peripheral Bus Controllers	April 13, 2000	09/548,200
5	Apparatus and Methods for Identifying Bus Protocol Violation	February 28, 2001	09/796,155
6	Dynamically Extendible Firewall	April 14, 2000	09/550,230
7	Fault-Tolerant Maintenance Bus Architecture	April 13, 2000	09/548,536
8	Fault-Tolerant Maintenance Bus Protocol And Method For Using The Same	April 13, 2000	09/548,202
9	Methods And Apparatus For Persistent Volatile Computer Memory	April 14, 2000	09/550,108
10	System And Method For Operating A SCSI Bus With Redundant SCSI Adaptors	April 13, 2000	09/548,530
11	Method And Apparatus For Deterministically Booting A Redundant Fault-Tolerant System	April 14, 2000	09/549,733
12	Method And Apparatus For Fault-Tolerant System Recovery	April 14, 2000	09/550,004
13	Secure Service Network	April 14, 2000	09/550,243
14	Robust Service Network	April 14, 2000	09/549,508
15	Maintenance Of Consistent, Redundant Mass Storage Images	September 18, 2000	09/664,483
16	Methods And Apparatus For Generating High-Frequency Clocks Deterministically From A Low-Frequency System Reference Clock	September 20, 2000	09/665,867
17	Method And Apparatus For Clock Management Based On Environmental Conditions	September 21, 2000	09/666,264
18	Apparatus And Methods For Boosting Power Supplied At A Remote Node	December 7, 2000	09/731,451
19	A Method And Apparatus For Efficiently Moving Portions Of A Memory Block	December 20, 2000	09/742,989
20	Apparatus And Methods For Limiting Electrical Current In Circuit Breaker Applications	December 22, 2000	09/748,596
21	Implementing Standards-Based File Operations In Proprietary Operating Systems	February 16, 2001	09/785,607
22	Electronic Circuit Design (filed simultaneously in Ireland as both short term and regular application and filed in European Patent Office)	August 8, 2000	N/A
23	Caching for I/O Virtual Address Translation and Validation Using Device Drivers	February 20, 2001	09/789,051
24	Methods And Apparatus for Computer Bug Error Termination	May 31, 2001	09/871,180
25	Coordinated Recalibration of High Bandwidth Memories in a Multiprocessor Computer	March 5, 2001	09/799,478

	PATENT APPLICATIONS FILED	FILING DATE	APPLICATION NUMBERS
26	Apparatus And Methods for Fault-Tolerant Computing Using a Switching Fabric	March 28, 2001	09/819,328
27	An Apparatus And Method for Two Computing Elements in a Fault-Tolerant Server to Execute Instructions in Lockstep	April 11, 2001	09/832,466
28	An Apparatus And Method for Accessing a Mass Storage Device in a Fault-Tolerant Server	April 11, 2001	09/832,467
29	Fault-Tolerant Power-Supply Current-Sharing Apparatus And Methods	September 21, 2001	09/961,130
30	A Method and Apparatus for Storing Transactional Information in Persistent Memory	February 22, 2001	09/790,750
31	System and Methods for Caching With File-Level Granularity	March 1, 2001	09/797,100
32	A Method and Apparatus for Managing Session Information	April 12, 2001	09/833,835
33	A Binary Object System for Automated Data Translation	June 15, 2001	09/882,874
34	A Method and Apparatus for Scanning Records	September 24, 2001	09/961,608