

10-16-2002

FORM PTO-1595

1-31-92



U.S. DEPARTMENT OF COMMERCE

Patent and Trademark Office

To the Honorable Commissioner of Patents

102250086

Original documents or copy thereof.

1. Name of conveying party(ies):

TRIPATH TECHNOLOGY INC.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of Conveyance:

☐ Assignment☒ Security Agreement☐ Other:☐ Merger☐ Change of Name

Execution Date: July 12, 2002

2. Name and address of receiving party(ies):

Name: COMERICA BANK-CALIFORNIA

Address: 333 WEST SANTA CLARA STREET

City: SANTA CLARA State: CA Zip: 95113

Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):

If this Document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)

See attached sheets

Patent No.(s)

See attached sheets

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Erin O'Brien

Internal Address: GRAY CARY WARE & FREIDENRICH  
4365 Executive Drive, Suite 1100  
San Diego, CA 92121-2133

6. Total number of applications and patents involved: 23

7. Total fee (37 CFR 3.41) . . . . . \$ 920.00

☒ Enclosed

8. Deposit account number:

Please debit any underpayment or credit any overpayment to the above deposit account.

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Erin O'Brien

Name of Person Signing

Signature

October 8, 2002

Date

Total number of pages comprising cover sheet: [ 9 ]

OMB No. 0651-0011 (exp. 4/94)

Do not detach this portion

Mail documents to be recorded with required cover sheet information to:

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920.00 DP

Gray Cary\PA\10261749.1  
1090371-975700PATENT  
REEL: 013372 FRAME: 0170

PATENTS

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
Scheme for reducing transmit-band noise floor and adjacent channel power with power backoff	09/908,967	07/18/01
Noise reduction scheme for operational amplifiers	09/908,862	07/18/01
Power device driver circuit	6,362,679	03/26/02
Loop delay compensation for a digital power amplifier	09/796,634	02/28/01
Resonant gate drive technique for a digital power amplifier	09/796,734	02/28/01
Self-timed switching for a digital power amplifier	09/796,731	02/28/01
Dual independently clocked analog-to-digital conversion for a digital power amplifier	6,348,836	02/19/02
Methods and apparatus for noise shaping a mixed signal power output	6,297,697	10/02/01
Break-before-make distortion compensation for a digital amplifier	6,362,683	03/26/02
Dynamic switching frequency control for a digital switching amplifier	6,351,184	02/26/02
Noise reduction scheme for operational amplifiers	6,329,876	12/11/01
DC offset calibration for a digital switching amplifier	6,316,992	11/13/01
Power efficient line driver	6,281,747	08/28/01
Power efficient line driver	6,246,283	06/12/01
Methods and apparatus for noise shaping a mixed signal power output	6,229,390	05/08/01
Power supply topology to reduce the effects of supply pumping	6,169,681	01/02/01
Method and apparatus for controlling an audio signal level	6,127,893	10/03/00
Methods and apparatus for reducing MOSFET body diode conduction in a half-bridge configuration	6,107,844	08/22/00
Methods and apparatus for compensating delays in modulator loops	5,909,153	06/01/99
Methods and apparatus for performance improvement by qualifying pulses in an oversampled noise-shaping signal processor	5,974,089	10/26/99
Method and apparatus for sensing a common mode voltage	5,808,491	09/15/98
Method and apparatus for oversampled, noise-shaping, mixed-signal	5,777,512	07/07/98

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1090371-975700

# PATENTS

Description  
processing

Registration/  
Application  
Number

Registration/  
Application  
Date

Method and apparatus for biasing a differential cascode circuit

5,754,079

05/19/98

# INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of July 12, 2002 by and between COMERICA BANK-CALIFORNIA ("Bank") and TRIPATH TECHNOLOGY INC., a Delaware corporation ("Grantor").

## RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated of even date herewith (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks and Patents to secure the obligations of Grantor under the Loan Agreement.

B. Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain copyrights, trademarks and patents to secure the obligations of Grantor under the Loan Agreement but only to the extent such security interest is necessary in order for Bank to have a perfected security interest in Grantor's accounts and other rights to payment.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement and all other agreements now existing or hereafter arising between Grantor and Bank, Grantor hereby represents, warrants, covenants and agrees as follows:

## AGREEMENT

To secure its obligations under the Loan Agreement and under any other agreement now existing or hereafter arising between Grantor and Bank, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

Grantor represents and warrants that Exhibits A, B, and C attached hereto set forth any and all intellectual property rights in connection to which Grantor has registered or filed an application with either the United States Patent and Trademark Office or the United States Copyright Office, as applicable.

Notwithstanding the foregoing, the Collateral shall not include any copyrights, patents, trademarks, servicemarks and applications therefor, now owned or hereafter acquired, or any claims for damages by way of any past, present and future infringement of any of the foregoing (collectively, the "Intellectual Property"); provided, however, that the Collateral shall include all accounts and general intangibles that consist of rights to payment and proceeds from the sale, licensing or disposition of all or any part, or rights in, the foregoing (the "Rights to Payment"). Notwithstanding the foregoing, if a judicial authority (including a U.S. Bankruptcy Court) holds that a security interest in the underlying Intellectual Property is necessary to have a security interest in the Rights to Payment, then the Collateral shall automatically, and effective as of the Closing Date, include the Intellectual Property to the extent necessary to permit perfection of Bank's security interest in the Rights to Payment.

This Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

TRIPATH TECHNOLOGY INC.

Address of Grantor:

3900 Freedom Circle  
Santa Clara, CA 95054

Attn: Chief Financial Officer

By: 

Title: CFO

BANK:

COMERICA BANK-CALIFORNIA

Address of Bank:

333 West Santa Clara Street  
San Jose, CA 95113

Attn: Corporate Banking Center

By: 

Title: ASSISTANT VICE PRESIDENT

EXHIBIT A

Copyrights

<u>Description</u>	Registration <u>Number</u>	Registration <u>Date</u>
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**EXHIBIT B****Patents**

<b><u>Description</u></b>	<b><u>Registration/ Application Number</u></b>	<b><u>Registration/ Application Date</u></b>
Scheme for reducing transmit-band noise floor and adjacent channel power with power backoff	09/908,967	07/18/01
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Break-before-make distortion compensation for a digital amplifier	6,362,683	03/26/02
Dynamic switching frequency control for a digital switching amplifier	6,351,184	02/26/02
Noise reduction scheme for operational amplifiers	6,329,876	12/11/01
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Power efficient line driver	6,246,283	06/12/01
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Method and apparatus for controlling an audio signal level	6,127,893	10/03/00
Methods and apparatus for reducing MOSFET body diode conduction in a half-bridge configuration	6,107,844	08/22/00
Methods and apparatus for compensating delays in modulator loops	5,909,153	06/01/99
Methods and apparatus for performance improvement by qualifying pulses in an oversampled noise-shaping signal processor	5,974,089	10/26/99

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1090371-900000

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
Method and apparatus for sensing a common mode voltage	5,808,491	09/15/98
Method and apparatus for oversampled, noise-shaping, mixed-signal processing	5,777,512	07/07/98
Method and apparatus for biasing a differential cascode circuit	5,754,079	05/19/98



EXHIBIT C

Trademarks

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
Tripath (and design)	76/157,810	10/31/00
TIO	76/094,294	07/24/00
TIO (and design)	76/096,234	07/24/00
Class-T	76/073,920	06/20/00
Tripath	2,398,029	10/24/00
DPP	2,453,669	05/22/01
Digital Power Processing	2,526,206	01/01/02