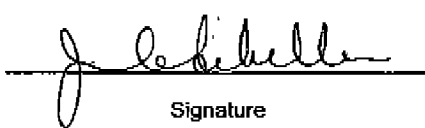


FORM PTO-1595 (Rev. 3/01) OMD NO. 0651-0011 exp. 5/31/2002		Recordation Form Cover Sheet PATENTS ONLY		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	
To the Honorable Commissioner of Patents and Trademarks. Please record the attached original documents or copy thereof.					
1. Name of conveying party(ies): Bridges2Silicon, Inc., a Delaware corporation Additional name(s) of conveying party(ies) attached? <input checked="" type="checkbox"/> No <input type="checkbox"/> Yes		2. Name and address of receiving party(ies): Name: <u>Synplicity, Inc.</u> Internal Address: _____ Street Address: <u>600 W. California Avenue</u> City: <u>Sunnyvale</u> State/Province: <u>California</u> Zip: <u>94086</u> Country: <u>United States of America</u> Additional name(s) & address(es) attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No			
3. Nature of Conveyance <input checked="" type="checkbox"/> Assignment <input type="checkbox"/> Merger <input type="checkbox"/> Security Agreement <input type="checkbox"/> Change of Name <input type="checkbox"/> Other: _____		Execution Date(s): <u>11/07/2002</u>			
4. Application Number(s) or patent number(s): If this document is being filed together with a new application, the execution date of the application is: _____ A. Patent Application No.(s) <u>09/724,702; 00982284.2; 09/724,840;</u> <u>10/210,509; 09/724,839; 09/724,585;</u> <u>10/212,128; 60/168,266; 60/230,068;</u> <u>60/360,627; 60/387,261</u>		B. Patent No.(s) Additional numbers attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No			
5. Name and address of party to whom correspondence concerning document should be mailed: James C. Scheller, Jr. Name: <u>Blakely, Sokoloff, Taylor & Zafman LLP</u> Internal Address: _____ Street Address: <u>12400 Wilshire Boulevard, 7th Floor</u> City: <u>Los Angeles</u> State: <u>California</u> Zip: <u>90025</u>		6. Total number of applications and patents involved: <u>11</u> 7. Total Fee (37 CFR 3.41....\$40.00) <input type="checkbox"/> Enclosed <input checked="" type="checkbox"/> Authorized to be charged to deposit account 8. Deposit Account Number: <u>02-2666</u> (Attach duplicate copy of this page if paying by deposit account)			
DO NOT USE THIS SPACE					
9. Statement and signature. <i>To the best of my knowledge and belief, the foregoing is true and correct and any attached copy is a true copy of the original document.</i>					
<u>James C. Scheller, Jr. #31.195</u> Name of Person Signing		 Signature		<u>2/14/2003</u> Date	
Total number of pages including cover sheet, attachments, and document: <u>10</u>					

Mail documents to be recorded with required cover sheet information to:
 Assistant Commissioner of Patents, Box Assignments
 Washington, D.C. 20231

Atty Docket No. 02986.G029

Patent Assignment Agreement

This Patent Assignment Agreement (the "Agreement") is made and effective as of November 8, 2002, by and between Bridges2Silicon, Inc., a Delaware corporation ("Assignor"), and Synplicity, Inc., a California corporation ("Assignee").

WHEREAS Assignor is the owner of the patent applications, continuations-in-part thereof, and provisional patent applications that are listed on Schedule 1 hereto (the "Patent Applications"), effectively assigned to Assignor on the filing date for each by all of the inventors of the techniques, electronic systems, designs, processes, methods, debugging methodologies and the like which are the subject of such Patent Applications; and

WHEREAS Assignee desires to acquire all of Assignor's title, right, interest, benefits and privileges to the Patent Applications and all inventive subject matter described in the Patent Applications which may be claimed in any patent applications or issued patents which claim priority to or are otherwise related to the Patent Applications anywhere in the world.

NOW, THEREFORE, for valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties hereby agree as follows:

1. Assignment. Assignor hereby, irrevocably and without reservation:

1.1 represents that Assignor is the sole owner and assignee and holder of record title to the Patent Applications and any patents that issue thereon and that it has full power to make the present assignment;

1.2 assigns, sells, transfers and conveys to Assignee all right, title and interest in and to the Patent Applications, any and all inventive subject matter described or claimed in the Patent Applications, and any and all other patent applications or issued patents claiming priority therefrom, or otherwise related to such Patent Applications, anywhere in the world, including all nonprovisional, divisional, renewal, substitute, continuation and convention applications, and any and all letters patent, reissues, reexaminations, and extensions of letters patent granted thereon, and every priority right that is or may be predicated upon or arise from the Patent Applications and patents based thereon;

1.3 binds its successors and assigns, as well as itself, to do, upon Assignee's request and at Assignee's expense, but without additional consideration to Assignor or them, all acts reasonably serving to assure that the Patent Applications and any patents issuing thereon shall be held and enjoyed by Assignee as fully and entirely as the same could have been held and enjoyed by Assignor, its successors and assigns if this Agreement had not been made; and particularly to execute and deliver to Assignee all lawful application documents including petitions, specifications and oaths, and all assignments, disclaimers and lawful affidavits in form and substance as may be reasonably requested by Assignee; to communicate to Assignee all facts known to Assignor relating to the Patent Applications; and to furnish Assignee with any and all documents, photographs, models, samples and other physical exhibits in Assignor's control or in the control of its successors or assigns which may be useful for establishing the facts of all conceptions, disclosures, and reduction to practice of the subject matter of the Patent Applications;

1.4 warrants unto Assignee and further agrees that Assignor shall, without demanding any further consideration therefor, at the request and at the expense of Assignee, do all lawful and just acts which are reasonable, including the execution and acknowledgment of instruments, that may be or become necessary for sustaining, obtaining continuations thereof, or reissuing said United States patent and foreign counterparts and for assisting Assignee in maintaining and perfecting its right to said patent, particularly in cases of interference and litigation; and

1.5 hereby authorizes the Commissioner of Patents to issue any and all patents which may be granted upon any of the Patent Applications herein referenced to Assignee, as the assignee to the entire interest therein.

2. Binding Agreement. The terms and covenants of this Agreement shall inure to the benefit of Assignee and its successors and assigns, and shall be binding upon Assignor and its successors and assigns.

3. Miscellaneous. This Agreement shall be governed by the laws of the State of California, without reference to conflict of laws principles. Any failure to enforce any provision of the Agreement shall not constitute a waiver thereof or of any other provision. This Agreement may not be amended, nor any obligation waived, except by a writing signed by both parties; nor shall any obligation herein be waived except in a writing signed by the person charged with making such waiver. If any provision of this Agreement is held by a court of competent jurisdiction to be unenforceable, then such provision shall be eliminated or limited to the extent required by applicable law and this Agreement, as so modified, shall remain enforceable in accordance with its terms.

[Remainder of Page Left Blank Intentionally]

IN WITNESS WHEREOF, Assignor and Assignee have each caused this Agreement to be duly executed and delivered as of the date first written above.

ASSIGNOR:

BRIDGES2SILICON, INC.

By: Robert M. Gardner
Robert Gardner
President

ASSIGNEE:

SYNPLICITY, INC.

By: Douglas S. Miller
Douglas S. Miller
Vice President of Finance and Chief Financial Officer

13:04 FROM:

TO: 7208383

P: 5:10

State of California)
) ss.
County of Santa Clara)

On this 7th day of November 2002, before me the undersigned, a Notary Public in and for the County and State aforesaid, personally appeared Robert Gardner, who is personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to within instrument and acknowledged to me that he executed the same in his authorized capacity and that by his signature on such instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS, my hand and official seal.



Nancy Bough

Notary Public

State of California)
) ss.
County of Santa Clara)

On this 7th day of November 2002, before me the undersigned, a Notary Public in and for the County and State aforesaid, personally appeared Douglas S. Miller, who is personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to within instrument and acknowledged to me that he executed the same in his authorized capacity and that by his signature on such instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS, my hand and official seal.



Nancy Bouch

Notary Public

Patent Assignment Agreement**SCHEDULE 1**

1. Application No. 09/724,702 for United States Patent entitled "HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE," filed in the U.S. Patent and Trademark Office ("USPTO") on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
2. European Patent Application No.: 00982284.2 for "*HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE*," filed with the European Patent Office on November 29, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
3. Application No. 09/724,840 for United States Patent entitled, "METHOD AND SYSTEM FOR PROVIDING AN ELECTRONIC SYSTEM DESIGN WITH ENHANCED DEBUGGING CAPABILITIES," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
4. Application No. 10/210,509 for United States Patent entitled "METHOD AND USER INTERFACE FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on July 31, 2002 as a continuation-in-part of Application No. 09/724,840 for United States Patent entitled, "METHOD AND SYSTEM FOR PROVIDING AN ELECTRONIC SYSTEM DESIGN WITH ENHANCED DEBUGGING CAPABILITIES," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000). No application number has been assigned for this continuation-in-part application yet.
5. Application No. 09/724,839 for United States Patent entitled "DESIGN INSTRUMENTATION CIRCUITRY," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
6. Application No. 09/724,585 for United States Patent entitled "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on November 28, 2000

(claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).

7. Application No. 10/212,128 for United States Patent entitled "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM USING INSTRUMENTATION CIRCUITRY AND A LOGIC ANALYZER," filed in the USPTO on July 31, 2002 as a continuation-in-part of Application No. 09/724,585 for United States Patent entitled, "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000). No application number has been assigned for this continuation-in-part application yet.

8. Provisional Application No. 60/168,266 for United States Patent entitled "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed in the U.S. Patent and Trademark Office ("USPTO") on November 30, 1999.

9. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed in the U.S. Patent and Trademark Office ("USPTO") on August 31, 2000.

10. Provisional Application No. 60/360,627 for United States Patent entitled, "HARDWARE-BASED HDL CODE COVERAGE AND DESIGN ANALYSIS," filed in the U.S. Patent and Trademark Office ("USPTO") on March 1, 2002.

11. Provisional Application No. 60/387,261 for United States Patent entitled, "ENHANCED HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE," filed in the U.S. Patent and Trademark Office ("USPTO") on June 7, 2002.

EXHIBIT D**Transferred Patents**

Reference is made to the Asset Purchase Agreement (the "Acquisition Agreement"), dated as of October 28, 2002, by and among Synplicity, Inc., a California corporation ("Synplicity" or "Buyer"), Bridges2Silicon, Inc., a Delaware Corporation ("Bridges" or "Seller"), and, solely for the purposes of Article IX of such Acquisition Agreement, Robert M. Gardner, and individual (the "Seller's Agent"). This Exhibit D is incorporated in the Acquisition Agreement by reference and made a part thereof. Capitalized terms used herein and not otherwise defined shall have the meanings ascribed to them in the Acquisition Agreement and/or the additional exhibits and/or attachments thereto, as the case may be.

Seller holds no registered Patents relating to the Products, the Business or the Technology. Pursuant to Section 1.1.2 of the Acquisition Agreement, Seller agrees to transfer, convey, assign, and deliver to the Buyer on the Closing Date all of Seller's right, title and interest in and to the following pending patent applications, continuations thereof in part, and provisional applications, as the case may be, that are related to the Products, the Business and the Technology:

1. Application No. 09/724,702 for United States Patent entitled "HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE," filed in the U.S. Patent and Trademark Office ("USPTO") on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
2. European Patent Application No.: 00982284.2 for "*HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE*," filed with the European Patent Office on November 29, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
3. Application No. 09/724,840 for United States Patent entitled, "METHOD AND SYSTEM FOR PROVIDING AN ELECTRONIC SYSTEM DESIGN WITH ENHANCED DEBUGGING CAPABILITIES," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).
4. Application No. 10/210,509 for United States Patent entitled "METHOD AND USER INTERFACE FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on July 31, 2002 as a continuation-in-part of Application No. 09/724,840 for United States Patent

entitled, "METHOD AND SYSTEM FOR PROVIDING AN ELECTRONIC SYSTEM DESIGN WITH ENHANCED DEBUGGING CAPABILITIES," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).

5. Application No. 09/724,839 for United States Patent entitled "DESIGN INSTRUMENTATION CIRCUITRY," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).

6. Application No. 09/724,585 for United States Patent entitled "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).

7. Application No. 10/212,128 for United States Patent entitled "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM USING INSTRUMENTATION CIRCUITRY AND A LOGIC ANALYZER," filed in the USPTO on July 31, 2002 as a continuation-in-part of Application No. 09/724,585 for United States Patent entitled, "METHOD AND SYSTEM FOR DEBUGGING AN ELECTRONIC SYSTEM," filed in the USPTO on November 28, 2000 (claiming priority of (i) U.S. Provisional Application No. 60/168,266 for United States Patent entitled, "INTERACTIVE DEBUGGING OF HDL SOURCE CODE," filed on November 30, 1999 and (ii) U.S. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed on August 31, 2000).

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9. Provisional Application No. 60/230,068 for United States Patent entitled, "HDL-BASED HARDWARE DEBUGGING," filed in the U.S. Patent and Trademark Office ("USPTO") on August 31, 2000.

10. Provisional Application No. 60/360,627 for United States Patent entitled, "HARDWARE-BASED HDL CODE COVERAGE AND DESIGN ANALYSIS," filed in the U.S. Patent and Trademark Office ("USPTO") on March 1, 2002.

11. Provisional Application No. 60/387,261 for United States Patent entitled, "ENHANCED HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE," filed in the U.S. Patent and Trademark Office ("USPTO") on June 7, 2002.