12-09-2002

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U.S. DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

Philsar Semiconductor, Inc.

12-2-02

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

3. Nature of conveyance:

[X] Assignment [ ] Merger
[ ] Security Agreement [ ] Change of Name
[ ] Other_____

Execution Date: June 25, 2002

2. Name and address of receiving party(ies)

Name: Washington Sub, Inc.

Internal Address: _____

Street Address: 4311 Jamboree Road

Newport Beach, CA., 92660-3095, USA
City:_____State:____Zip:_____

Additional name(s) & address(es) attached? [ ] Yes [X] No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:_____

A. Patent Application No.(s) 09/753,581
09/629,484 09/702,691

B. Patent No.(s) _____

Additional numbers attached? [ ] Yes [X] No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Shapiro Cohen

Internal Address:_____

Street Address: P.O. Box 3440
Station D
Ottawa, Ontario, Canada, K1P 6P1
City:_____State:____Zip:_____

6. Total number of applications and patents involved: 3

7. Total fee (37 CFR 3.41).....$ 120.00

[ ] Enclosed
[X] Authorized to be charged to deposit account

8. Deposit account number:
16-0600

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9. Signature.

12/06/2002 GTON11 00000045 160600 09753581
01 FC:8021 120.00 CH

Robert A. Wilkes
Name of Person Signing

Signature

29 Nov 02
Date

Total number of pages including cover sheet, attachments, and documents: 5

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

ASSIGNMENT OF INVENTIONS, PATENTS, PATENT APPLICATIONS AND TRADEMARKS

WHEREAS, PHILSAR SEMICONDUCTOR, INC ("Assignor"), a company organized under the laws of Canada, with an office at 146 Colonnade Road, Nepean, Ontario, Canada, K2E 7Y, owns or has rights to certain inventions, patents, patent applications and trademarks identified in the attached Schedule entitled "IP SCHEDULE B";

WHEREAS, WASHINGTON SUB, INC. ("Assignee"), a Delaware corporation with an office at 4311 Jamboree Road, Newport Beach, California 92660-3095, wishes to acquire full rights and ownership of said inventions, patents, patent applications and trademarks.

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor grants, conveys, assigns and transfers to the Assignee and the Assignee's successors and assigns, Assignee's entire right, title and interest in and to said inventions, patents, patent applications and trademarks listed on the attached Schedule identified as "IP SCHEDULE B", including all corresponding applications such as continuations, continuations-in-part, divisionals, provisionals, reissues, reexaminations, and foreign counterparts thereof, along with the subject matter of any and all claims which may be obtained in the aforementioned, in the United States and every foreign country, including all rights to profits and damages by reason of past infringement by any party or parties, with the right to sue and collect same for Assignee's, and Assignee's successors and assigns own use and benefit.

UPON SAID CONSIDERATION, Assignor appoints Assignee and Assignee's successors and assigns as its attorney-in-fact to act in Assignor's name and place to execute, deliver and record any document or instrument of assignment or conveyance necessary to perfect, grant, and confirm the rights granted herein, and Assignor conveys to the Assignee the right to make application, prosecute, receive and enforce in its own behalf and name the inventions, patents, patent applications and trademarks of "IP SCHEDULE B" in the United States and all foreign countries and to claim priority therefrom under the Patent Cooperation Treaty, the International Convention and/or any other international arrangement.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be duly executed by one of its officers on the date shown below.

PHILSAR SEMICONDUCTOR, INC.	WASHINGTON SUB, INC.
By Mohy F. Abdelgawy	By
Name Mohy F. Abdelgawy	Name Balakrishnan S. Iyer
Title VP - RF BU	Title

Date: June 25, 2002

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0758W (23-1)	Cdn patent appln	2,289,823 11/15/99		Published	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/ Filtering Radio Receiver Architecture for Low-IF or Zero-IF	Parent Canadian app; Published
00CXT0758W (23-2)	US patent appln	09/675,513 9/29/00		Pending	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/ Filtering Radio Receiver Architecture for Low-IF or Zero IF	Nationally filed US app; Pending
00CXT0758W (23-3)	PCT	PCT/CA00/01297 11/6/00		Inactive	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/Filtering Radio Receiver Architecture for Low-IF or Zero IF	PCT app; Inactive
00CXT0758W (23-3)	EPC			To Be Filed	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/Filtering Radio Receiver Architecture for Low-IF or Zero IF	EP app from PCT; To Be Filed
00CXT0759W (24-1)	Cdn patent appln			Closed/ Combined with 00CXT0756W		Calibration Means for Two-Point Modulation Scheme (Filiol; Riley; Martin Snelgrove)	Canadian app closed/combined with 00CXT0756W
00CXT0760W (25-1)	Cdn patent appln	2,288.495 11/2/99		Pending	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	Parent Canadian app; Pending
00CXT0760W (25-2)	US patent appln	09/702,691 11/1/00		Pending	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	Nationally filed US app; Pending
00CXT0760W (25-3)	PCT patent appln	00/01302 11/1/00		Inactive	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	PCT; Inactive

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0760W (25-4)	EPC			To Be Filed	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	EP app to be filed from PCT
00CXT0761W (26-1)	Cdn patent appln	2,295,435 1/6/00		Published	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Parent Canadian app; Published
00CXT0761W (26-2)	US patent appln	09/753,626 1/4/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Nationally filed US app; Pending
00CXT0761W (26-3)	PCT patent appln	01/00020 1/5/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	PCT app; Pending
00CXT0761W (26-4)	Taiwan patent appln	90100821 1/15/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Nationally filed Taiwan app; Pending
00CXT0762W (27-1)	Cdn patent appln	2,294,404		Published	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Parent Canadian app; Published
00CXT0762W (27-2)	US patent appln	09/753,581 1/4/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Nationally filed US app; Pending

IP SCHEDULE B

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0762W (27-3)	PCT patent appln	01/00019 1/5/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	PCT patant app; Pending
00CXT0762W (27-4)	Taiwan patent appln	90100820 1/15/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Nationally filed Taiwan app; Pending
00CXT0763W (28-1)	US patent appln	09/088,74 5 6/2/98		Pending	Balteanu	Balanced Mixer with a Feedback Preamplifier	Parent US patent app; Pending
00CXT0764W (29-1)	US patent appln	09/629,48 4 7/31/00		Pending	Riley	Frequency Synthesizer	Parent US patent app; Pending
00CXT0764W (29-2)	PCT patent appln	01/01093 7/30/01		Pending	Riley	Frequency Synthesizer	PCT patent app; Pending
00CXT0765W (30-1)	US patent appln	09/545,88 7 4/7/00		Pending	Beriault	ESD Protection in Mixed Signal ICS	Parent US patent app; CPA filed 2/26/02; Pending
01CXT0166W (31-1)	US patent appln	10/008,44 2 6-Dec-2001		Pending	Balteanu; Gheorghe	Low Power Bandgap Circuit	Parent US patent app; Pending
00CXT0800W (32-1)	US patent appln			Unfiled	Cojocaru	Low-Voltage Bipolar Current Mode Logic (CML) Family Using Schottky Diodes	Parent US patent app; Assigned /Unfiled