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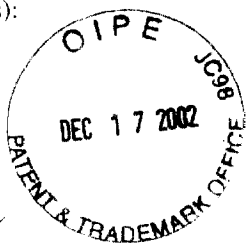
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102319102

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

STMicroelectronics N.V.



2. Name and address of receiving party(ies):

AMI Semiconductor Belgium BVBA

Westerring 15

B-9700 Oudenaarde, Belgium

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment☐ Merger☐ Security Agreement☐ Change of Name☐ Other

Execution Date: June 26, 2002

Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)

See attached list

B. Patent No.(s)

See attached list

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:

SUGHRUE MION, PLLC

2100 Pennsylvania Avenue, N.W.

Suite 800

Washington, D.C. 20037-3213

6. Total number of applications and patents involved:

7

7. Total fee (37 CFR 3.41): \$280.00

☒ Enclosed.☐ Authorized to be charged to Deposit Account No. 19-4880.

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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

David J. Cushing

Reg. No. 28,703

December 17, 2002

Date

Total number of pages including cover sheet, attachments, and documents: 14

Mail documents to be recorded with required cover sheet information to:

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Box Assignment

Washington, D.C. 20231

12/20/2002 DBYRNE 00000043 09897075

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DJC - ID - 053602

PATENT
REEL: 013589 FRAME: 0189

LIST OF U.S. APPLICATIONS/PATENTS TO BE TRANSFERRED

U.S. Applications

1. 09/897,075
2. 09/708,711
3. 09/652,788
4. 09/950,835
5. 09/768,151
6. 60/286,826

U.S. Patents

7. 5,661,432

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PATENT ASSIGNMENT OF RIGHTS

THIS PATENT ASSIGNMENT is made by STMicroelectronics N.V., a Dutch corporation with its principal place of business located at Strawinskylaan 1725, Tower B 17th floor, 1077 XX Amsterdam, The Netherlands acting for purposes of this Agreement through its Swiss branch located at 20 route de Pré-Bois, ICC – Bloc A, 1215 Geneva 15, Switzerland (“**Assignor**”) to AMI Semiconductor Belgium BVBA, a Belgian company, whose registered office is at Westering 15, B-9700 Oudenaarde, Belgium (“**Assignee**”).

WHEREAS, Alcatel, a French société anonyme, having its principal place of business at 54, rue la Boétie, 75008, Paris, France (“**Alcatel**”) and Assignor have entered on June 26, 2002 into a “Patent Transfer and License Agreement” transferring to Assignor certain patents of Alcatel;

WHEREAS, Assignee and Assignor have entered into that certain Business Purchase Agreement, dated as of May 8, 2002 (the “**Agreement**”), pursuant to which Assignor has agreed to sell and assign, and Assignee has agreed to buy and acquire, certain assets associated with the MSB Business acquired by Assignor from Alcatel Bell NV a Belgian company;

WHEREAS, pursuant to Section 2.1 of the Agreement, Assignor desires to assign to Assignee all of Assignor's right, title and interest in and to the patents and patent applications set forth on Exhibit A, attached hereto (the “**Patents**”).

NOW, THEREFORE, in consideration of entering into the Agreement and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor does hereby sell, assign, set over and transfer to Assignee, its successors and assigns all of Assignor's entire right, title and interest in and to the Patents, including any divisions, continuations, continuations-in-part, renewals, extensions or reissues thereof, and all rights of priority resulting from the filing of the Patents, and any and all applications for patent and patents issuing therefrom in any and all countries of the world, including all divisions, reissues, continuations, continuations-in-part, renewals, extensions and extensions thereof, and all rights of priority resulting from the filing of the respective applications for said Patents identified above, the same to be held and enjoyed by Assignee for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms for which the Patents are or may be granted or reissued as fully and entirely as the same would have been held and enjoyed by the Assignor if this Assignment and sale had not been made; together with all claims for damages by reason of past infringements of the Patents with the right to sue for and collect the same for its own use and benefit, and for the use and on behalf of its successors, assigns and other legal representatives; provided, however, Assignee will be responsible for those costs and expenses reasonably incurred by Assignor in carrying out Assignor's obligations pursuant to this paragraph.

Assignor agrees that, on request and without further consideration, Assignor will communicate to Assignee or its representatives or nominees any facts known to

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Assignor respecting the Patents and the inventions set forth therein, and will at Assignee's expense testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing, continuing-in-part, reissue applications and renewals and extensions, make all rightful oaths and generally do everything reasonably requested by Assignee to aid Assignee to obtain, maintain, and enforce patent protection in any country for the inventions set forth in the Patents. To the extent that any of the foregoing is required of Alcatel, Assignor agrees to use reasonable efforts to cause Alcatel to do so pursuant to the Patent Transfer and License Agreement.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer on this 26th day of June, 2002.

STMicroelectronics N.V.

By: 

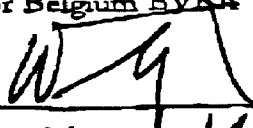
Name:

Title:

Alain Guilleul
Corp V.P.

Assignee,

AMI Semiconductor Belgium BVBA

By: 

Name:

Title:

Walter Matthies
Managing Director.

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EXHIBIT A

AME PORTFOLIO

Reference	Title as filed Short Title (internal use)	Ter.	Application No.	Filing Date	Publication No.	Publication Date	Patent No.	Grant Date
94330		EP	94200854.1	29/03/1994	680151	02/11/1995	680151	14/06/2000
18337	Chopping amplifier DISPOSITIF DE REGLAGE AUTOMATIQUE DE NIVEAU D'UN SIGNAL Device for automatic control of signal level	AT	92 400 796.6	24/03/1992			0 506 547	10/05/1995
		BE	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		CH	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		DE	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		EP	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		ES	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		FR	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		GB	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		IT	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		NL	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
		SE	92 400 796.6	24/03/1992	0 506 547	30/09/1992	0 506 547	10/05/1995
91937	Schaltungsanordnung zur A/D Wandlung mit Filtern zur Bandbegrenzung Filter For A/D Converter	DE	P3605928.5	25/02/1986			3605928	17/02/1994
120445	METHOD AND DEVICE GENERATING IN...	EP	2290192	1/29/02				

Agreed by ST Microelectronics N.V.

Francis Guibert
By: Francis Guibert
Title:

Update : June 14, 2002

92162	Schaltungsanordnung zur Entkopplung des Ausgangs eines Spannungswandlers isolation network	DE	P3705249.7	19/02/1987			3705249	16/01/1990
93226	Filter for A/D Converter Integrierter oder hybrider bipolarer oder bipolar-MOS-Halbleiterschaltkreis	DE	P4110007.7	27/03/1991				
93796	Offset-Voltage Reduction Metallische Kontaktflächen auf einem Halbleitersubstrat	DE	P4232814.4	30/09/1992				
94604	Semiconductor Contacts Linear tunable GM-C integrator	EP	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		DE	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		ES	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		FR	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		GB	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		IT	95200330,9	10/02/1995	726652	14/08/1996	726652	17/10/2001
		US	588345	18/01/1996			5661432	26/08/1997
120277	REFERENCE VOLTAGE GENERATOR WITH MONITORING AND START UP MEANS. LOW-POWER CMOS BANDGAP REFERENCE.	EP	99401555	22/06/1999	1063578	27/12/2000		

PATENT

REEL: 013589 FRAME: 0195

AME PORTFOLIO

120281	VOLTAGE GENERATING CIRCUIT CHARGE PUMP WITH POSITIVE FEEDBACK.	EP	99402133,5	26/08/1999	1079506	28/02/2001	
120283	REGULATOR FOR SINE WAVE GENERATOR AND SINE WAVE GENERATOR UNIT INCLUDING SUCH A REGULATOR. CURRENT SINE WAVE GENERATOR.	EP	99402881,9	19/11/1999	1104109	30/05/2001	
120294	INTEGRATED SINE WAVE GENERATING CIRCUIT DRIVERS ON CHIP INTEGRATED SOLUTION.	EP	402008,7	12/07/2000	1172931	16/01/2002	
		AU	54147/01	29/06/2001			
		CA	2353003	10/07/2001		12/01/2002	
		IL	143930	21/06/2001			
		JP	2001-203320	04/07/2001	2002-125382	26/04/2002	
		KR	10-2001-41889	12/07/2001			
		SG	2001042774-6	12/07/2001			
		TW	90117251	13/07/2001			
		US	09/897075	03/07/2001	02-0017945-A	14/02/2002	

120309	TRANSDUCER INTERFACE ARRANGEMENT INCLUDING A SIGMA-DELTA MODULATOR WITH OFFSET CORRECTION AND WITH GAIN SETTING.	EP	99402897,5	19/11/1999	1102405	23/05/2001	
	SIGMA DELTA MODULATOR WITH GAIN AND OFFSET SETTING.						
		JP	2000-346047	14/11/2000	2001-196931	19/07/2001	
		US	09/708711	09/11/2000			
120363	METHOD FOR PROCESSING CONDUCTIVE LAYER STRUCTURES AND DEVICES INCLUDING SUCH CONDUCTIVE LAYER STRUCTURES.	EP	99402187,1	03/09/1999	1081537	07/03/2001	
	LIGHT SHIELD FOR A MICRO- DISPLAY LIGHT VALVE.						
		JP	2000-249267	21/08/2000	2001-133811	18/05/2001	
		TW	89102976	21/02/2000			
		US	09/652788	31/08/2000			

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120400	METHOD OF PROCESSING A HIGH VOLTAGE P + + /N-WELL JUNCTION AND DEVICE OBTAINED THEREOF.	EP	402501,1	08/09/2000	1189276	20/03/2002	
	HIGH BREAKDOWN VOLTAGE DRAIN JUNCTION FOR USE IN SUBMICRON CMOS PROCESSES.						
		JP	2001-260875	30/08/2001			
		KR	10-2001-54427	05/09/2001			
		TW		08/09/2000			
		US	09/950835	10/09/2001			
120524	METHOD FOR TUNGSTEN CHEMICAL VAPOR DEPOSITION ON A SEMICONDUCTOR SUBSTRATE.	EP	403705,7	28/12/2000	1219725	03/07/2002	
	A NOVEL ONE-STEP TUNGSTEN CHEMICAL VAPOR DEPOSITION PROCESS FOR METAL INTERCONNECTS.						
		CN	1144080,5	28/12/2001			
		JP	2001-393381	26/12/2001			
		US	09/768151	24/01/2001	3630	04/07/2002	

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120554	PROCESS FOR SELECTIVE EPITAXIAL GROWTH AND BIPOLAR TRANSISTOR MADE BY USING SUCH PROCESS SELECTIVE EPITAXY.	EP	1401908,7	16/07/2001				
120583	CHARGE PUMP CIRCUIT. VOLTAGE AND CURRENT CONTROL FOR CHARGE PUMP.	EP	1401637,2	20/06/2001				
120594	LAYOUT CONFIGURABLE ELECTROSTATIC DISCHARGE DEVICE FOR INTEGRATED CIRCUITS	EP	2290153,2	21/01/2002				
	ESD PROTECTION	US	60/286,826	27/04/2001				
		EP	98 440 298.2	23/12/1998	0 929 168	14/07/1999		
		ES	98 440 298.2	23/12/1998				
		FR	98 440 298.2	23/12/1998				
		GB	98 440 298.2	23/12/1998				
		IT	0 98 A 000 007	07/01/1998			1 301 114	09/06/2000

17636	CIRCUIT DE MESURE DU NIVEAU D'UN SIGNAL ELECTRIQUE COMPRENANT DES MOYENS DE CORRECTION DE DECALAGE ET APPLICATION AUX AMPLIFICATEURS A COMMANDE... Signal level measuring circuit	AT	90 124 567.0	18/12/1990	0 452 557	23/10/1991	0 452 557	28/09/1994
120709	SEMICONDUCTOR STRUCTURE AND METHOD FOR PROCESSING SUCH A STRUCTURE. DEEP TRENCH ISOLATION FOR HIGH VOLTAGE DMOS.	EP	2290902,2	11/04/2002				
120654	METHOD FOR REDUCING A RESIDUAL ELECTRIC CHARGE CREATED BY A PREVIOUS PROCESS STEP ON A CONDUCTIVE STRUCTURE. METHOD OF REDUCING A RESIDUAL ELECTRIC CHARGE ON CONDUCTIVE STRUCTURES DURING TREATMENT IN PLASMA.	EP	1403276,7	17/12/2001				

PATENT

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Update : June 14, 2002

120632	METHOD FOR MAKING INTERCONNECT STRUCTURES METHOD FOR PREVENTING ELECTROCHEMICAL EROSION OF INTERCONNECTED STRUCTURES.	EP	1403275,9	17/12/2001			
120681	PROTECTION CIRCUIT PROTECTING AGAINST VOLTAGE IRREGULARITIES. ON CHIP REVERSE BATTERY PROTECTION.	EP	2291010,3	22/04/2002			
120691	MULTIPLEX TRANSMISSION SYSTEM WITH IN-CIRCUIT ADDRESSING. IN-CIRCUIT ADDRESS ASSIGNMENT FOR MULTIPLEX BUSES.	EP	1403234,6	13/12/2001			
120692	MULTIPLEX BUS SYTEM WITH DUTY CYCLE CORRECTION. DUTY-CYCLE CORRECTION AS PART OF THE CLOCK SYNCHRONISATION.	EP	2290332,2	11/02/2002			

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120591	EMC IMMUNE LOW DROP REGULATOR.	EP	1402035,8	26/07/2001				
120592	EMC IMMUNE LOW DROP REGULATOR. LOW DROP VOLTAGE REGULATOR. LOW DROP (LD) REGULATOR.	EP	14Q2036,6	26/07/2001				
91303	Verfahren zum Herstellen eines DMOS-Transistors HIGH VOLTAGE SWITCH	AT	84106690,5	12/06/1984	133204	20/02/1985	133204	09/09/1987

RECORDED: 12/17/2002

PATENT
REEL: 013589 FRAME: 0202

Update : June 14, 2002