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Execution Date: May 22, 1992

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A. Patent Application No.(s)
10/086,197 (.0170009)

B. Patent No.(s)
5,497,499 (.0170001)
5,737,624 (.0170004)
5,974,526 (.0170005)
6,289,433 (.0170007)

Additional numbers attached? ☐ yes ☒ no

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: **Sterne, Kessler, Goldstein & Fox P.L.L.C.**

Internal Address: c/o Thomas C. Fiala

Street Address: 1100 New York Ave., N.W.

City: Washington State: D.C. Zip Code: 20005-3934

6. Total number of applications and patents involved: 5

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ASSIGNMENT
(Corporate)

S MOS SYSTEMS, INC. a California corporation, having a principal place of business at 2460 North First Street, San Jose, California 95131-1002 (hereafter the "Assignor"), is the owner by respective assignments of United States patent applications identified below (hereafter sometimes called the "Patent Applications").

SEIKO EPSON CORPORATION, a corporation of Japan, having a place of business at 4-1 Nishishinjuku 2-chome, Shinjuku-ku Tokyo-to, Japan (hereafter the "Assignee"), desires to acquire all of the rights to the Patent Applications and all inventions described and claimed therein.

THEREFORE, in consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to it, Assignor hereby sells and assigns to the Assignee the entire right, title and interest in and to the Patent Applications identified below, and all inventions described and claimed therein, in any and all Letters Patent(s) therefor, and in any and all reissues, extensions, renewals, reexaminations, divisions and continuations of such applications or Letters Patent(s) to the full end of the term or terms for which such Letters Patent(s) issue, such entire right, title and interest to be held and enjoyed by the above-named Assignee the same as they would have been held and enjoyed by the Assignor had this assignment and sale not been made.

ATTY DOCKET	SER. NO.	FILING DATE	TITLE
SP010	07/877,562	05/01/92	64-Bit Floating Point Multiplier
SP014	07/726,929	07/08/91	Single Chip Page Printer Controller
SP015	07/727,006	07/08/91	High Performance RISC Microprocessor Architecture
SP016	07/726,893	07/08/91	Microprocessor Architecture Capable of Supporting Multiple Heterogeneous Processors
SP019	07/726,942	07/08/91	RISC Microprocessor Architecture Implementing Fast Trap and Exception Handling
SP021	07/727,058	07/08/91	Extensible RISC Microprocessor Architecture
SP022	07/727,744	07/08/91	RISC Microprocessor Architecture With Isolated Architecture Dependencies
SP024	07/802,816	12/06/91	ROM with SRAM and CRC
SP025	07/853,604	03/18/92	Dual Width Memory Subsystem
SP027	07/798,917	11/27/91	Printer Video Processor
SP028	07/798,704	11/27/91	Orthogonal Rotator
SP029	07/798,705	11/27/91	Pixel Modification Unit
SP030	07/862,623	03/31/92	Virtual FIFO Peripherals Interface
SP031	07/805,838	12/13/91	Semaphore Bypass

TERNE, KESSLER, GOLDSTEIN & FOX
ATTORNEYS AT LAW
888 CONNECTICUT AVENUE
WASHINGTON, D. C. 20036
(202) 408-0800

SP032	07/857,599	03/31/92	CISC to RISC Microprocessor Decode Unit
SP035	07/860,719	03/31/92	Instruction Scheduling
SP038	07/877,451	05/01/92	Instruction Retirement
SP039	07/861,417	03/31/92	App. For Generating 3D Color Images...
SP040	07/867,637	04/13/92	High Density Memory Architecture
SP041	07/860,718	03/31/92	Floor Plan Layout for Register Renaming Check
SP044	07/833,419	02/10/92	Automatic Power Slit Generation
SP045	07/860,717	03/31/92	Selective Power Down For High Performance CPU/System
SP046	07/831,272	02/07/92	Hardware Accelerator with Real Silicon Components
SP047	07/844,066	03/02/92	Clock Generation
SP049	07/817,813	01/08/92	Single Chip Page Printer Controller
SP050	07/817,810	01/08/92	High Performance RISC Microprocessor Architectureance
SP051	07/817,811	01/08/92	RISC Microprocessor Architecture Implementing Fast Trap and Exception Handling
SP052	07/817,809	01/08/92	Extensible RISC Microprocessor Architecture
SP053	07/817,807	01/08/92	RISC Microprocessor Architecture With Isolated Architecture Dependencies
SP054	07/846,237	03/05/92	Register File Backup Queue
SP055	07/844,494	03/04/92	Dual Output Reset Circuit
SP056	07/846,231	03/06/92	Elimination of the Critical Path in Memory Control Unit and Input/Output Control Unit Operations
SP074	07/833,422	02/10/92	Single Chip Page Printer Controller

By its undersigned representative, the Assignor agrees

a. to execute all papers necessary in connection with the Patent Applications and any continuing, divisional, reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient;

b. to execute all papers necessary in connection with any interference which may be declared concerning the Patent Applications or any continuation, division, reissue or reexamination thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference; and

STERNE, KESSLER, GOLDSTEIN & FOX
ATTORNEYS AT LAW
1100 CONNECTICUT AVENUE
WASHINGTON, D.C. 20036
(202) 466-0800

c. to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee on any of the Patent Applications and on any continuation, division, reissue or reexamination of any of the Patent Applications.

The Assignor hereby covenant(s) that it has the full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict therewith.

Assignor and Assignee hereby grant Robert Greene Sterne, Esquire, Registration No. 28,912, Edward J. Kessler, Registration No. 25,688, Jorge A. Goldstein, Registration No. 29,021, and Samuel L. Fox, Registration No. 30,353 of STERNE, KESSLER, GOLDSTEIN & FOX, 1225 Connecticut Avenue, Washington, D.C. 20036, power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

IN WITNESS WHEREOF, executed by the Assignor's undersigned representative on the date following the undersigned's name.

S MOS SYSTEMS, INC.

By: 

Shuji Kato
Print Name

Executive Vice-President
Title

May 22, 1992
Date

smos/1397-000.asn

ERNE, KESSLER,
LDSTEIN & FOX
ATTORNEYS AT LAW
5 CONNECTICUT AVENUE
SHINGTON, D. C. 20036
(202) 466-0800