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To the Honorable Commissioner of Patents and Trademarks: Please Record the attached original documents or copy thereof.

1. Name of conveying party(ies):
Philsar Semiconductor, Inc.

Additional name of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: Washington Sub, Inc.

Internal Address:

Street Address: 4311 Jamboree Road

City: Newport Beach State: CA Zip: 92660

Additional Name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other ____

Execution Date: June 25, 2002

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: ____

A. Patent Application No.(s)

B. Patent No.(s)
6,329,939

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning this document should be mailed:

Name: Daniel J. Santos

Internal Address:

Street Address: 600 Village Trace, Suite 300

City: Marietta State: GA Zip: 30067

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41) . . . . . $ 40.00

☐ Enclosed

☒ Authorized to be charged to deposit account

8. Deposit account number:

501513

(Attach duplicate copy of this page if paying by deposit account)

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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Daniel J. Santos
Name of Person Signing

Signature

Jan 22, 2004
Date

Total number of pages including cover sheet, attachments, and documents: 14

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

CH $40.00 501513 6329939

ASSIGNMENT OF INVENTIONS, PATENTS, PATENT APPLICATIONS AND TRADEMARKS

WHEREAS, PHILSAR SEMICONDUCTOR, INC ("Assignor"), a company organized under the laws of Canada, with an office at 146 Colonnade Road, Nepean, Ontario, Canada, K2E 7Y, owns or has rights to certain inventions, patents, patent applications and trademarks identified in the attached Schedule entitled "IP SCHEDULE B";

WHEREAS, WASHINGTON SUB, INC. ("Assignee"), a Delaware corporation with an office at 4311 Jamboree Road, Newport Beach, California 92660-3095, wishes to acquire full rights and ownership of said inventions, patents, patent applications and trademarks.

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor grants, conveys, assigns and transfers to the Assignee and the Assignee's successors and assigns, Assignee's entire right, title and interest in and to said Inventions, patents, patent applications and trademarks listed on the attached Schedule identified as "IP SCHEDULE B", including all corresponding applications such as continuations, continuations-in-part, divisionals, provisionals, reissues, reexaminations, and foreign counterparts thereof, along with the subject matter of any and all claims which may be obtained in the aforementioned, in the United States and every foreign country, including all rights to profits and damages by reason of past infringement by any party or parties, with the right to sue and collect same for Assignee's, and Assignee's successors and assigns own use and benefit.

UPON SAID CONSIDERATION, Assignor appoints Assignee and Assignee's successors and assigns as its attorney-in-fact to act in Assignor's name and place to execute, deliver and record any document or instrument of assignment or conveyance necessary to perfect, grant, and confirm the rights granted herein, and Assignor conveys to the Assignee the right to make application, prosecute, receive and enforce in its own behalf and name the inventions, patents, patent applications and trademarks of "IP SCHEDULE B" in the United States and all foreign countries and to claim priority therefrom under the Patent Cooperation Treaty, the International Convention and/or any other international arrangement.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be duly executed by one of its officers on the date shown below.

PHILSAR SEMICONDUCTOR, INC.

By Mohy F. Abdelgawy

Mohy F. Abdelgawy
Name

VP - RF BU
Title

WASHINGTON SUB, INC.

By

Balakrishnan S. Iyer
Name

Title

Date: June 25, 2002

IP SCHEDULE B
(6/04/02)

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0736W (1-1)	Cdn patent appln	2,204,455 5/5/97		Abandoned	Beriault; Lussier	Base Station for Local Area Network	Abandoned
00CXT0736W (1-2)	US patent appln	09/071,937 5/5/98		Abandoned	Beriault; Lussier	Base Station for Local Area Network	Abandoned
00CXT0737W 2-1	Cdn patent appln			Closed/Not Assigned	Not available	International Fax/Voice Mail Product	Closed/Not Assigned
00CXT0738W 3-1	Cdn patent appln			Closed/Not Assigned	Not available	Integrated GPS Receiver on a Chip	Closed/Not Assigned
00CXT0739W (4-1)	Cdn preliminary patent appln	2,209,509 8/1/97		Abandoned	Yu; Snelgrove	Mismatch Cancellation for Complex Bandpass Sigma-Delta Modulations	Preliminary app; Aban in favor of Canadian Utility 2,244,446
00CXT0739W (4-2)	Cdn patent appln	2,244,446 7/31/98		Pending	Yu; Snelgrove	Signal Processor for Reducing Undesirable Signal Content	Parent Canadian app; Pending
00CXT0739W (4-3)	US patent appln	09/127,844 8/3/98		Pending	Yu; Snelgrove	Signal Processor for Reducing Undesirable Signal Content	Nationally filed in US; Pending

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0740W (5-1)	Cdn preliminary patent appln	2,213,156 8/15/97		Abandoned	Cojocaru; Varelas; Cloutier; Lussier	One Bit Digital Quadrature Vector Modulator	Preliminary app; Aban in favor of Canadian Utility 2,245,072
00CXT0740W (5-2)	Cdn patent appln	2,245,072		Published	(Cojocaru; Varelas; Cloutier; Lussier)	One Bit Digital Quadrature Vector Modulator	Parent Canadian app; Published
00CXT0740W (5-3)	US patent appln US patent	09/135,243 8/17/98	6,339,621 1/15/02	Issued	(Cojocaru; Varelas; Cloutier; Lussier)	One Bit Digital Quadrature Vector Modulator	Nationally filed in US; Issued
00CXT0741W (6-1)	Cdn preliminary patent appln	2,229,737 2/18/98		Published	Swaminathan; MacRobbie; Snelgrove	Analog to Digital Converter for Radio Applications	Preliminary app; Aban in favor of Canadian Utility 2,262,209
00CXT0741W (6-2)	Cdn patent appln	2,262,209 2/18/99		Published	Swaminathan; MacRobbie; Snelgrove	Method and Apparatus for Minimizing Mismatch in A Complex Filter	Parent Canadian app; Published
00CXT0741W (6-3)	US patent application US Patent	09/252,381 2/18/99	6,329,939 12/11/01	Issued	Swaminathan; MacRobbie; Snelgrove	Method and Apparatus for Minimizing Mismatch in A Complex Filter	Nationally filed in US; Issued

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0742W (7-1)	Cdn preliminary patent appln	2,224,261 12/9/97		Abandoned	Cloutier	Low Phase Noise, High Q, High Gain Amplifier in an Integrated Circuit	Preliminary app; Aban in favor of Canadian Utility 2,280,878
00CXT0742W (7-2)	Cdn patent	2,280,878 12/9/98	2,280,878 2/5/02	Issued	Cloutier	An Amplifier for Continuous High Gain, Narrowband Signal Amplification	Parent Canadian app; Issued
00CXT0742W (7-3)	US patent appln	09/209,051 12/9/98	6,057,735 5/2/00	Issued	Cloutier	An Amplifier for Continuous High Gain, Narrowband Signal Amplification	Filed in US via PCT app; Issued
00CXT0742W (7-4)	PCT appln	PCT/CA98/01123		Inactive	Cloutier	An Amplifier for Continuous High Gain, Narrowband Signal Amplification	PCT app; Inactive
00CXT0742W (7-5)	Japanese patent appln	11-529559 21/9/98		Pending	Cloutier	An Amplifier for Continuous High Gain, Narrowband Signal Amplification	Japanese app filed via PCT; Pending
00CXT0742W (7-6)	German patent appln	19882089.5 12/9/98		Published	Cloutier	An Amplifier for Continuous High Gain, Narrowband Signal Amplification	German app filed via PCT; Published

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0743W (8-1)	Cdn patent appln	2,225,910 12/24/97		Published	Lussier; Bériault; Glandon	Audio Recording and Playback System	Parent Canadian app; Published; Abandoned
00CXT0743W (8-2)	US patent appln	09/220,625 12/24/98		Abandoned	Lussier; Bériault; Glandon	Audio Recording and Playback System	Nationally filed in US; Abandoned
00CXT0744W (9-1)	Cdn preliminary patent appln	2,233,8313/31/98		Abandoned	Riley	Delta-Sigma Fractional-N Synthesizer	Preliminary app; Aban in favor of Canadian Utility 2,267,496
00CXT0744W (9-2)	Cdn patent appln	2,267,496 3/30/99		Published	Riley	A Fractional-N Divider Using a Delta-Sigma Modulator	Parent Canadian app; Published
00CXT0744W (9-3)	US patent appln	09/281,854 3/31/99	6,236,703 5/22/01	Issued	Riley	A Fractional-N Divider Using a Delta-Sigma Modulator	Nationally filed in US; Issued
00CXT0745W (10-1)	Cdn Preliminary patent appln	2,229,756 2/18/98		Abandoned	Swaminathan; Snelgrove; MacRobbie	Method and Apparatus for Correcting Element Mismatch in Digital-to-Analog Converters	Preliminary app; Abandoned
00CXT0746W (11-1)	Cdn patent appln			Closed	Lussier; O'Neil	Radio PCS/GPS Solution	Closed per IRC

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Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0747W (12-1)	Cdn patent appln			Closed	MacRobbie	Digital Gain Control in Sigma-Delta Modulators via Reference and/or Input Modulation Using Sigma-Delta Techniques	Closed per IRC
00CXT0748W (13-1)	Cdn patent appln	2,229,756 2/18/98		Published	Swaminathan	Method and Apparatus for Correcting Element Mismatch in Bandpass Digital-to-Analog Converters	Parent Canadian app; Published
00CXT0749W (14-1)	Cdn preliminary patent appln	2,253,090 11/9/98		Abandoned	Cloutier	Inverted Super Regenerative Receiver	Preliminary app; Aban in favor of Canadian Utility 2,289,345
00CXT0749W (14-2)	Cdn patent appln	2,289,345 11/9/99		Published	Cloutier	Inverted Super Regenerative Receiver	Parent Canadian app; Published
00CXT0749W (14-3)	US patent appln	09/435,647 11/9/99		Pending	Cloutier	Inverted Super Regenerative Receiver	Nationally filed in US; Pending

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0750W (15-1)	Cdn preliminary patent appln	2,260,456 1/27/99		Abandoned	Swaminathan; Cloutier; Cherry	A Frequency-Locked Loop with Gated Reference and VCO Inputs	Preliminary app; Aban in favor of Canadian Utility 2,290,862
00CXT0750W (15-3)	Cdn patent appln	2,290,862 11/25/99		Published	Swaminathan; Cloutier; Cherry)	A Frequency/ Phase Comparison Circuit with Gated Reference and Signal Inputs	Parent Canadian app; Published
00CXT0750W (15-2)	US patent appln	09/491,875 1/27/00		Pending	Swaminathan; Cloutier; Cherry	A Frequency/ Phase Comparison Circuit with Gated Reference and Signal Inputs	Nationally filed in US; Pending
00CXT0751W (16-1)	Cdn preliminary patent appln	2,260,717 2/4/99		Abandoned	Birkett; Snelgrove; MacRobbie	A WCDMA Integrated Circuit Chip Set	Preliminary app; Abandoned
00CXT0752W (17-1)	Cdn patent appln			On-Hold/Not Assigned	Riley; Balteanu; Namdar	Linear Low Noise PLL	On-Hold per IRC; Not Assigned

IP SCHEDULE B

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0753W (18-1)	Cdn patent appln	2,298,310 2/9/00		Published	Balteanu; Cherry	Low Voltage Transconductance Amplifier/ Filters	Parent Canadian app; Published
00CXT0753W (18-2)	US patent appln	09/676,597 9/29/00		Pending	Balteanu; Cherry	Low Voltage Transconductance Amplifier/ Filters	Nationally filed US app; Pending
00CXT0753W (18-3)	PCT appln	PCT/CA01/00132 2/9/01		Published	Balteanu; Cherry	Low Voltage Transconductance Amplifier/ Filters	PCT; Published
00CXT0754W (19-1)	Cdn patent appln			Closed/Not Assigned	Cojocaru	Low Voltage Technique for a Voltage Control Oscillator	Closed; Not Assigned
00CXT0755W (20-1)	Cdn patent appln	2,284,948 10/4/99		Published	Birkett; Filiol; Riley)	Comptex Phase-Locked Loop Demodulator for Low-IF and Zero-IF Radio Receivers	Parent Canadian app; Published
00CXT0755W (20-2)	US patent appln	09/676,233 9/29/00		Pending	Birkett; Filiol; Riley	Complex Phase-Locked Loop Demodulator for Low-IF and Zero-IF Radio Receivers	Nationally filed US app; Pending

IP SCHEDULE B

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0756W (21-1)	Cdn patent appln	2,281,522 9/10/99		Published	Filiol; Riley; Cloutier; Cojocaru; Balteanu	Delta-Sigma Based Dual-Port Modulation Scheme And Calibration Techniques For Similar Modulation Schemes	Parent Canadian app; Published
00CXT0756W (21-2)	US patent appln	09/628,330 7/28/00		Pending	Filiol; Riley; Cloutier; Cojocaru; Balteanu	Delta-Sigma Based Dual-Port Modulation Scheme And Calibration Techniques For Similar Modulation Schemes	Nationally filed US app; Pending
00CXT0757W (22-1)	Cdn patent appln	2,296,209 1/17/00		Pending	Payer; Birkett	Method and Apparatus for Dynamically Generating Multiple Level Decision Thresholds of an M-ary Coded Signal	Parent Canadian app; Pending
00CXT0757W (22-2)	US patent appln	09/676,235 9/29/00	6,317,062 11/13/01	Issued	Payer; Birkett	Method and Apparatus for Dynamically Generating Multiple Level Decision Thresholds of an M-ary Coded Signal	Nationally filed US app; Issued

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Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0758W (23-1)	Cdn patent appln	2,289,823 11/15/99		Published	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/ Filtering Radio Receiver Architecture for Low-IF or Zero-IF	Parent Canadian app; Published
00CXT0758W (23-2)	US patent appln	09/675,513 9/29/00		Pending	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/ Filtering Radio Receiver Architecture for Low-IF or Zero IF	Nationally filed US app; Pending
00CXT0758W (23-3)	PCT	PCT/CA00/01297 11/6/00		Inactive	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/Filtering Radio Receiver Architecture for Low-IF or Zero IF	PCT app; Inactive
00CXT0758W (23-3)	EPC			To Be Filed	Birkett; Cherry; Snelgrove; Balteanu	Complex AGC/Filtering Radio Receiver Architecture for Low-IF or Zero IF	EP app from PCT; To Be Filed
00CXT0759W (24-1)	Cdn patent appln			Closed/ Combined with 00CXT0756W		Calibration Means for Two-Point Modulation Scheme (Filiol; Riley; Martin Snelgrove)	Canadian app closed/combined with 00CXT0756W
00CXT0760W (25-1)	Cdn patent appln	2,288.495 11/2/99		Pending	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	Parent Canadian app; Pending
00CXT0760W (25-2)	US patent appln	09/702,691 11/1/00		Pending	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	Nationally filed US app; Pending
00CXT0760W (25-3)	PCT patent appln	00/01302 11/1/00		Inactive	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	PCT; Inactive

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0760W (25-4)	EPC			To Be Filed	Dell'Aera	Radio Calibration by Correcting the Crystal Frequency	EP app to be filed from PCT
00CXT0761W (26-1)	Cdn patent appln	2,295,435 1/6/00		Published	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Parent Canadian app; Published
00CXT0761W (26-2)	US patent appln	09/753,626 1/4/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Nationally filed US app; Pending
00CXT0761W (26-3)	PCT patent appln	01/00020 1/5/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	PCT app; Pending
00CXT0761W (26-4)	Taiwan patent appln	90100821 1/15/01		Pending	Riley	Linear Low Noise Phase Locked Loop Frequency Synthesizer Using Controlled Divider Pulse Widths	Nationally filed Taiwan app; Pending
00CXT0762W (27-1)	Cdn patent appln	2,294,404		Published	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Parent Canadian app; Published
00CXT0762W (27-2)	US patent appln	09/753,581 1/4/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Nationally filed US app; Pending

IP SCHEDULE B

Conexant Docket No.	Type	App. No./ File Date	Pat. No./ Issue Date	Status	Inventor(s)	Title	Comments
00CXT0762W (27-3)	PCT patent appln	01/00019 1/5/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	PCT patant app; Pending
00CXT0762W (27-4)	Taiwan patent appln	90100820 1/15/01		Pending	Kwasniewski; Lepley; Riley	Delta-Sigma Modulator for Fractional-N Frequency Synthesis	Nationally filed Taiwan app; Pending
00CXT0763W (28-1)	US patent appln	09/088,74 5 6/2/98		Pending	Balteanu	Balanced Mixer with a Feedback Preamplifier	Parent US patent app; Pending
00CXT0764W (29-1)	US patent appln	09/629,48 4 7/31/00		Pending	Riley	Frequency Synthesizer	Parent US patent app; Pending
00CXT0764W (29-2)	PCT patent appln	01/01093 7/30/01		Pending	Riley	Frequency Synthesizer	PCT patent app; Pending
00CXT0765W (30-1)	US patent appln	09/545,88 7 4/7/00		Pending	Berlault	ESD Protection in Mixed Signal ICS	Parent US patent app; CPA filed 2/26/02; Pending
01CXT0166W (31-1)	US patent appln	10/008,44 2 6-Dec-2001		Pending	Balteanu; Gheorghe	Low Power Bandgap Circuit	Parent US patent app; Pending
00CXT0800W (32-1)	US patent appln			Unfiled	Cojocaru	Low-Voltage Bipolar Current Mode Logic (CML) Family Using Schottky Diodes	Parent US patent app; Assigned /Unfiled

IP SCHEDULE B

IP SCHEDULE B

Philsar Trademarks

Trademark Name	Country Name	Trademark Status	Class	Register Date	Next Renewal Date
RADIODAC	Japan	Registered	WCD	09-Jul-1999	09-Jul-2009
PHILSAR	United States of America	Registered	WCD	28-Aug-2001	28-Aug-2011
PHILSAR	Canada	Registered	WCD	18-Dec-2000	18-Dec-2015
PHILSAR	Japan	Registered	WCD	10-Dec-1999	10-Dec-2009