


Form PTO-1595 (Rev. 03/01) OMB No. 0651-0027 (exp. 5/31/2002)		RECORDATION FORM COVER SHEET PATENTS ONLY		U.S. DEPARTMENT OF COMMERCE U.S. Patent and Trademark Office	
To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof					
1. Name of conveying party(ies): Emulex Corporation Additional name(s) of conveying party(ies) attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No		2. Name and address of receiving party(ies) Name: Emulex Design & Manufacturing Corporation Internal Address: _____ Street Address: 3333 Susan Street City: Costa Mesa State: CA Zip: 92626 Additional name(s) & address(es) attached: <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No			
3. Nature of Conveyance: <input checked="" type="checkbox"/> Assignment <input type="checkbox"/> Merger <input type="checkbox"/> Security Agreement <input type="checkbox"/> Change of Name <input type="checkbox"/> Other _____ Execution Date: March 15, 2004					
4. Application number(s) or patent number(s): If this document is being filed together with a new application, the execution date of the new application is: _____ A. Patent Application No.(s): _____ B. Patent No.(s): 6,459,701 Additional numbers attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No					
5. Name and address of party to whom correspondence concerning document should be mailed: Name: Glenn M. Kubota Morrison & Foerster LLP Internal Address: Atty. Dkt.: 491442008400 Street Address: 555 West Fifth Street Suite 3500 City: Los Angeles State: CA Zip: 90013-1024		6. Total number of applications and patents involved: 1 7. Total fee (37 CFR 3.41) \$ 40.00 <input type="checkbox"/> Enclosed <input checked="" type="checkbox"/> Authorized to be charged to deposit account <input type="checkbox"/> Authorized to be charged to credit card (Form 2036 enclosed) 8. Deposit account number: 03-1952			
DO NOT USE THIS SPACE					
9. Statement and signature. <i>To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.</i> Glenn M. Kubota  03/31/2004 Name of Person Signing Signature Date Total number of pages including cover sheet, attachments, and documents: 10					

CH \$40.00 031952 6459701

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ASSIGNMENT

WHEREAS, Emulex Corporation, a California corporation, with offices at 3333 Susan Street, Costa Mesa, California 92626 ("ASSIGNOR"), owns certain U.S. and foreign patents and/or registrations, as listed in Exhibit A attached hereto and incorporated herein by this reference ("PATENTS"); and

WHEREAS, Emulex Design & Manufacturing Corporation, a Delaware corporation (p/k/a Vixel Corporation), with offices at 3333 Susan Street, Costa Mesa, California 92626 ("ASSIGNEE"), desires to acquire all of the right, title and interest of ASSIGNOR in, to and under the PATENTS;

WHEREAS, ASSIGNOR and ASSIGNEE have entered into a certain Contribution and Assignment Agreement dated February 22, 2004, assigning, among other things, all right, title and interest in and to the PATENTS from ASSIGNOR to ASSIGNEE;

NOW, THEREFORE, ASSIGNOR does hereby sell, assign, transfer and convey unto ASSIGNEE its entire right, title and interest in and to the PATENTS, including all foreign rights, divisions, continuations, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the PATENTS (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the PATENTS.

ASSIGNOR: Emulex Corporation

By: 

Name: Paul Folino

Title: Chairman & Chief Executive Officer

Date: March 15, 2004

ASSIGNEE: Emulex Design & Manufacturing Corporation

By: 

Name: Michael J. Rothenbach

Title: Executive Vice President & Chief Financial Officer

Date: March 15, 2004

PATENT
REEL: 014475 FRAME: 0349

STATE OF CALIFORNIA)
) ss.
COUNTY OF ORANGE)

On MARCH 15, 2004, before me, the undersigned notary public in and for said County and State, personally appeared MICHAEL J. ROCKENBACH

X personally known to me *or*
 proved to me on the basis of satisfactory evidence

to be the person(s) whose name(s) IS subscribed to the within instrument and acknowledged to me that HE executed the same in HIS authorized capacity(ies) and that, by HIS signature(s) on the instrument, the person(s) or the entity(ies) upon behalf of which the person(s) acted executed the instrument.

WITNESS my hand and official seal.

Kathryn Cole

My commission expires on
JUNE 1, 2007



EXHIBIT A**Schedule of Issued Patents to be Transferred From
Emulex Corporation (California) to Emulex Design & Manufacturing Corporation (Delaware)**

Title	Country/Region	Filing Date	Application #	Patent #
Linked Caches Memory For Storing Units Of Information	United States	4/15/1997	08/843,315	5,745,727
Linked Caches Memory For Storing Units Of Information	Canada	5/24/1996	2221797	2,221,797
Linked Caches Memory For Storing Units Of Information	Japan	5/24/1996	08-535893	3288712
Linked Caches Memory For Storing Units Of Information	South Korea	5/24/1996	97-708485	299358
Linked Caches Memory For Storing Units Of Information	WIPO	5/24/1996	PCT/US96/07636	
Apparatus for Reordering Data Frames Within An Interface Device	United States	3/27/1995	08/410,712	5,588,000
Window Comparator	South Korea	3/22/1996	97-706877	0364385
Window Comparator	WIPO	3/22/1996	PCT/US96/03970	
Computer Control Device For Managing A Timer Array	United States	4/27/1995	08/429,916	5,659,720
Timer Manager	Canada	4/26/1996	2219296	2,219,296
Timer Manager	Japan	4/26/1996	08-532768	3083565
Timer Manager	South Korea	4/26/1996	97-707617	0284718
Timer Manager	WIPO	4/26/1996	PCT/US96/05880	
Memory Buffer System Using A Single Pointer To Reference Multiple Associated Data	United States	6/7/1995	08/484,592	5,860,149
Efficient Transmission Buffer Management System	United States	1/12/1999	09/229,464	6,041,397
Split Buffer Architecture	South Korea	6/6/1996	97-708890	288453
Split Buffer Architecture	WIPO	6/6/1996	PCT/US96/09934	
Burst Broadcasting On A Peripheral Component Interconnect Bus	United States	6/7/1995	08/488,035	5,634,138
Burst-Broadcasting On A Peripheral Component Interconnect Bus	Canada	6/7/1996	2223930	2,223,930
Burst-Broadcasting On A Peripheral Component Interconnect Bus	European Patent Convention Regionally filed: France, Germany, UK	6/7/1996	96923249.5	0870239 B1

Title	Country/Region	Filing Date	Application #	Patent #
Burst-Broadcasting On A Peripheral Component Interconnect Bus	South Korea	6/7/1996	97-708804	0295968
Burst-Broadcasting On A Peripheral Component Interconnect Bus	WIPO	6/7/1996	PCT/US96/09777	
Cylinder Defect Management System For Data Storage System	United States	12/16/1988	07/285,808	4,935,825
Connector Mounting Device For Extending I/O Connections To A Personal Computer	United States	4/15/1983	29/485,450	D282,160 (Expired)
Elastic Bus Interface Data Buffer	United States	3/10/1997	08/813,271	5,838,936
Elastic Bus Interface Data Buffer	Canada	3/10/1998	2283229	2,283,229
Elastic Bus Interface Data Buffer	South Korea	3/10/1998	1999-7008174	0337059
Elastic Bus Interface Data Buffer	WIPO	3/10/1998	PCT/US98/04823	
Full-Duplex Communication Processor Which Can Be Used For Fibre Channel Frames	United States	9/24/1997	08/937,066	6,005,849
Full-Duplex Communication Processor	Canada	9/24/1998	2304340	2,304,340
Full-Duplex Communication Processor	South Korea	9/24/1998	10-2000-7003187	0315245
Full-Duplex Communication Processor	WIPO	9/24/1998	PCT/US98/20003	
Communication Processor Having Buffer List Modifier Control Bits	United States	9/24/1997	08/937,065	6,304,910 B1
Communication Processor Having Buffer List Modifier Control Bits	Japan	9/24/1998	2000-513358	3457947
Communication Processor Having Buffer List Modifier Control Bits	South Korea	9/24/1998	10-2000-7003185	0367949
Communication Processor Having Buffer List Modifier Control Bits	WIPO	9/24/1998	PCT/US98/20011	
Buffering Data That Flows Between Buses Operating At Different Frequencies	United States	10/27/1997	08/957,856	6,047,339
Buffering Data That Flows Between Buses Operating At Different Frequencies	Canada	10/27/1998	2307816	2,307,816
Buffering Data That Flows Between Buses Operating At Different Frequencies	South Korea	10/27/1998	10-2000-7004461	0337056
Buffering Data That Flows Between Buses Operating At Different Frequencies	WIPO	10/27/1998	PCT/US98/22807	
Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields	United States	5/1/1998	09/071,276	6,098,125
Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields	Canada	4/26/1999	2,330,014	2,330,014

Title	Country/Region	Filing Date	Application #	Patent #
Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields	South Korea	4/26/1999	10-2000-7012132	0345539
Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields	WIPO	4/26/1999	PCT/US99/08987	
Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames	United States	3/26/1998	09/048,930	6,314,100 B1
Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames	Canada	3/24/1999	2325857	2,325,857
Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames	South Korea	3/24/1999	10-2000-7010661	0394546
Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames	WIPO	3/24/1999	PCT/US99/06490	
Loop Network Hub Using Loop Initialization Insertion ¹	United States	5/1/1998	09/072,275	6,560,205 B1
Loop Network Hub Using Loop Initialization Insertion	South Korea	4/26/1999	10-2000-7012134	0364446
Loop Network Hub Using Loop Initialization Insertion	WIPO	4/26/1999	PCT/US99/08986	
Programmable Error Control Circuit	United States	5/1/1998	09/071,431	6,167,026
Programmable Error Control Circuit	Canada	4/27/1999	2327766	2,327,766
Programmable Error Control Circuit	South Korea	4/27/1999	10-2000-7012133	0394310
Programmable Error Control Circuit	WIPO	4/27/1999	PCT/US99/09120	
Automatic Isolation In Loops	United States	5/1/1998	09/071,678	6,188,668 B1
Automatic Isolation In Loops	United States	9/15/1999	09/398,523	6,289,002 B1
Automatic Isolation In Loops	South Korea	4/27/1999	10-2000-7012159	0391480
Automatic Isolation In Loops	WIPO	4/27/1999	PCT/US99/09123	
Scalable Hub	United States	5/1/1998	09/071,508	6,282,188 B1
Scalable Hub	South Korea	4/28/1999	10-2000-7012154	0391484
Scalable Hub	WIPO	4/28/1999	PCT/US99/09426	
Hub Port With Constant Phase	United States	5/1/1998	09/071,932	6,157,652
Hub Port With Constant Phase	South Korea	4/28/1999	10-2000-7012120	0393927
Hub Port With Constant Phase	WIPO	4/28/1999	PCT/US99/09428	

¹ Assignment to Emulex Corporation was recorded with incorrect serial number; investigating how to correct

Title	Country/Region	Filing Date	Application #	Patent #
Hub Port Without Jitter Transfer	United States	5/1/1998	09/071,632	6,064,679
Hub Port Without Jitter Transfer	South Korca	4/30/1999	10-2000-7012151	0388339
Hub Port Without Jitter Transfer	WIPO	4/30/1999	PCT/US99/09423	
Automatic Loop Segment Failure Isolation	United States	5/1/1998	09/071,288	6,101,166
Automatic Loop Segment Failure Isolation	United States	9/15/1999	09/398,520	6,201,787 B1
Automatic Loop Segment Failure Isolation	Canada	4/29/1999	2330770	2,330,770
Automatic Loop Segment Failure Isolation	South Korea	4/29/1999	10-2000-7012155	0394312
Automatic Loop Segment Failure Isolation	WIPO	4/29/1999	PCT/US99/09478	
Elimination Of Invalid Data In Loop Network	United States	5/1/1998	09/071,930	6,226,269 B1
Elimination Of Invalid Data In Loop Network	South Korea	4/30/1999	10-2000-7012150	0389782
Elimination Of Invalid Data In Loop Network	WIPO	4/30/1999	PCT/US99/09351	
Node Insertion And Removal In A Loop Network	United States	10/22/1998	09/177,550	6,215,775 B1
Node Insertion And Removal In A Loop Network	South Korea	10/21/1999	10-2001-700505	0403984
Node Insertion And Rcmoval In A Loop Network	WIPO	10/21/1999	PCT/US99/24893	
Sanitizing Fibre Channel Frames	United States	1/20/1999	09/234,231	6,226,299 B1
Sanitizing Fibre Channel Frames	United States	1/30/2001	09/774,428	6,600,753 B1
Sanitizing Fibre Channel Frames	WIPO	1/19/2000	PCT/US00/01286	
Automatic Detection Of 8B/10B Data Rates	United States	12/2/1998	09/204,669	6,158,014
Automatic Detection Of 8B/10B Data Rates	Canada	12/2/1999	2353435	2,353,435
Automatic Detection Of 8B/10B Data Rates	WIPO	12/2/1999	PCT/US99/28805	
Variable Access Fairness In A Fibre Channel Arbitrated Loop	United States	8/6/1999	09/370,096	6,459,701 B1
Variable Access Fairness In A Fibre Channel Arbitrated Loop	WIPO	8/2/2000	PCT/US00/40554	
Detecting And Counting Node Port Loop Initialization Origination	United States	8/16/2000	09/640,564	6,687,219

Title	Country/Region	Filing Date	Application #	Patent #
Detecting And Counting Node Port Loop Initialization Origination	WIPO	8/16/2001	PCT/US01/25667	
Detecting And Counting Open Ordered Sets Originating From An Attached Node Port	United States	10/12/2000	09/687,259	6,483,843 B1
Fiber Channel Star Hub	WIPO	10/9/2001	PCT/US01/31749	
Old-Port Node Detection And Hub Port Bypass	United States	12/4/2000	09/730,149	6,496,514 B2
Old-Port Node Detection And Hub Port Bypass	WIPO	11/30/2001	PCT/US01/45114	
Hardware Initialization With Or Without Processor Intervention	WIPO	2/6/2002	PCT/US02/03759	
Method For Determining Valid Bytes For Multiple-Byte Burst Memories	WIPO	10/9/2001	PCT/US0131750	
Data Formatter Employing Data Shifter Based On The Destination Address	WIPO	7/30/2002	PCT/US02/24139	
Phase-Locked Loop (PLL) Circuit For Selectively Correcting Clock Skew In Different Modes	United States	6/3/2002	10/161,922	6,647,081 B2
Computer Network Interface For Direct Mapping Of Data Transferred Between Applications On Different Host Computers From Virtual Addresses To Physical Memory Addresses Application Data	United States	12/4/1996	08/762,186	6,094,712
Computer Interface From Direct Mapping Of Application Data	WIPO	12/3/1997	PCT/US97/22439	
Computer Interface From Direct Mapping Of Application Data	Australia	12/3/1997	53767/98	726992
System And Method For Transferring Information Representative Of Conditions At A Receiving Device For A Virtual Circuit In A Computer Network	United States	4/27/1998	09/067,533	5,991,818
System For Transferring Information Between Devices Over Virtual Circuit Established Therebetween Using Computer Network	WIPO	4/27/1999	PCT/US99/09114	
System And Method For Regulating Message Flow In A Digital Data Network	United States	4/23/1998	09/065,118	6,570,850 B1
System And Method For Regulating Message Flow In A Digital Data Network	WIPO	4/23/1999	PCT/US99/09046	
System And Method For Scheduling Message Transmission And Processing In A Digital Data Network	Australia	4/23/1999	37621/99	752188

Title	Country/Region	Filing Date	Application #	Patent #
System And Method For Scheduling Message Transmission And Processing In A Digital Data Network	WIPO	4/23/1999	PCT/US99/09021	
Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network	Australia	5/1/1999	59481/99	764270
Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network	WIPO	5/1/1999	PCT/US99/09668	