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To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof

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| <p>1. Name of conveying party(ies): Emulex Corporation</p> <p>Additional name(s) of conveying party(ies) attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No</p> <p>3. Nature of Conveyance: <input checked="" type="checkbox"/> Assignment <input type="checkbox"/> Merger <input type="checkbox"/> Security Agreement <input type="checkbox"/> Change of Name <input type="checkbox"/> Other _____</p> <p>Execution Date: <u>March 15, 2004</u></p> | <p>2. Name and address of receiving party(ies) Emulex Design & Manufacturing</p> <p>Name: <u>Corporation</u></p> <p>Internal Address: _____</p> <p>Street Address: <u>3333 Susan Street</u></p> <p>City: <u>Costa Mesa</u></p> <p>State: <u>CA</u> Zip: <u>92626</u></p> <p>Additional name(s) & address(es) attached: <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No</p> |
|--|--|

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the new application is: _____

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| <p>A. Patent Application No.(s): <u>10/407,031</u></p> | <p>B. Patent No.(s): _____</p> |
|--|--------------------------------|


Additional numbers attached? Yes No

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| <p>5. Name and address of party to whom correspondence concerning document should be mailed:</p> <p>Name: <u>Glenn M. Kubota</u> <u>Morrison & Foerster LLP</u></p> <p>Internal Address: <u>Atty. Dkt.: 491442011300</u></p> <p>Street Address: <u>555 West Fifth Street</u> <u>Suite 3500</u></p> <p>City: <u>Los Angeles</u> State: <u>CA</u> Zip: <u>90013-1024</u></p> | <p>6. Total number of applications and patents involved: <u>1</u></p> <p>7. Total fee (37 CFR 3.41) \$ <u>40.00</u></p> <p><input type="checkbox"/> Enclosed <input checked="" type="checkbox"/> Authorized to be charged to deposit account <input type="checkbox"/> Authorized to be charged to credit card (Form 2038 enclosed)</p> <p>8. Deposit account number: <u>03-1952</u></p> |
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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

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|---|--|---------------------------|
| <u>Glenn M. Kubota (44,197)</u> Name of Person Signing |  Signature | <u>04/02/2004</u> Date |
|---|--|---------------------------|

Total number of pages including cover sheet, attachments, and documents: 10/12

CH \$40.00 03-1952 10407031

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ASSIGNMENT

WHEREAS, Emulex Corporation, a California corporation, with offices at 3333 Susan Street, Costa Mesa, California 92626 ("ASSIGNOR"), owns certain U.S. and foreign patent applications, as listed in Exhibit A attached hereto and incorporated herein by this reference ("PATENTS"); and

WHEREAS, Emulex Design & Manufacturing Corporation, a Delaware corporation (p/k/a Vixel Corporation), with offices at 3333 Susan Street in Costa Mesa, California 92626 ("ASSIGNEE"), desires to acquire all of the right, title and interest of ASSIGNOR in, to and under the PATENTS;

WHEREAS, ASSIGNOR and ASSIGNEE have entered into a certain Contribution and Assignment Agreement dated February 22, 2004, assigning, among other things, all right, title and interest in and to the PATENTS from ASSIGNOR to ASSIGNEE;

NOW, THEREFORE, ASSIGNOR does hereby sell, assign, transfer and convey unto ASSIGNEE its entire right, title and interest in and to the PATENTS, including all foreign rights, divisions, continuations, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the PATENTS (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the PATENTS.

ASSIGNOR: Emulex Corporation

By: Paul Folino

Name: Paul Folino

Title: Chairman & Chief Executive Officer

Date: March 15, 2004

ASSIGNEE: Emulex Design & Manufacturing Corporation

By: Michael J. Rockenbach

Name: Michael J. Rockenbach

Title: Executive Vice President & Chief Financial Officer

Date: March 15, 2004

STATE OF CALIFORNIA)
) ss.
COUNTY OF ORANGE)

On MARCH 15, 2004, before me, the undersigned notary public in and for said County and State, personally appeared PAUL F. FOLINO

X personally known to me or
proved to me on the basis of satisfactory evidence

to be the person(s) whose name(s) IS subscribed to the within instrument and acknowledged to me that HE executed the same in HIS authorized capacity(ies) and that, by HIS signature(s) on the instrument, the person(s) or the entity(ies) upon behalf of which the person(s) acted executed the instrument.

WITNESS my hand and official seal.

Kathryn Cole

My commission expires on
JUNE 1, 2007



STATE OF CALIFORNIA)
) ss.
COUNTY OF ORANGE)

On MARCH 15, 2004, before me, the undersigned notary public in and for said County and State, personally appeared MICHAEL J. RICKENBACH,

X personally known to me or
proved to me on the basis of satisfactory evidence

to be the person(s) whose name(s) IS subscribed to the within instrument and acknowledged to me that HE executed the same in HIS authorized capacity(ies) and that, by HIS signature(s) on the instrument, the person(s) or the entity(ies) upon behalf of which the person(s) acted executed the instrument.

WITNESS my hand and official seal.

Kathryn Cole

My commission expires on

JUNE 1, 2007



EXHIBIT A

**Schedule of Pending Patent Applications to be Transferred From
Emulex Corporation (California) to Emulex Design & Manufacturing Corporation (Delaware)**

| Title | Country/Region | Filing Date | Application # | Patent # |
|---|----------------|-------------|----------------|----------|
| Flow-Through Register | United States | 1/8/2003 | 10/338,629 | |
| Flow-Through Register | PCT | 12/5/2003 | PCT/US03/38841 | |
| Flow-Through Register | Taiwan | 12/17/2003 | 92135832 | |
| Hot Swap Compact PCI Power Supply | United States | 5/9/2003 | 10/434,626 | |
| Dynamically Self-Adjusting Polling Mechanism | United States | 5/19/2003 | 10/440,681 | |
| Method and Apparatus for Local and Distributed Data Memory Access ("DMA") Control | United States | 6/2/2003 | 10/452,330 | |
| Local Emulation Of Data RAM Utilizing Write-Through Cache Hardware Within A CPU Module | United States | 3/28/2003 | 10/401,459 | |
| Hardware Assisted Firmware Task Scheduling And Management | United States | 3/28/2003 | 10/402,182 | |
| Memory Data Interface | United States | 5/19/2003 | 10/440,855 | |
| Direct Memory Access From Host Without Processor Intervention | United States | 8/29/2003 | 10/651,887 | |
| Multi-Channel Memory Access Arbitration Method And System | United States | 8/29/2003 | 10/651,890 | |
| Integrated Network Interface Supporting Multiple Data Transfer Protocols | United States | 9/3/2003 | 10/653,767 | |
| Read/Write Command Buffer Pool Resource Management Using Read-Path Prediction Of Future Resources | United States | 6/27/2003 | 10/609,291 | |
| Sparse And Non-Sparse Data Management Method And System | United States | 6/27/2003 | 10/609,289 | |
| Queue Register Configuration Structure | United States | 9/22/2003 | 10/668,138 | |
| System For Communication With A Storage Area Network | United States | 1/24/2002 | 10/057,626 | |
| Re-Programmable Finite State Machine | United States | 9/16/2002 | 10/245,436 | |
| Method And Apparatus For Improving Noise Immunity In A DDR SDRAM System | United States | 9/16/2002 | 10/245,437 | |
| Structure And Method For Maintaining Ordered Linked Lists | United States | 10/10/2002 | 10/268,178 | |
| Structure And Method For Managing Available Memory Resources | United States | 2/26/2003 | 10/376,354 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|---|----------------------------|----------------------|-----------------------------|----------|
| Structure And Method For Managing Available Memory Resources | PCT | 2/6/2004 | PCT/US03/40967 | |
| Structure And Method For Managing Available Memory Resources | Taiwan | awaiting filing date | awaiting application number | |
| Window Comparator | Canada | 3/22/1996 | 2216642 | |
| Window Comparator | European Patent Convention | 3/22/1996 | 96911379.4 | |
| Window Comparator | Japan | 3/22/1996 | 8-529544 | |
| Timer Manager | European Patent Convention | 4/26/1996 | 96914558.0 | |
| Split Buffer Architecture | Canada | 6/6/1996 | 2223890 | |
| Split Buffer Architecture | European Patent Convention | 6/6/1996 | 96919329.1 | |
| Split Buffer Architecture | Japan | 6/6/1996 | 09-502095 | |
| Elastic Bus Interface Data Buffer | European Patent Convention | 3/10/1998 | 98909136.8 | |
| Elastic Bus Interface Data Buffer | Japan | 3/10/1998 | 10-539786 | |
| Full-Duplex Communication Processor | European Patent Convention | 9/24/1998 | 98951937.6 | |
| Communication Processor Having Buffer List Modifier Control Bits | Canada | 9/24/1998 | 2304620 | |
| Communication Processor Having Buffer List Modifier Control Bits | European Patent Convention | 9/24/1998 | 98949477.8 | |
| Buffering Data That Flows Between Buses Operating At Different Frequencies | European Patent Convention | 10/27/1998 | 98957392.8 | |
| Buffering Data That Flows Between Buses Operating At Different Frequencies | Japan | 10/27/1998 | 2000-518329 | |
| Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields | European Patent Convention | 4/26/1999 | 99921470.3 | |
| Method Of Mapping Fibre Channel Frames Based On Control And Type Header Fields | Japan | 4/26/1999 | 2000-547550 | |
| Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames | European Patent Convention | 3/24/1999 | 99914129.4 | |
| Method Of Validation And Host Buffer Allocation For Unmapped Fibre Channel Frames | Japan | 3/24/1999 | 2000-538472 | |
| Loop Network Hub Using Loop Initialization Insertion | United States | 5/6/2003 | 10,431,647 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|--|----------------------------|-------------|----------------|----------|
| Loop Network Hub Using Loop Initialization Insertion | Canada | 4/26/1999 | 2329950 | |
| Loop Network Hub Using Loop Initialization Insertion | European Patent Convention | 4/26/1999 | 99922729.1 | |
| Loop Network Hub Using Loop Initialization Insertion | Japan | 4/26/1999 | 2000-547712 | |
| Loop Network Hub Using Loop Initialization Insertion | WIPO | 4/26/1999 | PCT/US99/08986 | |
| Programmable Error Control Circuit | European Patent Convention | 4/27/1999 | 99920073.6 | |
| Programmable Error Control Circuit | Japan | 4/27/1999 | 2000-547715 | |
| Automatic Isolation In Loops | United States | 5/4/2001 | 09/849,102 | |
| Automatic Isolation In Loops | Canada | 4/27/1999 | 2330768 | |
| Automatic Isolation In Loops | European Patent Convention | 4/27/1999 | 99920075.1 | |
| Automatic Isolation In Loops | Japan | 4/27/1999 | 2000-547718 | |
| Scalable Hub | Canada | 4/28/1999 | 2330766 | |
| Scalable Hub | European Patent Convention | 4/28/1999 | 99918918.6 | |
| Scalable Hub | Japan | 4/28/1999 | 2000-547739 | |
| Hub Port With Constant Phase | Canada | 4/28/1999 | 2330743 | |
| Hub Port With Constant Phase | European Patent Convention | 4/28/1999 | 99918920.2 | |
| Hub Port With Constant Phase | Japan | 4/28/1999 | 2000-547736 | |
| Hub Port Without Jitter Transfer | Canada | 4/30/1999 | 2330012 | |
| Hub Port Without Jitter Transfer | European Patent Convention | 4/30/1999 | 99920190.8 | |
| Hub Port Without Jitter Transfer | Japan | 4/30/1999 | 2000-547713 | |
| Automatic Loop Segment Failure Isolation | European Patent Convention | 4/29/1999 | 99921567.6 | |
| Automatic Loop Segment Failure Isolation | Japan | 4/29/1999 | 2000-547716 | |
| Elimination Of Invalid Data In Loop Network | Canada | 4/30/1999 | 2330742 | |
| Elimination Of Invalid Data In Loop Network | European Patent Convention | 4/30/1999 | 99920157.7 | |
| Elimination Of Invalid Data In Loop Network | Japan | 4/30/1999 | 2000-547738 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|--|----------------------------|-------------|-----------------|----------|
| Node Insertion And Removal In A Loop Network | Canada | 10/21/1999 | 2349584 | |
| Node Insertion And Removal In A Loop Network | European Patent Convention | 10/21/1999 | 99970812.6 | |
| Node Insertion And Removal In A Loop Network | Japan | 10/21/1999 | 2000-577803 | |
| Sanitizing Fibre Channel Frames | United States | 2/28/2003 | 10/376,659 | |
| Sanitizing Fibre Channel Frames | Canada | 1/19/2000 | 2361453 | |
| Sanitizing Fibre Channel Frames | European Patent Convention | 1/19/2000 | 00970425.5 | |
| Sanitizing Fibre Channel Frames | Japan | 1/19/2000 | 2001-505261 | |
| Sanitizing Fibre Channel Frames | South Korea | 1/19/2000 | 10-2001-7009142 | |
| Automatic Detection Of 8B/10B Data Rates | European Patent Convention | 12/2/1999 | 99965126.8 | |
| Automatic Detection Of 8B/10B Data Rates | Japan | 12/2/1999 | 2000-585740 | |
| Automatic Detection Of 8B/10B Data Rates | South Korea | 12/2/1999 | 10-2001-7006951 | |
| Variable Access Fairness In A Fibre Channel Arbitrated Loop | Canada | 8/2/2000 | 2380420 | |
| Variable Access Fairness In A Fibre Channel Arbitrated Loop | European Patent Convention | 8/3/2000 | 00963784.4 | |
| Variable Access Fairness In A Fibre Channel Arbitrated Loop | Japan | 8/4/2000 | 2001-515567 | |
| Variable Access Fairness In A Fibre Channel Arbitrated Loop | South Korea | 8/5/2000 | 10-2002-7001404 | |
| Detecting And Counting Node Port Loop Initialization Origination | Canada | 8/16/2001 | 2419542 | |
| Detecting And Counting Node Port Loop Initialization Origination | European Patent Convention | 8/16/2001 | 01964087.9 | |
| Detecting And Counting Node Port Loop Initialization Origination | Japan | 8/16/2001 | 2002-520485 | |
| Detecting And Counting Node Port Loop Initialization Origination | South Korea | 8/16/2001 | 10-2003-7002048 | |
| Fiber Channel Star Hub | Canada | 10/9/2001 | 2425657 | |
| Fiber Channel Star Hub | European Patent Convention | 10/9/2001 | 01977709.3 | |
| Fiber Channel Star Hub | Japan | 10/9/2001 | 2002-535334 | |
| Fiber Channel Star Hub | South Korea | 10/9/2001 | 10-2003-7004898 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|--|----------------------------|-------------|-----------------------------|----------|
| Old-Port Node Detection And Hub Port Bypass | Canada | 11/30/2001 | 2436865 | |
| Old-Port Node Detection And Hub Port Bypass | European Patent Convention | 11/30/2001 | 01989810.5 | |
| Old-Port Node Detection And Hub Port Bypass | Japan | 11/30/2001 | 2002-548935 | |
| Old-Port Node Detection And Hub Port Bypass | Korea | 11/30/2001 | 10-2003-7007369 | |
| Hardware Initialization With Or Without Processor Intervention | United States | 2/7/2001 | 09/779,195 | |
| Hardware Initialization With Or Without Processor Intervention | Canada | 2/6/2002 | 2435665 | |
| Hardware Initialization With Or Without Processor Intervention | European Patent Convention | 2/6/2002 | 02704401.5 | |
| Hardware Initialization With Or Without Processor Intervention | Japan | 2/6/2002 | 2002-563123 | |
| Hardware Initialization With Or Without Processor Intervention | Korea | 2/6/2002 | 10-2003-7010415 | |
| Method For Determining Valid Bytes For Multiple-Byte Burst Memories | United States | 10/12/2000 | 09/687,526 | |
| Method For Determining Valid Bytes For Multiple-Byte Burst Memories | Canada | 10/9/2001 | 2425660 | |
| Method For Determining Valid Bytes For Multiple-Byte Burst Memories | European Patent Convention | 10/9/2001 | 01977710.1 | |
| Method For Determining Valid Bytes For Multiple-Byte Burst Memories | Japan | 10/9/2001 | 2002-534980 | |
| Method For Determining Valid Bytes For Multiple-Byte Burst Memories | Korea | 10/9/2001 | 10-2003-7005033 | |
| Data Formatter For Shifting Data To Correct Data Lanes | United States | 11/30/2001 | 10/000,848 | |
| Data Formatter Employing Data Shifter Based On The Destination Address | Canada | 7/30/2002 | awaiting application number | |
| Data Formatter Employing Data Shifter Based On The Destination Address | European Patent Convention | 7/30/2002 | awaiting application number | |
| Data Formatter Employing Data Shifter Based On The Destination Address | Japan | 7/30/2002 | awaiting application number | |
| Data Formatter Employing Data Shifter Based On The Destination Address | Korea | 7/30/2002 | 10-2004-7001454 | |
| Direct Memory Access (DMA) Transfer Buffer Processor | United States | 6/24/2002 | 10/179,816 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|--|----------------------------|-------------|----------------|----------|
| Direct Memory Access (DMA) Transfer Buffer Processor | WIPO | 12/10/2002 | PCT/US02/39551 | |
| Tracking Deferred Data Transfers On A System-Interconnect Bus | United States | 4/17/2002 | 10/125,101 | |
| Tracking Deferred Data Transfers On A System-Interconnect Bus | WIPO | 12/10/2002 | PCT/US02/39549 | |
| Receiving Data From Interleaved Multiple Concurrent Transactions In A FIFO Memory | United States | 4/10/2002 | 10/120,733 | |
| Receiving Data From Interleaved Multiple Concurrent Transactions In A FIFO Memory | WIPO | 5/9/2002 | PCT/US02/14815 | |
| Supercharge Message Exchanger | United States | 12/10/2002 | 10/316,604 | |
| Supercharge Message Exchange | WIPO | 12/11/2002 | PCT/US02/39788 | |
| Phase-Locked Loop (PLL) Circuit For Selectively Correcting Clock Skew In Different Modes | United States | 3/3/2003 | 10/379,776 | |
| Phase-Locked Loop (PLL) Circuit For Selectively Correcting Clock Skew In Different Modes | WIPO | 12/12/2002 | PCT/US02/40131 | |
| Computer Interface From Direct Mapping Of Application Data | Canada | 12/3/1997 | 2274031 | |
| Computer Interface From Direct Mapping Of Application Data | European Patent Convention | 12/3/1997 | 97950879.3 | |
| Computer Interface From Direct Mapping Of Application Data | Japan | 12/3/1997 | H10-525871 | |
| System For Transferring Information Between Devices Over Virtual Circuit Established Therebetween Using Computer Network | Australia | 4/27/1999 | 766026 | |
| System For Transferring Information Between Devices Over Virtual Circuit Established Therebetween Using Computer Network | Canada | 4/27/1999 | 2329366 | |
| System For Transferring Information Between Devices Over Virtual Circuit Established Therebetween Using Computer Network | Europe Patent Convention | 4/27/1999 | 99918855.0 | |
| System For Transferring Information Between Devices Over Virtual Circuit Established Therebetween Using Computer Network | Japan | 4/27/1999 | 2000-546308 | |
| System And Method For Regulating Message Flow In A Digital Data Network | United States | 3/11/2003 | 10/386,642 | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|---|----------------------------|-------------|-----------------------------|----------|
| System And Method For Regulating Message Flow In A Digital Data Network | Australia | 4/23/1999 | 38679/99 | |
| System And Method For Regulating Message Flow In A Digital Data Network | Canada | 4/23/1999 | 2329357 | |
| System And Method For Regulating Message Flow In A Digital Data Network | European Patent Convention | 4/23/1999 | 99921477.8 | |
| System And Method For Regulating Message Flow In A Digital Data Network | Japan | 4/23/1999 | 2000-545110 | |
| System And Method For Scheduling Message Transmission And Processing In A Digital Data Network | United States | 4/23/1998 | 09/065,115 | |
| System And Method For Scheduling Message Transmission And Processing In A Digital Data Network | Canada | 4/23/1999 | 2329542 | |
| System And Method For Scheduling Message Transmission And Processing In A Digital Data Network | Europe Patent Convention | 4/23/1999 | 99920035.5 | |
| System And Method For Scheduling Message Transmission And Processing In A Digital Data Network | Japan | 4/23/1999 | 2000-545109 | |
| Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network | Canada | 5/1/1999 | 2,329,367 | |
| Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network | European Patent Convention | 5/1/1999 | 99921625.2 | |
| Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network | Japan | 5/1/1999 | 2000-547737 | |
| Distributed Switch And Connection Control Arrangement And Method For Digital Communications Network | United States | 7/3/1999 | 09/347,709 | |
| System With Multiple Path Fail Over, Fail Back And Load Balancing | United States | 10/21/2002 | 10/278,189 | |
| System With Multiple Path Fail Over, Fail Back And Load Balancing | WIPO | 10/21/2003 | PCT/US03/33481 | |
| Abstracted Node Discovery | United States | 2/28/2003 | 10/377,496 | |
| Abstracted Node Discovery | WIPO | 10/8/2003 | PCT/US03/32407 | |
| Zero-Configuration Auto-Discovery For Network Storage | United States | 2/12/2003 | 10/365,963 | |
| Zero-Configuration Auto-Discovery For Network Storage | WIPO | 2/6/2004 | awaiting application number | |

| Title | Country/Region | Filing Date | Application # | Patent # |
|---|----------------|-------------|-----------------------------|----------|
| Zero-Configuration Auto-Discovery For Network Storage | Taiwan | 2/12/2004 | awaiting application number | |
| Direct Memory Access Controller System | United States | 12/19/2002 | 10/324,310 | |
| Direct Memory Access Controller System | WIPO | 12/11/2003 | PCT/US03/39583 | |
| Direct Memory Access Controller System | Taiwan | 12/19/2003 | 092136165 | |
| Direct Data Placement | United States | 3/24/2003 | 10/396,985 | |
| Network Configuration Synchronization for Hardware Accelerated Network Protocol | United States | 10/24/2002 | 10/280,503 | |
| Virtual Interface Over A Transport Protocol | United States | 8/28/2003 | 10/651,426 | |
| Method Of Queuing Fibre Channel Receive Frames | United States | 3/4/2003 | 10/382,728 | |
| Method Of Queuing Fibre Channel Receive Frames | WIPO | 10/16/2003 | PCT/US03/33035 | |
| Remote Management System | United States | 10/21/2002 | 10/277,922 | |
| Remote Management System | WIPO | 10/21/2003 | PCT/US03/33581 | |
| Message Logging | United States | 11/4/2002 | 10/288,616 | |
| Message Logging | WIPO | 11/4/2003 | PCT/US03/35121 | |
| Virtual Peripheral Component Interconnect Multi-Function Device | United States | 4/3/2003 | 10/407,031 | |
| Avoiding Port Collisions In Hardware-Accelerated Network Protocol | United States | 4/22/2003 | 10/421,495 | |
| Reverse Message Writes And Reads | United States | 4/23/2003 | 10/422,581 | |
| Memory Management | United States | 1/9/2003 | 10/340,078 | |
| Memory Management | WIPO | 12/19/2003 | PCT/US03/40967 | |
| Memory Management | Taiwan | 12/30/2003 | 092137494 | |