RECORDATION FORM COVER SHEET

U.S. Department of Commerce
Patent and Trademark Office

FORM PTO-1595
(Rev 10/02)
OMB No. 0651-0027 (exp.6/30/2005)

PATENTS ONLY

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

INFINEON TECHNOLOGIES AG

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

Name and address of receiving party(ies)

Name

RAMTRON INTERNATIONAL CORPORATION
1850 RAMTRON DRIVE
COLORADO SPRINGS, COLORADO 80921

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other **Amendment to Security Agreement & Release of Certain IP**

Execution Date: **March 30, 2004**

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)

B. Patent No.(s)

5,104,822	5,117,177	5,991,851	5,963,481
5,162,890	5,255,222	5,901,100	6,249,840
5,170,242	5,699,317	5,134,310	5,835,442
5,075,817	5,721,862	5,566,318	6,064,620
5,610,099	5,887,272	6,141,281	6,347,357
5,043,790	6,055,192	5,216,281	6,278,646
6,151,236	6,330,636	6,172,927	6,301,183
6,072,741			

Additional numbers attached? ☐ Yes ☒ No

5. Name and Address of party to whom correspondence concerning document should be mailed:

Name: Carol W. Burton
Internal Address: Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Street Address: same as above
City: Denver State: CO Zip: 80202

6. Total number of applications and patents involved: 29

7. Total fee (37 CFR 3.41) **$1,160.00**

☐ Enclosed
☒ Authorized to be charged to deposit account

8. Deposit account number: 50-1123
(Attach duplicate copy of this page if paying by deposit account)

CH $1160.00 501123 5104822

DO NOT USE THIS SPACE

9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Carol W. Burton, Reg. No. 35,465
Name of Person signing

Signature

April 5, 2004
Date

Total number of pages including cover sheet, attachments and document: 11

Mail documents to be recorded with required cover sheet information to: Mail Stop Assignment Recordation Services Director of the U.S. Patent & Trademark Offices P.O. Box 1450 Alexandria, VA 22313-1450

AMENDMENT TO SECURITY AGREEMENT AND RELEASE OF CERTAIN INTELLECTUAL PROPERTY

This Amendment and Release ("Amendment") to the Security Agreement dated as of March 28, 2002 (the "Security Agreement") by and between Infineon Technologies AG, a German stock corporation ("Infineon"), and Ramtron International Corporation, a Delaware corporation (the "Company") is dated as of March 30, 2004, and is being entered into by and between Infineon and the Company.

RECITALS

WHEREAS, Infineon and the Company entered into the Security Agreement in order to provide Infineon with a security interest in and to all of the Company's right, title and interest in and to the Collateral to secure the Company's repayment obligations under the Debenture purchased by Infineon pursuant to the Securities Purchase Agreement;

WHEREAS, pursuant to the Waiver Agreement dated August 18, 2003, by and between Infineon and the Company (the "Waiver Agreement"), the Company has agreed to make certain Waiver Payments (as defined in the Waiver Agreement) to decrease the Company's indebtedness under the Debenture;

WHEREAS, the Company wishes to sell the "Released IP" (as defined below) and within two business days after Company's receipt of proceeds from the sale of the Released IP, the Company will pay (by wire transfer or other agreed method) to Infineon the amount of One million ninety thousand Dollars ($1,090,000.00) or, if less, the full amount the Company receives as consideration for its sale of the Released IP (the "Payment"), which Payment shall, up to the amount of such Payment, (i) satisfy and be conclusively deemed to be in lieu of the Waiver Payments provided in Section 2 of the Waiver Agreement, and (ii) reduce the amount due under the Debenture Dollar for Dollar; the reminder, if any, of the Waiver Payments and the Debenture shall being due and payable in accordance with the agreed time schedules; and concurrently herewith, Infineon will release certain Collateral under the Security Agreement; and

WHEREAS, in consideration of the Payment to be made by the Company to Infineon, Infineon and the Company hereby wish to amend the Security Agreement and to execute a Release to delete from the Collateral certain intellectual property ("Released IP") listed on Schedule "1" as attached hereto.

NOW, THEREFORE, in consideration of the foregoing recitals, the following covenants and promises and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties hereto hereby agree as follows:

1. **Definitions**

Unless otherwise defined herein, all capitalized terms used herein and not otherwise defined herein shall have the respective meanings set forth in the Security Agreement, and references to "Section" or "Sections" herein are references to the specified sections of the Security Agreement.

2. **Amendment**

Section 1 – "Grant of Security". Section 1 of the Security Agreement is amended and restated to exclude the Released IP from the definition of Collateral.

3. **Release**

In consideration of and subject to the Payment to be made by the Company to Infineon under the Debenture and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Infineon has RELEASED and DISCHARGED, and by these presents does RELEASE and DISCHARGE, the Released IP from any and all security interests and liens held by Infineon and securing any indebtedness of the Company to Infineon and does hereby reassign and vest in the Company full title to the Released IP assigned to Infineon under the Security Agreement.

4. **Effect of Amendment**

Except as expressly modified by the provisions of this Amendment, the Security Agreement and all of the terms, provisions and conditions thereof shall for all purposes remain unchanged, and in full force and effect, and are approved, ratified and confirmed, and from and after the date hereof all references to the Agreement in any other agreement to which any of the undersigned are parties shall mean the Agreement as amended hereby. Without limiting the foregoing, Infineon and the Company agree that nothing herein affects in any way any license or other rights of Infineon in and to the Released IP, other than the security interest released in this Amendment.

5. **UCC3 Filing**

Infineon hereby authorizes the Company to file an amendment to UCC financing statement No. 2076971 5, filed on April 23, 2002, against the Company (the "Original Financing Statement"), with the Secretary of State of the State of Delaware, to delete the Released IP from the collateral listed on the Original Financing Statement.

6. **Counterparts**

This Amendment may be executed in any number of counterparts, each of which will be deemed an original, but all of which together will constitute one and the same instrument.

(Signature page follows)

IN WITNESS WHEREOF, the parties hereto have executed this Amendment effective as of the date set forth in the preamble hereof.

INFINEON TECHNOLOGIES AG

By i.V. Meyer
Name: Fleischmann
Title: VP Bus. Dev. Corp. Legal Counsel

RAMTRON INTERNATIONAL CORPORATION

By _____
Name:
Title:

IN WITNESS WHEREOF, the parties hereto have executed this Amendment effective as of the date set forth in the preamble hereof.

INFINEON TECHNOLOGIES AG

By _____
Name: Fleischmann
Title: VP Bus. Dev.

Meijer
Corp. Legal Counsel

RAMTRON INTERNATIONAL CORPORATION

By _____
Name: LuAnn D. Hanson
Title: Chief Financial Officer and VP of Finance

Schedule "1"

RELEASDED IP

Patent or Application No.	Country	Filing Date	Title Inventor(s)
Pat. 5,104,822 (RAM 317)	U.S.	07/30/1990	Method For Creating Self-Aligned, Non-Patterned Contact Areas And Stacked Capacitors Using The Method Butler
Pat. 5,162,890 (RAM 317 DIV)	U.S.	04/05/1991	Stacked Capacitor With Sidewall Insulation Butler
Pat. 2673615 (RAM 317 JPN)	Japan	07/30/1991	Method For Creating Self-Aligned, Non-Patterned Contact Areas And Stacked Capacitors Using The Method Butler
Pat. 5,170,242 (RAM 319 CON)	U.S.	05/10/1991	Reaction Barrier For A Multilayer Structure In An Integrated Circuit Stevens, Maekawa
Pat. 2075540 (RAM 319 JPN)	Japan	07/13/1990	Reaction Barrier For A Multilayer Structure In An Integrated Circuit Stevens, Maekawa
Pat. 5,075,817 (RAM 320)	U.S.	6/22/1990	Trench Capacitor For Large Scale Integrated Memory Butler
Pat. 2089169 (RAM 320 JPN)	Japan	08/21/1991	Trench Capacitor For Large Scale Integrated Memory Butler
Pat. 5,610,099 (RAM 321)	U.S.	06/28/1994	Process For Fabricating Transistors Using Composite Nitride Structure Stevens, Bailey, Taylor
Pat. 5,043,790 (RAM 322)	U.S.	04/05/1990	Sealed Self Aligned Contacts Using Two Nitrides Process Butler

Pat. 5,216,281 (RAM 322 CIP)	U.S.	08/26/1991	Sealed Self Aligned Contact Incorporating A Dopant Source Butler
Pat. 2005865 (RAM 322 JPN)	Japan	04/05/1991	Sealed Self Aligned Contacts Using Two Nitrides Process Butler
Pat. 5,134,310 (RAM 324)	U.S.	01/23/1991	Current Supply Circuit For Driving High Capacitance Load In An Integrated Circuit Mobley, Eaton
Pat. 2932122 (RAM 324 JPN)	Japan	01/23/1992	Current Supply Circuit For Driving High Capacitance Load In An Integrated Circuit Mobley, Eaton
Pat. 5,117,177 (RAM 325)	U.S.	01/23/1991	Reference Generator For An Integrated Circuit Eaton
Pat. 3106216 (RAM 325 JPN)	Japan	01/23/1992	Reference Generator For An Integrated Circuit Eaton
Pat. 5,255,222 (RAM 326)	U.S.	01/23/1991	Output Control Circuit Having Continuously Variable Drive Current Eaton
Pat. 3136424 (RAM 326 JPN)	Japan	01/22/1992	Output Control Circuit Having Continuously Variable Drive Current Eaton
Pat. 5,699,317 (RAM 343 CIP)	U.S.	10/06/1994	Enhanced Dram With All Reads From On-Chip Cache And All Writes To Memory Array Mobley, Sartore, Carrigan, Jones
Pat. 5,721,862 (RAM 343 CON)	U.S.	06/02/1995	Enhanced Dram With Single Row SRAM Cache For All Device Read Operations Mobley, Sartore, Carrigan, Jones
Pat. 69324508.6 (RAM 343 DE)	Germany	01/14/1993	Edram With Embedded Registers Mobley, Sartore, Carrigan, Jones
Pat. 5,887,272 (RAM 343 DIV)	U.S.	07/03/1997	Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones

Pat. 6,347,357 (RAM 343 DIV/CON)	U.S.	10/30/1998	Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones
App. 09/962,287 (RAM 343 DIV/CON2)	U.S.	09/24/2001	Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones
Pat. 2851503 (RAM 343 JPN)	Japan	01/21/1993	EDRAM Having A Dynamically-Sized Cache Memory And Associated Method Mobley, Sartore, Carrigan, Jones
Pat. 5,566,318 (RAM 381)	U.S.	08/02/1994	Circuit With A Single Address Register That Augments A Memory Controller By Enabling Cache Reads And Page-Mode Writes Joseph
Pat. 5,835,442 (RAM 393)	U.S.	03/22/1999	EDRAM With Integrated Generation And Control Of Write Enable And Column Latch Signals And Method For Making Same Joseph, D.N. Heisler, D.J. Heisler
Pat. 5,991,851 (RAM 417)	U.S.	05/02/1997	Enhanced Signal Processing Random Access Memory Device Utilizing A Dram Memory Array Integrated With An Associated SRAM Cache And Internal Refresh Control Alwais, Mobley
Pat. 5,901,100 (RAM 418)	U.S.	04/01/1997	First-In, First-Out Integrated Circuit Memory Device Utilizing A Dynamic Random Access Memory Array For Data Storage Implemented In Conjunction With An Associated Static Random Access Memory Cache Taylor
Pat. 6,072,741 (RAM 418 CIP)	U.S.	03/11/1999	First-In, First-Out Integrated Circuit Memory Device Utilizing A Dynamic Random Access Memory Array For Data Storage Implemented In Conjunction With An Associated Static Random Access Memory Cache Taylor
Pat. 6,172,927 (RAM 418 CIP2)	U.S.	03/24/2000	First-In, First-Out Integrated Circuit Memory Device Incorporating A Retransmit Function Taylor

Pat. 6,141,281 (RAM 429)	U.S.	04/29/1998	Technique For Reducing Element Disable Fuse Pitch Requirements In An Integrated Circuit Device Incorporating Replaceable Circuit Elements Mobley, Ash
Pat. 6,055,192 (RAM 430)	U.S.	09/03/1998	Dynamic Random Access Memory Word Line Boost Technique Employing A Boost-On-Writes Policy Mobley
Pat. 6,064,620 (RAM 432)	U.S.	07/08/1998	Multi-Array Memory Device, And Associated Method, Having Shared Decoder Circuitry Mobley
Pat. 6,278,646 (RAM 432 CIP)	U.S.	03/29/2000	Multi-Array Memory Device And Associated Method Having Shared Decoder Circuitry Mobley
Pat. 5,963,481 (RAM 447)	U.S.	06/30/1998	Embedded Enhanced DRAM And Associated Method Alwais, Peters
App. 99302956.0 (RAM 447 EPO)	Europe	04/16/1999	Embedded Enhanced DRAM And Associated Method Alwais, Peters
Pat. 6,249,840 (RAM 448)	U.S.	10/23/1998	Multi-Bank Esdram With Cross-Coupled SRAM Cache Registers Peters
Pat. 6,330,636 (RAM 450)	U.S.	01/25/1999	Double Data Rate Synchronous Dynamic Random Access Memory Device Incorporating A Static RAM Cache Per Memory Bank Bondurant, Peters, Mobley
Pat. 6,151,236 (RAM 460)	U.S.	02/29/2000	Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Grieshaber, Mobley, Peters
Pat. 6,301,183 (RAM 460 CON)	U.S.	07/27/2000	Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Grieshaber, Mobley, Peters

App. 2001-052888 (RAM 460 JPN)	Japan	02/27/2001	Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Griesheber, Mobley, Peters
Pat. 6,392,441 (RAM 461)	U.S.	06/13/2000	Fast Response Circuit Mosczuk
Pat. 6,373,751 (RAM 463)	U.S.	05/15/2000	Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant
Pat. 6,549,472 (RAM 463 CON)	U.S.	02/21/2002	Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant
Pat. 6,646,928 (RAM 463 DIV)	U.S.	01/16/2003	Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant
Pat. 6,501,698 (RAM 464)	U.S.	11/01/2000	Structure And Method For Hiding DRAM Cycle Time Behind A Burst Access Mobley
App. 09/828,283 (RAM 465)	U.S.	04/05/2001	Method For Hiding A Refresh In A Pseudo-Static Memory Mobley
Pat. 6,536,928 (RAM 466)	U.S.	10/11/2000	Method For Reducing The Width Of A Global Data Bus In A Memory Architecture Mobley
App. 09/828,488 (RAM 467) App. 10/782,386 (RAM 467 CON)	U.S.	04/05/2001 02/18/2004	Method And Circuit For Increasing The Memory Access Speed Of An Enhanced Synchronous SDRAM Peters

App. 10/178,072 (RAM491)	U.S.	06/20/2002	Method And Circuit For Increasing The Memory Access Speed Of An Enhanced Synchronous SDRAM Mobley, Peters, Schuette
Pat. 5,787,457	U.S.	10/18/1995	Cached Synchronous DRAM Architecture Allowing Concurrent DRAM Operations Miller, Rogers, Tomashot, Bondurant, Jones, Jr., Mobley
Pat. 6,269,416	U.S.	10/15/1999	Cached Synchronous DRAM Architecture Having A Mode Register Programmable Cache Policy Rogers, Tomashot, Bondurant, Jones, Jr., Mobley