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U.S. DEPARTMENT OF COMMERCE  
U.S. Patent and Trademark Office

Tab settings ⇌⇌⇌

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To the honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):  
Altera Corporation

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment☐ Merger☐ Security Agreement☐ Change of Name☐ Other \_\_\_\_\_Execution Date December 20, 2002, April 7, 2003

2. Name and address of receiving party(ies)

Name: PTS Corporation

Internal Address: \_\_\_\_\_

Street Address: 101 Innovation DriveCity: San Jose State: CA Zip: 95134Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: \_\_\_\_\_

A. Patent Application No.(s)  
**See attached sheet.**

B. Patent No.(s)  
**See attached sheet.**

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Peter H. PriestPriest & Goldstein, PLLC

Internal Address: \_\_\_\_\_

Street Address: 5015 Southpark DriveSuite 230City: Durham State: NC Zip: 27713-77366. Total number of applications and patents involved: 597. Total fee (37 CFR 3.41). . . . . \$ 2,360.00☐ Enclosed

(no fee enclosed as the \$2,360.00 was previously paid)

☒ Credit any overpayment or charge any underpayment to Deposit Account

8. Deposit account number:

50-1058

(Attach duplicate copy of this page if paying by deposit account)

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9. Statement and signature.

*To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.*

Peter H. Priest

Name of Person Signing

Signature

November 19, 2003

Date

Total number of pages including cover sheet, attachments, and documents: 38

11/25/2003 LNUELLER 00000018 09598566

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2360.00 DP

Mail documents to be recorded with required cover sheet information to:  
Commissioner of Patents & Trademarks, Box Assignments  
Washington, D.C. 20231

**PATENT**  
**REEL: 014683 FRAME: 0914**

**US. Patent Applications**

09/598,566  
09/432,705  
09/747,056  
09/337,839  
09/599,980  
09/598,567  
09/598,564  
09/598,558  
09/598,084  
09/711,218  
09/791,940  
09/791,256  
09/792,819  
10/004,010  
09/853,989  
09/886,855  
10/116,221  
10/013,908  
10/004,578  
09/783,156  
10/131,941  
09/796,040  
10/136,651  
10/282,925  
10/119,660  
10/282,919  
09/969,077  
10/036,789  
10/073,782  
10/114,652  
10/114,646  
10/254,049  
10/254,012  
10/254,105

**U.S. Patents**

6,023,753  
6,167,502  
6,151,668  
6,343,356  
6,167,501  
6,101,592  
6,173,389  
6,216,223  
6,366,999  
6,219,776  
6,446,190  
6,397,324  
6,356,994  
6,256,683  
6,260,082  
6,338,129  
6,408,382  
6,321,322  
6,366,997  
6,446,191  
6,470,441  
6,467,036  
6,430,677  
6,453,367  
6,457,073

## ASSIGNMENT AND TRANSFER OF PATENTS

**WHEREAS**, Altera Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, California, 95134 ("Assignor") owns certain patent applications and/or registrations, as listed in Exhibit A attached hereto and incorporated herein by this reference ("Patents"); and

**WHEREAS**, PTS Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, California 95134 ("Assignee"), desires to acquire all of the right, title and interest of Assignor in, to and under the Patents;

**WHEREAS**, Assignor and Assignee have entered into an agreement providing for the assignment of, among other things, all right, title and interest in and to the Patents and in and to the registrations for same from Assignor to Assignee. The parties wish to enter into this assignment to effect the legal and beneficial transfer of all rights in and to the Patents and to fully vest the same in the Assignee;


**NOW, THEREFORE**, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor does hereby irrevocably sell, assign, transfer and convey unto Assignee all of its right, title and interest in and to the Patents, including all divisions, continuations, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the Patents (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the Patents throughout the universe, including without limitation all foreign counterparts and foreign equivalents of any of the foregoing.

Assignor authorizes and requests the patent officials in the United States and in any and all foreign jurisdictions to issue any and all letters patent and foreign counterparts or equivalents thereof to PTS Corporation, as assignee of the entire interest of Assignor therein, and covenants that Assignor has full right to convey the entire interest herein assigned and that Assignor has not executed and will not execute any agreements in conflict herewith.

Assignor further agrees, for itself, its successors and assigns, to execute such further documents and to perform such further lawful acts as may reasonably be required to effectuate this assignment.

IN WITNESS WHEREOF, Assignor and Assignee have caused this assignment to be duly executed by an authorized officer to be effective April 7, 2003.

ALTERA CORPORATION

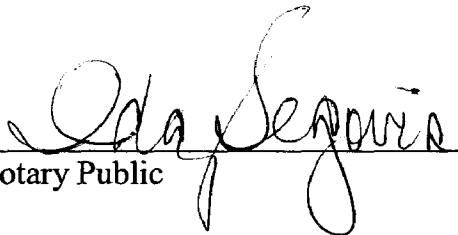
By 

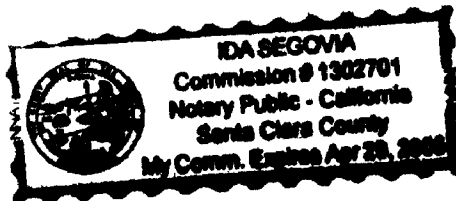
Name: Derek E. Minihane

Title: Director, IP Law and Assistant Secretary

On this 7th day of April 2003, personally appeared Derek Minihane to me known, who, being duly sworn, did depose and say that he/~~she~~ is the Assistant Secretary of the corporation described in and which executed the foregoing instrument that he/~~she~~ is duly authorised to execute the foregoing instrument.

STATE OF California  
COUNTY OF Santa Clara

  
Notary Public



**EXHIBIT A****PATENTS**

Client No.	Title	Country.	Inventors	Application No.
	Filing Date	Patent No.		
<b>800.0001</b>	Manifold Array Processor 6/30/1997	U.S. 6,023,753	Pechanek, G	08/885,310
800.0001-PCT	Manifold Array Processor 6/24/1998	PCT	Kurak, Jr.,	PCT/US98/13111
800.0001-EP	Manifold Array Processor 6/24/1998	EP 1002279		98932831.5-2201
800.0001-CA	Manifold Array Processor 6/24/1998	CA		2,295,109
800.0001-CN	Manifold Array Processor 6/24/1998	CN		98806757.9
800.0001-IL	Manifold Array Processor 6/24/1998	IL		133,691
800.0001-JP	Manifold Array Processor 6/24/1998	JP		11-505670
800.0001-KR	Manifold Array Processor 6/24/1998	KR		10-1999-7012547
800.0001-MX	Manifold Array Processor 6/24/1998	MX		09911982
<b>800.0002</b>	Method and Apparatus for 10/10/1997 Manifold Array Processing	U.S. 6,167,502	Pechanek, G	08/949,122
800.0002-PCT	Method and Apparatus for 10/9/1998 Manifold Array Processing	PCT	Pitsianis, N Barry, E	PCT/US98/21478
800.0002-EP	Method and Apparatus for 10/9/1998 Manifold Array Processing	EP 1034484		98954956.3
800.0002-CA	Method and Apparatus for 10/9/1998 Manifold Array Processing	CA		2,305,221
800.0002-CN	Method and Apparatus for 10/9/1998 Manifold Array Processing	CN		98809446.0
800.0002-IL	Method and Apparatus for 10/9/1998 Manifold Array Processing	IL		135,535
800.0002-JP	Method and Apparatus for 10/9/1998 Manifold Array Processing	JP		2000-516291
800.0002-KR	Method and Apparatus for 10/9/1998 Manifold Array Processing	KR		10-2000-7003864
800.0002-MX	Method and Apparatus for 10/9/1998 Manifold Array Processing	MX		3003
<b>800.0004</b>	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	U.S. 6,151,668	Pechanek, G Drabenstott, Revilla, J	09/187,539

800.0004-PCT	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	PCT		PCT/US98/23650
800.0004-EP	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	EP 1029266		98957630.1
800.0004-CA	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	CA		2,310,584
800.0004-CN	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	CN		98810767.8
800.0004-IL	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	IL		135,953
800.0004-JP	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	JP		2000-51983
800.0004-KR	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	KR		10-2000-7004975
800.0004-MX	Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	MX		3803
<b>800.0004.PROV</b>	Methods and Apparatus for 11/7/1997 Efficient Synchronous MIMD VLIW Communication	U.S.	Pechanek, G  Drabenstott, Revilla, J	60/064,619
<b>800.0011</b>	Methods and Apparatus for 10/9/1998 Dynamic Instruction Controlled Reconfiguration Reg	U.S. 6,343,356	Pechanek, G  Barry, E	09/169,255
<b>800.0011.PROV</b>	Methods and Apparatus for 7/9/1998 Dynamic Instruction Controlled Reconfiguration Reg	U.S.	Pechanek, G  Barry, E	60/092,148
<b>800.0012</b>	Methods and Apparatus for 10/9/1998 ManArray PE-PE Switch Control	U.S. 6,167,501	Barry, E  Pechanek, G Drabenstott,	09/169,256
800.0012-PCT	Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control	PCT		PCT/US99/23493
800.0012-EP	Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control	EP 1137999		99953107.2
800.0012-JP	Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control	JP		2000-576380

<b>800.0012.PROV</b>	Methods and Apparatus for 6/5/1998 ManArray PE-PE Switch Control	U.S.	Barry, E  Pechanek, G Drabenstott,	60/088,148
<b>800.0013</b>	Methods and Apparatus for 12/18/1998 Scalable Instruction Set Architecture with Dynamic Comp	U.S. 6,101,592	Pechanek, G  Barry, E Revilla, J	09/215,081
800.0013-PCT	Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp	PCT		PCT/US99/29516
800.0013-EP	Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp	EP		99968117.4
800.0013-IL	Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp	IL		143,431
800.0013-JP	Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp	JP		2000-590073
<b>800.0013.PROV</b>	Methods and Apparatus for 12/18/1997 Scalable Instruction Set Architecture	U.S.	Pechanek, G  Barry, E Drabenstott,	60/068,021
<b>800.0016</b>	Methods and Apparatus for 12/4/1998 Dynamic Very Long Instruction Word Sub-Instruction Selection System for Dynamic VLIW	U.S. 6,173,389	Pechanek, G  Revilla, J Barry, E	09/205,588
800.0016-PCT	Sub-Instruction Selection for Execution Time Parallelism in System for Dynamic VLIW 12/2/1999	PCT		PCT/US99/28506
800.0016-EP	Sub-Instruction Selection for Execution Time Parallelism in System for Dynamic VLIW 12/2/1999	EP 1247196		99965084.9
800.0016-JP	Sub-Instruction Selection for Execution Time Parallelism in System for Dynamic VLIW 12/2/1999	JP		2000-596762
800.0016-IL	Sub-Instruction Selection for Execution Time Parallelism in System for Dynamic VLIW 12/2/1999	IL		143,430
<b>800.0016.PROV</b>	Method and Apparatus for 12/4/1997 Dynamically Modifying Instructions in a Very Long In	U.S.	Revilla, J  Barry, E Pechanek, G	60/067,511
<b>800.0017</b>	Methods and Apparatus to 1/12/1999 Dynamically Reconfigure the Instruction Pipeline of an Ind	U.S. 6,216,223	Revilla, J  Barry, E Marchand, P	09/228,374



800.0017-PCT	Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of Indire	PCT		PCT/US00/00569
800.0017-EP	Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind	EP		00903213.7-2201
800.0017-IL	Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind	IL		144,162
800.0017-JP	Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind	JP		2000-594009
<b>800.0017.PROV</b>	Methods and Apparatus to 1/12/1998 Dynamically Expand the Instruction Pipeline of a Very	U.S.	Revilla, J	60/071,248
<b>800.0021</b>	Methods and Apparatus to 1/28/1999 Support Conditional Execution in a VLIW-Based Array Processo	U.S. 6,366,999	Drabenstott, Pechanek, G	09/238,446
800.0021-PCT	Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo	PCT	Barry, E	PCT/US00/01803
800.0021-EP	Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo	EP 1196855		00911637.7
800.0021-IL	Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo	IL		144,562
800.0021-JP	Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo	JP		2000-596471
<b>800.0021.PROV</b>	Methods and Apparatus to 1/28/1998 Support Conditional Execution in a VLIW-Based Array Processo	U.S.	Drabenstott, Pechanek, G Revilla, J	60/072,915
<b>800.0022</b>	Merged Array Controller with 10/9/1998 Processing Element	U.S. 6,219,776	Pechanek, G	09/169,072
800.0022-PCT	Methods and Apparatus for 10/8/1999 Dynamically Merging an Array Controller with an Array Proce	PCT	Revilla, J	PCT/US99/23495
800.0022-EP	Methods and Apparatus for 10/8/1999 Dynamically Merging an Array Controller with an Array Proce	EP 1127316		99953109.8
800.0022-JP	Methods and Apparatus for 10/8/1999 Dynamically Merging an Array	JP		2000-576374

	Controller with an Array Proce			
<b>800.0022.PROV</b>	Methods and Apparatus for 3/10/1998 Dynamically Merging an Array Controller with an Array Proce	U.S.	Pechanek, G  Revilla, J	60/077,457
<b>800.0023</b>	Register File Indexing 3/12/1999	U.S. 6,446,190	Barry, E	09/267,570
800.0023-PCT	Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000	PCT	Pechanek, G Marchand, P	PCT/US00/06334
800.0023-EP	Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000	EP		00913887.6
800.0023-CA	Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000	CA		
800.0023-IL	Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000	IL		144,970
800.0023-JP	Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 Methods and Apparatus for Providing Indirect Control of	JP		2000-604303
<b>800.0023.PROV</b>	Register File Indexing 3/12/1998 Methods and Apparatus for Providing Indirect Control of	U.S.	Barry, E	60/077,766
<b>800.0024</b>	Accessing Tables in Memory 6/16/2000	U.S. 6,397,324	Barry, E	09/596,103
800.0024-PCT	Banks Using Load and Store Address Generators Sharing Sto Methods and Apparatus for 5/10/2001	PCT	Kurak, Jr., Pechanek, G	PCT/US01/15232
800.0024-EP	Data Dependent Address Operations and Efficient Varia Methods and Apparatus for 5/10/2001 Data Dependent Address Operations and Efficient Varia	EP		01935327.5
<b>800.0024.PROV</b>	Methods and Apparatus for 6/18/1999 Data Dependent Address Operations and Efficient Varia	U.S.	Barry, E  Kurak, Jr., Pechanek, G	60/139,946
<b>800.0025</b>	Methods and Apparatus for 6/21/2000	U.S.	Barry, E	09/598,566
800.0025-PCT	Generalized Event Detection and Action Specification in a Methods and Apparatus for 6/21/2000 Generalized Event Detection	PCT	Marchand, P Pechanek, G	PCT/US00/40273

800.0025-EP	and Action Specification in a Methods and Apparatus for 6/21/2000 Generalized Event Detection and Action Specification in a	EP		00955904.8
<b>800.0025.PROV</b>	Methods and Apparatus for 6/21/1999 Generalized Event Detection and Action Specification in a	U.S.	Barry, E  Marchand, P Pechanek, G	60/140,245
<b>800.0026</b>	Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding	U.S.	Kurak, Jr.,  Moller, C	09/432,705
800.0026-PCT	Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding	PCT		PCT/US99/25707
800.0026-EP	Improved Motion Estimation 11/2/1999	EP 1157559		99971615.2
800.0026-JP	Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding	JP		2000-580388
800.0026-IL	Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding	IL		142,856
<b>800.0026.PROV</b>	Methods and Apparatus for 11/3/1998 Improved Motion Estimation for Video Encoding	U.S.		60/106,867
<b>800.0027</b>	Methods and Apparatus for 7/9/1999 Instruction Addressing in Indirect VLIW Processors	U.S. 6,356,994	Barry, E  Pechanek, G	09/350,191
800.0027-PCT	Methods and Apparatus for 7/7/2000 Instruction Addressing in Indirect VLIW Processors	PCT		PCT/US00/40143
800.0027-EP	Methods and Apparatus for 6/7/2000 Instruction Addressing in Indirect VLIW Processors	EP		00943442.4
<b>800.0027.PROV</b>	Methods and Apparatus for 7/9/1998 Instruction Addressing in Indirect VLIW Processors	U.S.	Barry, E	60/092,130
<b>800.0028</b>	Methods and Apparatus for 12/22/2000 Loading a Very Long Instruction Word Memory	U.S.	Barry, E  Pechanek, G	09/747,056
<b>800.0028.PROV</b>	Methods and Apparatus for 12/23/1999 Loading a Very Long Instruction Word Memory	U.S.	Barry, E  Pechanek, G	60/171,911

<b>800.0029</b>	Efficient Complex 6/22/1999 Multiplication and Fast Fourier Transform (FFT) Implem	U.S.	Pitsianis, N	09/337,839
800.0029-PCT	Efficient Complex 10/8/1999 Multiplication and Fast Fourier Transform (FFT) Implem	PCT	Pechanek, G Rodriguez, R	PCT/US99/23494
800.0029-EP	Efficient Complex 10/8/1999 Multiplication and Fast Fourier Transform (FFT) Implem	EP 1141819		99953108.0
800.0029-JP	Efficient Complex 10/8/1999 Multiplication and Fast Fourier Transform (FFT) Implem	JP		2000-576342
<b>800.0029.CPA</b>	Efficient Complex 6/22/1999 Multiplication and Fast Fourier Transform (FFT) Implem	U.S.	Pitsianis, N	09/337,839
<b>800.0029.PROV</b>	Efficient Complex 10/9/1998 Multiplication and Fast Fourier Transform (FFT) Implem	U.S.	Pitsianis, N	60/103,712
<b>800.0030</b>	Methods and Apparatus for 12/23/1999 Providing Direct Memory Access Control	U.S. 6,256,683	Barry, E	09/472,372
800.0030-PCT	Methods and Apparatus for 12/19/2000 Providing Direct Memory Access Control	PCT		PCT/US00/34456
800.0030-EP	Methods and Apparatus for 12/19/2000 Providing Direct Memory Access Control	EP		00986567.6
<b>800.0030.PROV</b>	Methods and Apparatus for 12/23/1998 Providing Direct Memory Access (DMA) Engine	U.S.	Barry, E Wolff, E	60/113,637
<b>800.0031</b>	Methods and Apparatus for 12/23/1999 Providing Data Transfer	U.S. 6,260,082	Barry, E	09/471,217
800.0031-PCT	Methods and Apparatus for 12/19/2000 Providing Data Transfer	PCT	Wolff, E	PCT/US00/34454
800.0031-EP	Methods and Apparatus for 12/19/2000 Providing Data Transfer	EP		00988150.9
<b>800.0031.PROV</b>	Methods and Apparatus 12/23/1998 Providing Transfer Control	U.S.	Barry, E Wolff, E	60/113,555
<b>800.0032</b>	Manifold Array Processor 6/1/1999	U.S. 6,338,129	Pechanek, G	09/323,609

<b>800.0034</b>	Methods and Apparatus for 6/22/2000 Parallel Processing Utilizing a Manifold Array (ManArray) Ar	U.S.	Kurak, Jr., Pechanek, G	09/599,980
<b>800.0034.PROV</b>	Methods and Apparatus for 6/22/1999 Parallel Processing Utilizing a Manifold Array (ManArray) Ar	U.S.	Strube, D Barry, E	60/140,425
<b>800.0035</b>	Methods and Apparatus for 6/21/2000 Improved Efficiency in Pipeline Simulation and Emulat	U.S.	Moller, C	09/598,567
<b>800.0035.PROV</b>	Methods and Apparatus for 6/21/1999 Improved Efficiency in Pipeline Simulation and Emulat	U.S.	Busboom, C Schneider, D	60/140,163
<b>800.0036</b>	Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI	U.S.	Pechanek, G	09/598,564
800.0036-PCT	Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI	PCT	Strube, D Wolff, E	PCT/US00/40283
800.0036-EP	Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI	EP		00960114.7
<b>800.0036.PROV</b>	Methods and Apparatus for 6/21/1999 Initiating and Resynchronizing Multi-Cycle SI	U.S.	Pechanek, G	60/140,162
<b>800.0037</b>	Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi	U.S.	Strube, D Morris, G	09/598,558
800.0037-PCT	Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi	PCT	Barry, E	PCT/US00/40272
800.0037-EP	Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi	EP	Pechanek, G Strube, D	00955903.0
<b>800.0037.PROV</b>	Methods and Apparatus for 6/21/1999 Providing One-by-One Manifold Array (1x1 ManArray) Program C	U.S.	Barry, E	60/140,244
<b>800.0038</b>	Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor	U.S.	Strube, D	09/598,084
			Barry, E	
			Wolff, E Marchand, P	

800.0038-PCT	Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor	PCT		PCT/US00/40263
800.0038-EP	Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor	EP		00951075.1
<b>800.0038.PROV</b>	Methods and Apparatus for 6/21/1999 Establishing Port Priority Functions in a VLIW Processor	U.S.	Barry, E	60/140,325
<b>800.0039</b>	Methods and Apparatus for 10/21/1999 Abbreviated Instruction Sets Adaptable to Configurable Proc	U.S. 6,408,382	Pechanek, G	09/422,015
800.0039-PCT	Methods and Apparatus for 10/16/2000 Abbreviated Instruction and Configurable Processor Archite	PCT	Kurak, Jr., Larsen, L	PCT/US00/28622
800.0039-EP	Methods and Apparatus for 10/16/2000 Abbreviated Instruction and Configurable Processor Archite	EP		00970952.8
<b>800.0040</b>	Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations	U.S.	Kurak, Jr., Pechanek, G	09/711,218
800.0040-PCT	Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations	PCT		PCT/US00/31120
800.0040-EP	Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations	EP		00977189.0
<b>800.0040.PROV</b>	Methods and Apparatus for 11/12/1999 Efficient Cosine Transform Implementations	U.S.	Kurak, Jr., Pechanek, G	60/165,337
<b>800.0042</b>	Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing	U.S.	Barry, E	09/791,940
800.0042-PCT	Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing	PCT	Pitsianis, N Coopman, K	PCT/US01/05714
800.0042-EP	Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing	EP		01912939.4
<b>800.0042.PROV</b>	Methods and Apparatus for 2/24/2000 Providing Bit-Reversal and Multicast Functions Utilizing	U.S.	Barry, E Pitsianis, N Coopman, K	60/184,668

<b>800.0043</b>	Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon	U.S.	Barry, E	09/791,256
800.0043-PCT	Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon	PCT	Marchand, P Pechanek, G	PCT/US01/06058
800.0043-EP	Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon	EP		01916233.8
<b>800.0043.PROV</b>	Methods and Apparatus for 2/24/2000 Scalable Array Processor Interrupt Detection and Respon	U.S.	Barry, E	60/184,529
			Marchand, P Pechanek, G	
<b>800.0044</b>	Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface	U.S.	Barry, E	09/792,819
800.0044-PCT	Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface	PCT		PCT/US01/06004
800.0044-EP	Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface	EP		01914486.4
<b>800.0044.PROV</b>	Methods and Apparatus for 2/24/2000 Flexible Strength Coprocessing Interface	U.S.	Barry, E	60/184,560
<b>800.0045.PROV</b>	Efficient Transformation and 3/29/2002 Lighting Implementation for 3D Graphics	U.S.	Rodriguez, R	60/368,509
			Jacobs, M Strube, D	
<b>800.0046</b>	Methods and Apparatus for 11/1/2001 Efficient Complex Long Multiplication and Covariance	U.S.	Pechanek, G	10/004,010
800.0046-PCT	Methods and Apparatus for 11/1/2001 Efficient Complex Long Multiplication and Covariance	PCT	Rodriguez, R Plonski, M	PCT/US01/45172
800.0046-EP	Methods and Apparatus for Efficient Complex Long Multiplication and Covariance	EP		01992935.5
<b>800.0046.PROV</b>	Methods and Apparatus for 11/1/2000 Efficient Complex Long Multiplication and Covariance	U.S.	Pechanek, G	60/244,861
			Rodriguez, R Plonski, M	
<b>800.0049</b>	Methods and Apparatus for 4/5/2000 Scalable Instruction Set	U.S. 6,321,322	Pechanek, G	09/543,473
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<b>800.0052</b>	Methods and Apparatus for 5/11/2001 Power Control in a Scalable Array of Processor Elements	U.S.	Marchand, P  Pechanek, G Wolff, E	09/853,989
<b>800.0052.PROV</b>	Methods and Apparatus for 5/12/2000 Power Control in a Scalable Array of Processor Elements	U.S.	Marchand, P  Pechanek, G Wolff, E	60/203,629
<b>800.0053</b>	Methods and Apparatus for 6/21/2001 Indirect VLIW Memory	U.S.	Pitsianis, N  Strautin, B Banerjee, S	09/886,855
800.0053.PCT	Methods and Apparatus for 6/21/2001 Indirect VLIW Memory	PCT		PCT/US01/19851
800.0053-EP	Methods and Apparatus for 6/21/2001 Indirect VLIW Memory	EP		01946628.3
<b>800.0053.PROV</b>	Methods and Apparatus for 6/21/2000 Indirect VLIW Memory	U.S.	Pitsianis, N  Strautin, B Banerjee, S	60/212,987
<b>800.0057</b>	Methods and Apparatus for 4/4/2002 Generating Functional Test Programs by Traversing a Finit	U.S.	Raimi, R  Aloul, F	10/116,221
<b>800.0057.PROV</b>	Methods and Apparatus for 4/4/2001 Generating Functional Test Programs by Traversing a Finit	U.S.	Raimi, R  Aloul, F	60/281,523
<b>800.0066</b>	Methods and Apparatus for 8/29/2000 ManArray PE-PE Switch Control	U.S. 6,366,997	Barry, E  Pechanek, G Drabenstott,	09/649,647
<b>800.0067</b>	Methods and Apparatus for 10/2/2000 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE	U.S. 6,446,191	Pechanek, G  Drabenstott, Revilla, J	09/677,732
<b>800.0069</b>	Method and Apparatus for 11/6/2000 Manifold Array Processing	U.S. 6,470,441	Pechanek, G  Pitsianis, N Barry, E	09/707,209
<b>800.0071</b>	Methods and Apparatus for 11/21/2000 Dynamic Very Long Instruction Word Sub-Instruction Selection	U.S. 6,467,036	Pechanek, G  Revilla, J Barry, E	09/717,992
<b>800.0072</b>	Methods and Apparatus for 2/28/2001 Dynamic Instruction Controlled Reconfigurable Regi	U.S. 6,430,677	Pechanek, G  Barry, E	09/796,037



<b>800.0073</b>	Methods and Apparatus for 10/19/2001 Efficient Vocoder	U.S.	Sadri, A  Jaffer, N Silivra, A	10/013,908
<b>800.0073-PCT</b>	Methods and Apparatus for 10/19/2001 Efficient Vocoder	PCT		PCT/US01/45451
<b>800.0073-EP</b>	Methods and Apparatus for 10/19/2001 Efficient Vocoder	EP		01989028.4
<b>800.0073.PROV</b>	Methods and Apparatus for 10/20/2000 Efficient Vocoder	U.S.	Sadri, A  Jaffer, N Silivra, A	60/241,940
<b>800.0077</b>	Methods and Apparatus for 12/4/2001 Providing Improved Physical Designs and Routing with Reduc	U.S.	Chandna, A  O'Brien, T Brown, D	10/004,578
<b>800.0077.PROV</b>	Methods And Apparatus for 12/4/2000 Providing Improved Physical Designs and Routing with Reduc	U.S.	Chandna, A  Brown, D	60/251,072
<b>800.0078</b>	Merged Array Controller with 2/14/2001 Processing Element	U.S.	Pechanek, G  Revilla, J	09/783,156
<b>800.0079</b>	Methods and Apparatus for 5/14/2001 Providing Direct Memory Access Control	U.S. 6,453,367	Barry, E	09/854,789
<b>800.0080</b>	Methods and Apparatus for 4/25/2002 Pipelined Bus	U.S.	Wolff, E  Baker, D Cope, B	10/131,941
<b>800.0080.PROV</b>	Methods and Apparatus for 4/27/2001 Pipelined Bus	U.S.	Wolff, E  Baker, D Cope, B	60/287,270
<b>800.0081</b>	Methods and Apparatus to 2/28/2001 Dynamically Reconfigure the Instruction Pipeline of an Ind	U.S.	Revilla, J  Barry, E Marchand, P	09/796,040
<b>800.0088</b>	Methods and Apparatus for 5/1/2002 Removing Compression Artifacts in Video Sequences	U.S.	Petrescu, D	10/136,651
<b>800.0088.PROV</b>	Methods and Apparatus for 5/4/2001 Removing Compression Artifacts in Video Sequences	U.S.	Petrescu, D	60/288,965

<b>800.0089</b>	Methods and Apparatus for 10/29/2002 Video Decoding	U.S.	Petrescu, D  Stern, T Jacobs, M	10/282,925
<b>800.0089.PROV</b>	Methods and Apparatus for 10/30/2001 Video Decoding	U.S.	Petrescu, D  Stern, T Jacobs, M	60/340,620
<b>800.0093</b>	Methods and Apparatus for 4/10/2002 Automated Generation of Abbreviated Instruction Set an	U.S.	Larin, S  Pechanek, G Conte, T	10/119,660
<b>800.0093.PROV</b>	Methods and Apparatus for 4/13/2001 Automated Generation of Abbreviated Instruction Set an	U.S.	Larin, S  Pechanek, G Conte, T	60/283,582
<b>800.0097</b>	Methods and Apparatus for a 10/29/2002 Bit Rake Instruction	U.S.	Wolff, E  Molnar, P Elezabi, A	10/282,919
<b>800.0097.PROV</b>	Methods and Apparatus for a 11/1/2001 Bit Rake Instruction	U.S.	Wolff, E  Molnar, P Elezabi, A	60/335,159
<b>800.0101</b>	Methods and Apparatus for 6/29/2001 Providing Data Transfer	U.S. 6,457,073	Barry, E  Wolff, E	09/896,687
<b>800.0104</b>	Methods and Apparatus for 9/28/2001 Scalable Instruction Set Architecture with Dynamic Comp	U.S.	Pechanek, G  Barry, E Revilla, J	09/969,077
<b>00.0114.PROV</b>	Motion Estimation Method for 4/18/2002 MPEG-4 Simple Profile Video Coding for a MPEG-4 Codec on M	U.S.	Petrescu, D  Searles, D	60/373,551
<b>800.0119</b>	Manifold Array Processor 12/21/2001	U.S.	Pechanek, G	10/036,789
<b>800.0121</b>	Methods and Apparatus for 2/11/2002 Instruction Addressing in Indirect VLIW Processors	U.S.	Barry, E  Pechanek, G	10/073,782
<b>800.0122</b>	Methods and Apparatus to 4/1/2002 Support Conditional Execution in a VLIW-Based Array Processo	U.S.	Drabenstott,  Pechanek, G Barry, E	10/114,652
<b>800.0123</b>	Methods and Apparatus for 4/1/2002 ManArray PE-PE Switch Control	U.S.	Barry, E  Pechanek, G Drabenstott,	10/114,646

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<b>800.0125</b>	Method and Apparatus for 9/24/2002 Manifold Array Processing	U.S.	Pechanek, G  Pitsianis, N Barry, E	10/254,049
<b>800.0126</b>	Methods and Apparatus for 9/24/2002 Dynamic Very Long Instruction Word Sub-Instruction Selection	U.S.	Pechanek, G  Revilla, J Barry, E	10/254,012
<b>800.0127</b>	Methods and Apparatus for 9/24/2002 Providing Data Transfer	U.S.	Barry, E  Wolff, E	10/254,105