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AMD Investments, Inc.
One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088-3453 U.S.A.

and

Fijitsu Limited
1-1 Kamikodanaka 4-Chome,
Nakahara-Ku Kawasaki-Shi,
Kanagawa-Ken,
211-8588 Japan

2. Name and address of receiving party(ies):

FASL LLC
One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088-3453 U.S.A.

3. Nature of conveyance:

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4. Application number(s) or patent number(s):
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5. Name and address of party to whom correspondence concerning the document should be mailed:

Wagner, Murabito & Hao LLP
2 N. Market Street
Third Floor
San Jose, CA 95113
ph. (408) 938-9060
fax (408) 938-9069

6. Total number of applications involved: **62**

7. Total fee (37 CFR 3.41) **$2,480.00**

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James P. Hao
Reg. No.: 36,398

July 6, 2004
Date

Total number of pages including cover sheet, attachments, and documents: 11 pages

CH $2480.00 230085 09676623

Attachment A

	App. No.	App. Date	Status	Patent No.	Grant Date	Inventors	Title	Docket No.
1	09/676,623	10/2/00	Filed			KURIHARA, KAZUHIRO (FUJITSU) CHEN, PAU-LING 15896	I/O BASED COLUMN REDUNDANCY FOR VIRTUAL GROUND WITH 2-BIT CELL FLASH MEMORY	AF01045
2	09/741,320	12/19/00	Filed			NGUYEN, KENDRA LIN, JIN-LIEN AKAOGI, TAKAO N/E AL-SHAMMA, ALI K. CLEVELAND, LEE 22191 TEH, BOON-TANG (PNG)	INITIAL LATENCY CLOCKING FOR BURST MODE READ IN A BURST MODE MEMORY DEVICE	AF01079
3	10/431,320	5/6/03	Filed			KURIHARA, KAZUHIRO (FUJITSU) LE, BINH QUANG 23326 (CA) CHEN, PAU-LING 15896 HAMILTON, DARLENE G. 21331 (CA) HSIA, EDWARD 22517	NON-VOLATILE MEMORY READ CIRCUIT WITH END OF LIFE SIMULATION	AF01154
4	10/243,315	9/12/02	Filed			YANG, TIEN-CHUN SHIEH, MING-HUEL KURIHARA, KAZUHIRO (FUJITSU) CHEN, PAU-LING 15896	SYSTEM AND METHOD FOR Y-DECODING IN A FLASH MEMORY DEVICE	AF01165
5	10/264,387	10/4/02	Filed			YANG, TIEN-CHUN YAMADA, SHIGEKAZU (FUJITSU) SHIEH, MING-HUEL CHEN, PAU-LING 15896	GROUND STRUCTURE FOR PAGE READ AND PAGE WRITE FOR FLASH MEMORY	AF01166
6	10/431,065	5/6/03	Filed			RUNNION, ED YANG, TIEN-CHUN LE, BINH QUANG 23326 (CA) YAMADA, SHIGEKAZU (FUJITSU) HAMILTON, DARLENE G. 21331 (CA)	METHOD TO OBTAIN TEMPERATURE INDEPENDENT PROGRAM THRESHOLD VOLTAGE DISTRIBUTION USING TEMPERATURE DEPENDENT VOLTAGE REFERENCE	AF01168
7	10/387,774	3/12/03	Filed			OGAWA, HIROYUKI (FUJITSU) SUN, YU 10853 HUI, ANGELA T. 21104 (CA)	METHOD FOR FABRICATING MEMORY DEVICE HAVING REVERSE LDD	AF01174
8	10/086,112	2/27/02	Granted	6,750,103	6/15/04	MASAAKI, HIGASHITAHI (FJ) RANDOLPH, MARK 63721	NROM CELL WITH N-LESS CHANNEL	AF01047
9	10/243,792	9/12/02	Granted	6,744,666	6/1/04	YACHARENI, SANTOSH K KURIHARA, KAZUHIRO (FUJITSU) SHIEH, MING-HUEL CHEN, PAU-LING 15896	METHOD AND SYSTEM TO MINIMIZE PAGE PROGRAMMING TIME FOR FLASH MEMORY DEVICES	AF01164
10	09/422,198	10/19/99	Granted	6,259,633	7/10/01	CHEN, TIEN-MIN KURIHARA, KAZUHIRO (FUJITSU) AKAOGI, TAKAO N/E	SENSE AMPLIFIER ARCHITECTURE FOR SLIDING BANKS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01001

Attachment A

11	09/421,985	10/19/99	Granted	6,359,808	3/19/02	CHEN, TIEN-MIN AKAOGI, TAKAO N/E KURIHARA, KAZUHIRO (FUJITSU)	LOW VOLTAGE READ CASCADE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01002
12	09/421,775	10/19/99	Granted	6,327,181	12/4/01	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN AKAOGI, TAKAO N/E	REFERENCE CELL BITLINE PATH ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01003
13	09/421,774	10/19/99	Granted	6,163,478	12/19/00	KASA, YASUSHI (FJ) LAI, FAN W (CA)	COMMON FLASH INTERFACE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01005
14	09/650,401	8/29/00	Granted	6,275,412	8/14/01	KASA, YASUSHI (FJ) LAI, FAN W (CA)	COMMON FLASH INTERFACE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01005
15	09/632,390	8/4/00	Granted	6,397,313	5/28/02	KASA, YASUSHI (FJ) WANG, GUOWEI (EDDIE)	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY	AF01006
16	09/421,105	10/19/99	Granted	6,125,055	9/26/00	KASA, YASUSHI (FJ) WANG, GUOWEI (EDDIE)	SECTOR WRITE PROTECT CAMS FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Af01007
17	09/421,470	10/19/99	Granted	6,550,028	4/15/03	KUO, TIAO-HUA 22492 (CA) AKAOGI, TAKAO N/E LAI, FAN W (CA)	ARRAY VT MODE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01008
18	09/661,358	9/14/00	Granted	6,275,421	8/14/01	CHEN, TIEN-MIN KURIHARA, KAZUHIRO (FUJITSU)	CHIP ENABLE INPUT BUFFER	AF01009
19	09/663,765	9/18/00	Granted	6,463,516	10/8/02	LEONG, NANCY S. 22609 CHEN, JOHNNY CHUNG-LEE 75232 KUO, TIAO-HUA 22492 (CA) KURIHARA, KAZUHIRO (FUJITSU)	VARIABLE SECTOR SIZE FOR A HIGH DENSITY FLASH MEMORY DEVICE	AF01010
20	09/663,909	9/18/00	Granted	6,285,627	9/4/01	KURIHARA, KAZUHIRO (FUJITSU) SHIEH, THOMAS T	ADDRESS TRANSITION DETECTOR (ATD) ARCHITECTURE FOR HIGH DENSITY FLASH MEMORY DEVICE	AF01011
21	09/663,552	9/18/00	Granted	6,353,566	3/5/02	AKAOGI, TAKAO N/E KURIHARA, KAZUHIRO (FUJITSU) SHIEH, THOMAS T	SYSTEM & METHOD FOR TRACKING SENSING SPEED BY AN EQUALIZATION PULSE FOR A HIGH DENSITY FLASH MEMORY DEVICE	AF01012
22	09/712,382	11/13/00	Granted	6,297,993	10/2/01	CHEN, JOHNNY CHUNG-LEE 75232 KASA, YASUSHI (FJ) PHAM, TRUNG S	ACCELERATION VOLTAGE IMPLEMENTATION FOR HIGH DENSITY FLASH MEMORY DEVICE	AF01014
23	09/644,358	8/23/00	Granted	6,327,194	12/4/01	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN	PRECISE REFERENCE WORDLINE LOADING COMPENSATION FOR A HIGH DENSITY FLASH MEMORY DEVICE	AF01015

Attachment A

24	09/420,535	10/19/99	Granted	6,662,262	12/9/03	KASA, YASUSHI (FJ) CHEN, JOHNNY CHUNG-LEE 75232 WANG, GUOWEI (EDDIE) KUO, TIAO-HUA 22492 (CA)	OTP SECTOR DOUBLE PROTECTION FOR A SIMULTANEOUS OPERATION FLASH MEMORY	AF01016
25	09/421,758	10/19/99	Granted	6,571,307	5/27/03	KUO, TIAO-HUA 22492 (CA) LEONG, NANCY S. 22609 AKAOGI, TAKAO N/E KASA, YASUSHI (FJ)	MULTIPLE PURPOSE BUS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01018
26	09/421,757	10/19/99	Granted	6,331,950	12/18/01	KUO, TIAO-HUA 22492 (CA) KASA, YASUSHI (FJ) CHEN, JOHNNY CHUNG-LEE 75232	WRITE PROTECT INPUT IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01019
27	09/421,982	10/19/99	Granted	6,125,058	9/26/00	KUO, TIAO-HUA 22492 (CA) LEONG, NANCY S. 22609 AKAOGI, TAKAO N/E CHEN, JOHNNY CHUNG-LEE 75232	SYSTEM FOR OPTIMIZING THE EQUALIZATION PULSE OF A READ SENSESMPLIFIER FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01020
28	09/421,142	10/19/99	Granted	6,201,753	3/13/01	AKAOGI, TAKAO N/E KURIHARA, KAZUHIRO (FUJITSU)	LATCHING CAM DATA IN A FLASH MEMORY DEVICE	AF01023
29	09/421,984	10/19/99	Granted	6,185,128	2/6/01	AKAOGI, TAKAO N/E KURIHARA, KAZUHIRO (FUJITSU) CHEN, JOHNNY CHUNG-LEE 75232	REFERENCE CELL FOUR-WAY SWITCH FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01024
30	09/421,776	10/19/99	Granted	6,111,787	8/29/00	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN AKAOGI, TAKAO N/E	ADDRESS TRANSITION DETECT TIMING ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01025
31	09/547,556	4/12/00	Granted	6,208,556	3/27/01	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN AKAOGI, TAKAO N/E	ADDRESS TRANSITION DETECT TIMING ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01025
32	09/421,471	10/19/99	Granted	6,285,585	9/4/01	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN	OUTPUT SWITCHING IMPLEMENTATION FOR A FLASH MEMORY DEVICE	AF01026
33	09/422,199	10/19/99	Granted	6,118,698	9/12/00	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN AKAOGI, TAKAO N/E	OUTPUT MULTIPLEXING IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	AF01027
34	09/661,356	9/14/00	Granted	6,266,284	7/24/01	KURIHARA, KAZUHIRO (FUJITSU) CHEN, TIEN-MIN	OUTPUT BUFFER FOR EXTERNAL VOLTAGE	AF01028
35	09/676,902	10/2/00	Granted	6,310,805	10/30/01	KASA, YASUSHI (FJ) SHIEH, MING-HUEL	ARCHITECTURE FOR A DUAL-BANK PAGE MODE MEMORY WITH REDUNDANCY	AF01029
36	09/652,742	8/31/00	Granted	6,298,007	10/2/01	SANTURKAR, VIKRAM S KASA, YASUSHI (FJ)	METHOD AND APPARATUS FOR ELIMINATING FALSE DATA IN A PAGE MODE MEMORY DEVICE	AF01030

Attachment A

37	09/667,891	9/22/00	Granted	6,324,108	11/27/01	BILL, COLIN 16072 BAUTISTA JR., EDWARD V. 23672 YAMADA, SHIGEKAZU (FUJITSU)	APPLICATION OF EXTERNAL VOLTAGE DURING ARRAY VT TESTING	AF01032
38	09/668,100	9/22/00	Granted	6,438,041	8/20/02	YAMADA, SHIGEKAZU (FUJITSU) BILL, COLIN 16072	NEGATIVE VOLTAGE REGULATION	AF01033
39	09/680,344	10/5/00	Granted	6,400,638	6/4/02	YAMADA, SHIGEKAZU (FUJITSU) AKAOGI, TAKAO N/E BILL, COLIN 16072	WORDLINE DRIVER FOR FLASH MEMORY READ MODE	AF01036
40	09/724,675	11/28/00	Granted	6,622,003	9/16/03	YANO, MASARU N/E HOLLMER, SHANE C. 22154 (CA) CHUNG, MICHAEL S.C. 23278	MULTI SET BLOCK ERASE	AF01041
41	09/558,764	4/26/00	Granted	6,201,737	3/13/01	HOLLMER, SHANE C. 22154 (CA) KURIHARA, KAZUHIRO (FUJITSU)	APPARATUS AND METHOD TO CHARACTERIZE THE THRESHOLD DISTRIBUTION IN AN NROM VIRTUAL GROUND ARRAY	AF01042
42	09/689,036	10/12/00	Granted	6,373,742	4/16/02	KURIHARA, KAZUHIRO (FUJITSU) HOLLMER, SHANE C. 22154 (CA) CHEN, PAU-LING 15896	TWO SIDE DECODING OF A MEMORY ARRAY	AF01043
43	09/688,936	10/16/00	Granted	6,583,479	6/24/03	FASTOW, RICHARD 25087 HOLLMER, SHANE C. 22154 (CA) CHEN, PAU-LING 15896 VAN BUSKIRK, MICHAEL A, 020498 HIGASHITANI,	SIDEWALL NROM AND METHOD OF MANUFACTURE THEREOF FOR NON-VOLATILE MEMORY CELLS	AF01050
44	09/798,667	3/2/01	Granted	6,528,390	3/4/03	KOMORI, HIDEKI FOOTE, DAVID K. (T) 19324 (CA) WANG, FEI 63099 RANGARAJAN, BHARATH	PROCESS FOR FABRICATING A NON-VOLATILE MEMORY DEVICE	AF01057
45	09/810,155	3/16/01	Granted	6,573,140	6/3/03	OGURA, JUSUKE (FUJITSU) IZUMI, KIYOSHI (FUJITSU) YANO, MASARU N/E KOMORI, HIDEKI PHAM, TUAN DUC (T) 23353 (CA) HUI, ANGELA T. 21184 (CA)	PROCESS FOR MAKING A DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES	AF01063
46	09/809,969	3/16/01	Granted	6,713,809	3/30/04	OGURA, JUSUKE (FUJITSU) KURIHARA, KAZUHIRO (FUJITSU) YANO, MASARU N/E KOMORI, HIDEKI PHAM, TUAN DUC (T) 23353 (CA) HUI, ANGELA T. 21184 (CA)	DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES	AF01067
47	09/691,643	10/18/00	Granted	6,537,866	3/25/03	SHIELDS, JEFFREY 22523 PHAM, TUAN DUC (T) 23353 (CA) OGURA, JUSUKE (FUJITSU) RANGARAJAN, BHARATH CHAN, SIMON SIU-SING 22412	METHOD OF FORMING NARROW INSULATING SPACERS FOR USE IN REDUCING MINIMUM COMPONENT SIZE	AF01068

Attachment A

48	09/501,159	2/9/00	Granted	6,243,316	6/5/01	AKAOGI, TAKAO N/E AL-SHAMMA, ALI K. CLEVELAND, LEE 22191 KIM, YONG K. 23062 (CA) LIN, JIN-LIEN TEH, BOON-TANG (PNG)	IMPROVED VOLTAGE BOOST RESET CIRCUIT FOR A FLASH MEMORY	AF01071
49	09/595,519	6/16/00	Granted	6,351,420	2/26/02	AKAOGI, TAKAO N/E AL-SHAMMA, ALI K. CLEVELAND, LEE 22191 KIM, YONG K. 23062 (CA) LIN, JIN-LIEN TEH, BOON-TANG (PNG)	VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY	AF01072
50	09/690,554	10/17/00	Granted	6,347,052	2/12/02	AKAOGI, TAKAO N/E AL-SHAMMA, ALI K. KIM, YONG K. 23062 (CA) LIN, JIN-LIEN TEH, BOON-TANG (PNG) NGUYEN, KENDRA	WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY	AF01073
51	09/729,388	12/4/00	Granted	6,463,003	10/8/02	AL-SHAMMA, ALI K. AKAOGI, TAKAO N/E	POWER SAVING SCHEME FOR BURST MODE IMPLEMENTATION DURING READING OF DATA FROM A MEMORY DEVICE	AF01074
52	09/526,239	3/15/00	Granted	6,240,040	5/29/01	AKAOGI, TAKAO N/E CLEVELAND, LEE 22191 NGUYEN, KENDRA	MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY	AF01075
53	09/829,518	4/9/01	Granted	6,621,761	9/16/03	AKAOGI, TAKAO N/E CLEVELAND, LEE 22191 NGUYEN, KENDRA	BURST ARCHITECTURE FOR A FLASH MEMORY	AF01076
54	09/724,669	11/28/00	Granted	6,307,787	10/23/01	AL-SHAMMA, ALI K. AKAOGI, TAKAO N/E	BURST READ INCORPORATING OUPUT BASED REDUNDANCY	AF01078
55	09/698,614	10/27/00	Granted	6,507,527	1/14/03	CLEVELAND, LEE 22191 LIN, JIN-LIEN AKAOGI, TAKAO N/E AL-SHAMMA, ALI K. TEH, BOON-TANG (PNG) NGUYEN, KENDRA	MEMORY LINE DISCHARGE BEFORE SENSING	AF01080
56	09/638,055	8/11/00	Granted	6,229,735	5/8/01	AKAOGI, TAKAO N/E NGUYEN, KENDRA KIM, YONG K. 23062 (CA) CLEVELAND, LEE 22191	BURST READ WORDLINE BOOSTING	AF01081
57	09/675,372	9/29/00	Granted	6,400,633	6/4/02	AL-SHAMMA, ALI K. AKAOGI, TAKAO N/E CLEVELAND, LEE 22191	POWER-SAVING MODES FOR MEMORIES	AF01083
58	10/061,620	2/1/02	Granted	6,611,473	8/26/03	AL-SHAMMA, ALI K. AKAOGI, TAKAO N/E CLEVELAND, LEE 22191	POWER-SAVING MODES FOR MEMORIES	AF01083
59	09/490,340	1/24/00	Granted	6,212,108	4/3/01	AKAOGI, TAKAO N/E CLEVELAND, LEE 22191	DISTRIBUTED VOLTAGE CHARGE CIRCUITS TO REDUCE SENSING TIME IN A MEMORY DEVICE	AF01084

Attachment A

60	10/243,433	9/12/02	Granted	6,728,160	4/27/04	YANG, TIEN-CHUN KURIHARA, KAZUHIRO (FUJITSU) CHEN, PAU-LING 15696	PATH GATE DRIVER CIRCUIT	AF01167
61	09/166,385	10/5/98	Granted	6,134,146	10/17/00	BILL, COLIN 16072 SU, JONATHAN 22917 AKAOGI, TAKAO N/E GUTALA, RAVI P. 21656 (T)	WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)	C715497
62	09/419,695	10/14/99	Granted	6,147,908	11/14/00	BILL, COLIN 16072 YAMADA, SHIGEKAZU (FUJITSU)	METHOD AND SYSTEM FOR SAVING OVERHEAD PROGRAM TIME IN A MEMORY DEVICE	E0248

ASSIGNMENT AGREEMENT

This Assignment Agreement by and between **AMD INVESTMENTS, INC.**, a corporation of Delaware having a place of business at One AMD Place, P. O. Box 3453, Sunnyvale, California 94088-3453, U.S.A. and **Fujitsu Limited**, a Japanese corporation (hereinafter collectively referred to as "ASSIGNORS") and **FASL LLC**, a limited liability company of Delaware, having a place of business at One AMD Place, P. O. Box 3453, Sunnyvale, California, 94088-3453, U.S.A. (hereinafter "ASSIGNEE") is effective on the 30TH day of June, 2003.

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, ASSIGNORS hereby assign, transfer and convey all of their right, title and interest in the United States and throughout the world in and to all invention disclosures, United States patent applications, United States patents, foreign patents, and foreign patent applications (including any Patent Cooperation Treaty (PCT) applications) identified on Schedule A attached hereto and made a part hereof, and the entire right, title and interest in the United States and throughout the world in and to the inventions to which said invention disclosures, patents and patent applications pertain, in and to all worldwide rights of priority, and in and to any corresponding United States and foreign patents, extensions and renewals of patents, results of reexamination, substitutions, reissues, patent applications, divisionals, continuations, continuations-in-part, utility models, petty patents, patents of importation, invention registrations, and inventor's certificates, together with all the rights and privileges granted and secured by said patents, extensions and renewals of patents, results of reexamination, substitutions, reissues, patent applications, divisionals, continuations, continuations-in-part, utility models, petty patents, patents of importation, invention registrations and inventor's certificates, including without limitation all claims, demands, rights and causes of action that ASSIGNORS may have against others on account of any past, present and future infringement of any of said patents, patent applications, utility models, petty patents, patents of importation, invention registrations, and inventor's certificates with the right in ASSIGNEE to sue for and obtain all relief to which ASSIGNORS may have been entitled by reason of any such infringement. ASSIGNORS further agree that ASSIGNEE may apply for and receive Letters Patent, utility models, petty patents, patents of importation, invention registrations, and inventor's certificates for said inventions in its own name.

Said entire right, title, and interest is to be held and enjoyed by ASSIGNEE for its own use and benefit and for the use and benefit of its successors and assigns, to the full end of the term for which said patents, registrations or certificates may be granted, as fully and

entirely as the same would have been held and enjoyed by ASSIGNORS had this assignment and sale not been made.

ASSIGNORS
AMD INVESTMENT, INC.

By: Thomas M. McCoy Date May 5, 2004
Name: Thomas M. McCoy
Title: Vice President and Secretary

State of **CALIFORNIA**)
County of **SANTA CLARA**)

On May 5, 2004, before me, Peg A O'Malley, a Notary Public, personally appeared Thomas M. McCoy, personally known to me ~~or proved to me on the basis of satisfactory evidence~~ to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

PEG A. O'MALLEY
Commission # 1279250
Notary Public - California
Santa Clara County
My Comm. Expires Oct 30, 2004

Witness my hand and official seal.

Peg A. O'Malley
SIGNATURE OF NOTARY

ASSIGNORS
FUJITSU, INC.

By: 黒川博昭 Date: May 25, 2004
Name: Hiroaki Kurokawa
Title: President and Representative Director

藤田正美 Date: May 25, 2004
Name: Masami Fujita
Witness for Hiroaki Kurokawa

西川陽子 Date: May 25, 2004
Name: Toyoko Nishikawa
Witness for Hiroaki Kurokawa

ASSIGNEE
FASL LLC

By: Hollis O'Brien Date: June 3, 2004
Name: Hollis M. O'Brien
Title: Assistant Secretary

State of **CALIFORNIA**)
County of **SANTA CLARA**)

On June 3, 2004, before me, M. Pacheco, a Notary Public, personally appeared Hollis M. O'Brien, pereonally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that ~~he~~/she executed the same in ~~his~~/her authorized capacity, and that by ~~his~~/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Witness my hand and official seal.

M. PACHECO
Commission # 1428556
Notary Public - California
Santa Clara County
My Comm. Expires Jul 30, 2007

M Pacheco
SIGNATURE OF NOTARY