PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Brecis Communications Corporation	08/15/2004

RECEIVING PARTY DATA

Name:	PMC-Sierra, Inc.
Street Address:	3975 Freedom Circle
Internal Address:	Attention: President
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 14

Property Type	Number
Patent Number:	5923894
Patent Number:	5940626
Patent Number:	6016539
Patent Number:	6067601
Patent Number:	6178482
Patent Number:	6308254
Patent Number:	6327632
Patent Number:	6438679
Patent Number:	6677786
Patent Number:	6505291
Patent Number:	6216218
Application Number:	10086953
Application Number:	10301369
Application Number:	10262464

OP $560.00 5923894

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Patricia A. Conner

Total Attachments: 4
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PATENT AND PATENT APPLICATION ASSIGNMENT

This Patent and Patent Application Assignment (this "Assignment") is made as of August 15, 2004 by and between Brecis Communications Corporation, a California corporation ("Assignor") and PMC-Sierra, Inc., a Delaware corporation ("Assignee").

RECITALS

A. Assignor and Assignee have entered into an Asset Purchase Agreement dated as of August 15, 2004. All capitalized terms used herein but not otherwise defined shall have the meanings set forth in the Asset Purchase Agreement.

B. Assignor has filed with the United States Patent and Trademark Office the patents and patent applications set forth on Exhibit A hereto (the "Patents").

C. Pursuant to the Asset Purchase Agreement, Assignor desires to assign to Assignee all of Assignor's right, title and interest in and to the Patents.

ASSIGNMENT

NOW, THEREFORE, in consideration of the foregoing premises, the mutual covenants and agreements contained in the Asset Purchase Agreement and the covenants and agreements in this Assignment and to induce Assignee to consummate the transactions contemplated by the Asset Purchase Agreement, Assignor agrees as follows:

1. Assignor does hereby sell, transfer, convey, assign and deliver to Assignee all of Assignor's right, title and interest in and to the Patents and any patents that may issue therefrom, including any foreign counterparts, provisional applications, non-provisional applications, divisionals, continuations, continuations-in-part, reissues, reexaminations, national phase applications, including petty patent applications, and utility model applications of such patents, and extensions or derivations thereof, both foreign and domestic, that may issue thereon, the same to be held by Assignee for Assignee's own use and enjoyment, and for the use and enjoyment of Assignee's successors, assigns and other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor if this Assignment and sale had not been made; together with all claims for damages and other remedies by reason of past infringements of the Patents, along with the right to sue for and collect such damages and other remedies for the use and benefit of Assignee and its successors, assigns and other legal representatives.

2. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States, and, in the case of any Patents filed with any office of any country or countries foreign to the United States, any officer of such country whose duty it is to issue patents or other evidence or forms of intellectual property protection or applications as aforesaid, to issue the same to Assignee and its successors, assigns and other legal representatives in accordance with the terms of this instrument.

3. Assignor conveys to the Assignee the right to make application in its own behalf for protection of the Patents in the U.S. and countries foreign to the U.S. and to claim under the Patent Cooperation Treaty, the International Convention and/or other international arrangement for any such application the date of any earlier U.S. application (or any other application of the invention) to gain priority with respect to other applications.

IN WITNESS WHEREOF, Assignor has executed this Assignment on the date first above written.

Brecis Communications Corporation. ("ASSIGNOR")

By: _____

Name: George Alexy

Title: President and Chief Executive Officer

Acknowledgment by Notary Public

State of California

County of Santa Clara

On this 15th day of August, 2004, before me, the undersigned Notary Public, personally appeared George Alexy, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument, and acknowledged to me that he or she executed the same.

Seal:

Signature: _____

Name: Catherine Tenner, Notary Public

Ryan CRT

CATHERINE RYAN TENNER
Commission # 1305009
Notary Public - California
Santa Clara County
My Comm. Expires May 19, 2005

PATENT ASSIGNMENT SIGNATURE PAGE

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EXHIBIT A
PATENTS

File Date or Application Date	Date of Patent	Patent No.	Application No. or International Application No.	Publication or International Publication No. and Date	Inventor	Assignee	Title
11/3/97	7/13/99	US 5,923,894	08/963,346	---	Donald L.Sollars	TeraGen Corporation ("TeraGen")	Adaptable Input/Output Pin Control
11/3/97	8/17/99	US 5,940,626	08/963,387	---	Donald L. Sollars	TeraGen	Processor having an Instruction Set Architecture Implemented with Hierarchically Organized Primitive Operations
11/3/97	1/18/00	US 6,016,539	08/963,345	---	Donald L. Sollars	TeraGen	Data Path Control Logic for Processors Having Instruction Set Architectures Implemented with Hierarchically Organized Primitive Operations
11/3/97	5/23/00	US 6,067,601	08/963,389	---	Donald L. Sollars	Brecis Communications Corporation ("Brecis")	Cache Memory Based Instruction Execution
11/3/97	1/23/01	US 6,178,482 B1	08/963,391	---	Donald L. Sollars	Brecis	Virtual Register Sets
11/18/99	10/23/01	US 6,308,254 B1	09/442,848	---	Donald L. Sollars	Brecis	Processing Instructions of an Instruction Set Architecture by Executing Hierarchically Organized Snippets of Atomic Units of Primitive Operations
1/14/99	12/4/01	US 6,327,632 B1	09/231,942	---	Donald L. Sollars	Brecis	Adaptable I/O Pins Manifesting I/O Characteristics Responsive to Bit Values Stored in Selected Addressable Storage Locations, Each Pin Coupled to Three Corresponding Addressable Storage Locations

File Date or Application Date	Date of Patent	Patent No.	Application No. or International Application No.	Publication or International Publication No. and Date	Inventor	Assignee	Title
7/21/98	8/20/02	US 6,438,679 B1	09/120,043	---	Donald L. Sollars	Brecis	Multiple ISA Support by a Processor Using Primitive Operations
2/28/02	1/13/04	US 6,677,786 B2	10/086,500	---	Tore L. Kellgren	Brecis	Multi-Service Processor Clocking System
10/26/00	1/7/03	US 6,505,291 B1	09/697,911	---	Donald L. Sollars	Brecis	Processor Having a Datapath and Control Logic Constituted with Basic Execution Blocks
7/21/98	4/10/01	US 6,216,218 B1	09/120,041	---	Donald L. Sollars	None.	Processor Having a Datapath and Control Logic Constituted with Basic Execution Blocks
2/28/02	---	---	10/086,953	US 2002/0159474 A1, dated 10/31/02	George Apostol Jr., Mahadev S. Kolluru, Tom Vu	None.	On-Chip Inter-Subsystem Communication Including Concurrent Data Traffic Routing
11/20/02	---	---	10/301,369	US 2004/0098530, dated 5/20/04	Jeffrey S. Earl, George Apostol Jr., Douglas A. Cross	None.	Flexible Data Transfer to and from External Devices of System-On-Chip
9/30/02	---	---	10/262,464	US 2004/0062260 A1, dated 4.1.04	Anthony E. Raetz, Yanghua Liu	None.	Multi-Level Jitter Control