FORM PTO-1595
(Rev. 5-95)

RECORDATION FORM COVER SHEET

U.S. DEPARTMENT OF COMMERCE
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PATENTS ONLY

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

4198638 CANADA INC

Additional names of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Name: RICHARD S. NORMAN

Internal Address: 1877 chemin Poissant, Sutton, Quebec, Canada, J0E 2K0

Street Address:

SAME AS ABOVE

City: _____ State _____ ZIP _____

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☐ Other _____

Execution Date: October 14, 2004

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is: _____

A. Patent Application No

09/376,194	10/324,110	08/323,580	10/023,478
09/679,168	10/323,896	10/000,813	10/022,851
08/618,397	10/368,003	10/022,856	10/458,734
10/324,071	09/144,695	10/022,852	

B. Patent No.(s)

Additional numbers attached ? ☐ Yes ☒No

5. Name and address of party to whom correspondence concerning document should be mailed:

CUSTOMER NUMBER 020988

Tel. (514) 847-4462

Attorney Docket No.: 17272-GEN CMB/clb

6. Total number of application and patents involved: 1

7. Total fee (37 CFR 3.41): ..... $ 600.00

☒ Enclosed

☒ Any deficiencies in enclosed fees are authorized to be charged to deposit account

8. Deposit account number: 19-5113

(Attach duplicate copy of this page if paying by deposit account)

CH $600.00 19513 09376194

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9. Statement and signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

C. Marc Benoît, Reg. No. 50,200
Name of Person Signing

Signature

November 23, 2004
Date

Total number of pages comprising cover sheet: 1

Mail documents to be recorded with required cover sheet information to: Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

Assignment - World

ASSIGNMENT

WHEREAS,

4198638 Canada Inc.

hereinafter referred to as Assignor, whose full post office address is,

4028 Marlowe, Montreal, Quebec, H4A 3M2

is the owner of the Intellectual Property as fully set forth and described in the Letters Patents and Patent Applications listed on Schedule A hereto attached,

hereinafter referred to as The Invention(s);

AND WHEREAS,

Richard S. Norman

hereinafter referred to as Assignee, whose full post office address is,

1877 chemin Poissant, Sutton, QC J0E 2K0

desires to acquire Assignor's entire right, title and interest in and to The Invention(s);

NOW THEREFORE, in consideration of the sum of One Dollar ($1.00) and other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and set over to Assignee, its successors, assigns, or legal representatives, its entire right, title and interest for Canada, the United States and all other countries throughout the World in and to The Invention(s), together with its entire right, title and interest to any and all Letters Patent that have issued or may issue for The Invention(s), including any and all divisions, reissues, continuations and extensions of The Invention(s), to the full end of the term for which each said Letters Patent may be granted, and including any right to claim priority based on The Invention(s), and including the right to bring suit and recover damages for past infringement, the same to be held and enjoyed as fully and completely as the same would have been held and enjoyed by Assignor had this Assignment not been made;

AND ASSIGNOR, on behalf of itself and its executors and administrators, does hereby covenant and agree to do all such lawful acts and things and to execute without further consideration such further lawful assignments, documents, assurances, applications and other instruments as may reasonably be required by said Assignee, its successors, assigns, or legal representatives, to obtain any and all Letters Patent for The Invention and vest the same in said Assignee, its successors, assigns, or legal representatives.

THE PARTIES agree to this Assignment being drawn up in the English language.

Assignor	**Witness**
Frances Layden *Per* 4198638 CANADA INC.	*Name*
Signature Layden	*Signature*
Date October 19, 2004	*Date* October 19, 2004

SCHEDULE A

Inventor (1)	Category	File Number	Application number	Description	Status	Filing Date
				LARGE AREA (LA) IC – DEFECT TOLERANCE		
Richard Norman	LAIC-DT	P(CA)1996-002 P(JP)1996-004 P(KR)1996-005 P(US)1999-009 P(US)2000-116	2,185,787 7-524267 705245/96 US 09/376,194 – US 09/679,168–		Pending Pending Issued Issued Issued	
Richard Norman	LAIC-DT	P(EP)1996-003	95912116.1	Defect Tolerance with Use of Unassigned Spare Cells	Issued	22/03/1995
Richard Norman	LAIC-DT	P(US)1996-001	US 08/618,397 –	Direct Replacement Cell Fault Tolerance	Issued	22/03/1995
Richard Norman	LAIC-DT	P(US)2002-124	US 10/330,069	Array of Discrete Modules Fabricated on a Wafer	Allowed	30/12/2002
Richard Norman, et al.	LAIC-DT	P(US)2002-133	US10/324,071 –	Bus For Parallel Processing System	Pending	20/12/2002
Yvon Savaria, et al.	LAIC-DT	P(US)2002-134	US 10/324,110 –	Large Scale Signal Paths in Parallel Processing System	Pending	20/12/2002
Yvon Savaria, et al.	LAIC-DT	P(US)2002-135	US 10/323,896–	Fault Tolerant Scan Chain for a Parallel Processing System	Pending	20/12/2002
Richard Norman	LAIC-DT	P(US)2003-001	US10/368,003 –	Fault Tolerant Cell Array Architecture	Pending	19/02/2003
				LA IC – INTER-RETICLE STITCHING		
Richard Norman	LAIC/IRS	P(US)1998-004	US 09/144,695 –	Integrated Circuit Having Lithographic Array Interconnections	Issued	01/09/1998
Richard Norman, et al.	LAIC-IRS	P(US)2002-131	US 10/330,068	Wave-Front Clock Synchronization	Pending	30/12/2002
Richard Norman, et al.	LAIC-IRS	P(US)2003-011	US 10/462,283	Bus Architecture with Efficient Use of Integrated Circuit Area	Pending	17/06/2003
				LA IC – INPUT/OUTPUT		
Richard Norman	LAIC-I/O	P(US)1994-002	US 08/323,580–	Massively-Parallel Array with Outputs from Individual Processors	Issued	17/10/1994
Richard Norman	LAIC-I/O	P(EP)1999-013 P(GB)2003-003	00110048.6 00110048.6	Massively Parallel System w/ Photovoltaic Cells Display Architecture with Integrated Power Supply	Issued Validated	22/03/1995
Richard Norman	LAIC-I/O	P(US)2001-183	US 10/000,813 –	Output and/or Input Coordinated Processing Array	Issued	30/11/2001

SCHEDULE A

Inventor (1)	Category	File Number	Application number	Description	Status	Filing Date
				LA IC – SIGNAL INTEGRITY		
Karl Fecteau, et al. Yvon Savaria, et al. Claude Thibeault et al.	LAIC-SI	P(US)2001-199 P(US)2001-200 P(US)2001-201 P(US)2001-019	US 10/022,856 - US 10/022,852 - US 10/023,478 - US 10/022,851 -	Method for Reducing Interference on Nearby Conductors	Pending Allowed Pending Pending	20/12/2001 30/12/2002
Richard Norman	LAIC-SI	P(US)2002-130	US 10/330,230	Reference Wires for an Electrical Bus	Pending	19/12/2003
Richard Norman	LAIC-SI	P(US)2003-016	US 10/739,047	Conductive Fabric with Balanced Mutual Interference		
				LA IC – MECHANICAL/PACKAGING		
Richard Norman	LAIC-Mech	P(US)2002-125	US 10/330,231	High-Performance Interconnect for Discrete Modules	Pending	30/12/2002
Richard Norman	LAIC-Mech	P(US)2002-126	US 10/330,232	Connector Between Contact Pads on Two Surfaces	Pending	30/12/2002
Richard Norman, et al.	LAIC-Mech	P(US)2002-127	US 10/330,234	Reduced Thermal Expansion Effects	Pending	30/12/2002
Richard Norman	LAIC-Mech	P(US)2002-128	US 10/330,067	Defect Tolerant Method of Mounting Chip to Substrate	Pending	30/12/2002
Richard Norman	LAIC-Mech	P(US)2002-129	US 10/330,23	Compound Semiconductor Structure	Pending	30/12/2002
Richard Norman	LAIC-Mech	P(US)2002-132	US 10/330,319	Architecture for a Microelectronic Complex on a Planar Body	Pending	11/06/2003
Richard Norman	LAIC-Mech	P(US)2003-008	US 10/458,734	Method for Continuous Linear Production of Integrated Circuits	Pending	27/06/2003
Richard Norman, et al.	LAIC-Mech	P(US)2003-009	US 10/606,886	Flexible Device for Interfacing with a Wafer	Pending	03/10/2003
Richard Norman	LAIC-Mech	P(US)2003-012		Connectors with Fault Tolerance	Pending	03/10/2003
Richard Norman	LAIC-Mech	P(US)2003-013	US 10/677,292	Cooling Multiple Discrete Functional Modules		