PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Advanced Technology Materials, Inc.	09/10/2004

RECEIVING PARTY DATA

Name:	Emosyn America, Inc.
Street Address:	1171 Sonora Court
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94086

PROPERTY NUMBERS Total: 46

Property Type	Number
Application Number:	09809897
Application Number:	09394757
Application Number:	10376682
Application Number:	10238757
Application Number:	10339218
Application Number:	10338551
Application Number:	10340342
Application Number:	10339223
Application Number:	60436702
Application Number:	10378413
Application Number:	10378414
Application Number:	10448944
Application Number:	09840447
Application Number:	09109168
Application Number:	09764683

CH $1840.00 09809897

Patent Number:	6223144
Patent Number:	6157979
Patent Number:	6108236
Patent Number:	6173419
Patent Number:	6145020
Patent Number:	6400603
Patent Number:	6510081
Patent Number:	6292874
Patent Number:	6219291
Patent Number:	6466488
Patent Number:	6421213
Patent Number:	6691055
Patent Number:	6639428
PCT Number:	US9906226
PCT Number:	US9905419
PCT Number:	US9910123
PCT Number:	US0113581
PCT Number:	US0041243
PCT Number:	US0113408
PCT Number:	US0108153
PCT Number:	US0239998
PCT Number:	US0208215
PCT Number:	US0040782
PCT Number:	US0328104
PCT Number:	US0341590
PCT Number:	US0341594
PCT Number:	US0341581
PCT Number:	US0341592
PCT Number:	US0340792
PCT Number:	US0406202
PCT Number:	US0415310

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Edward B. Weller

Total Attachments: 11
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PATENT / PATENT APPLICATION ASSIGNMENT OFGS File Nos.:

WHEREAS, Advanced Technology Materials, Inc., a corporation organized and existing under the laws of Delaware and having a principal place of business at 7 Commerce Drive, Danbury, Connecticut, United States of America, (hereinafter referred to as "ASSIGNOR"), is the owner of a United States Patent and applications for United States Letters Patents, PCT Patent Applications, and various international patent(s) and/or applications for international patents set forth in the SCHEDULE annexed hereto; and

WHEREAS, Emosyn America, Inc., a corporation organized and existing under the laws of the State of Delaware (hereinafter referred to as "ASSIGNEE"), is desirous of acquiring all right, title and interest in said applications for patent (set forth in the SCHEDULE), the inventions set forth therein (and any patent that may be granted therefore).

NOW, THEREFORE, in consideration of One Dollar ($1.00) and other good and valuable consideration, the receipt of which is hereby acknowledged, ASSIGNOR does hereby sell, assign and set over to said ASSIGNEE the entire right, title and interest for the United States and all other countries in and the aforesaid patent and applications for patent.

[Signature follows next page]

IN WITNESS WHEREOF, the undersigned has signed this Patent Assignment as of the date stated below.

Advanced Technology Materials, Inc.

Date: September ___, 2004

By: _____
Name: Eugene G. Banucci, Ph.D.
Title: Chief Executive Officer

SCHEDULE

PATENT SCHEDULE

Granted U.S. Patents

No.	Country	Title	Patent No. or Publication No.	Application No.
1	US	METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS	6,223,144	09/047,809
2	PCT	METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS		PCT/US99/06226
3	Europe; DE, FR, GB, IT, NL	METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS		99914031.2
4	US	PROGRAMMABLE CONTROLLING DEVICE WITH NON-VOLATILE FERROELECTRIC STATE-MACHINES FOR RESTARTING PROCESSOR WHEN POWER IS RESTORED WITH EXECUTION STATES RETAINED IN SAID NON-VOLATILE STATE-MACHINES ON POWER DOWN	6,157,979	09/039,299
5	PCT	FERROELECTRIC MEMORY FOR A PROGRAMMABLE CONTROLLING DEVICE		PCT/US99/05419
6	US	SMART CARD COMPRISING INTEGRATED CIRCUITRY INCLUDING EPROM AND ERROR CHECK AND CORRECTION SYSTEM	6,108,236	09/118,736
7	Europe	A SINGLE CHIP EMBEDDED MICROCONTROLLER WITH FLASH EPROM AND ERROR CHECK AND CORRECTION SYSTEM	0973095	99113937.9
8	US	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE	6,173,419	09/078,872
9	PCT	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		PCT/US99/10123
10	Europe	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE	1029275	99920408.4
11	US	MICROCONTROLLER INCORPORATING AN ENHANCED PERIPHERAL CONTROLLER FOR AUTOMATIC UPDATING THE CONFIGURATION DATA OF MULTIPLE PERIPHERALS BY USING A FERROELECTRIC MEMORY ARRAY	6,145,020	09/078,952

PATENT
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PATENT SCHEDULE

No.	Country	Title	Patent No. or Publication No.	Application No.
12	US	ELECTRONICALLY-ERASEABLE PROGRAMMABLE READ-ONLY MEMORY HAVING REDUCED-PAGE-SIZE PROGRAM AND ERASE	6,400,603	09/564,324
13	PCT	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		PCT/US01/13581
14	Australia	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		2001255732
15	Brazil	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		0110585-0
16	Canada	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		2407888
17	Europe	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE	1305805	01928930.5
18	Israel	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		152577
19	Japan	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE	2003532968	2001581285
20	Korea	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		10-2002-7014751
21	New Zealand	FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE		522383
22	US	Electronically-eraseable programmable read-only memory having reduced-page-size program and erase	6,510,081	10/022,314
23	US	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES	6,292,874	09/420,318
24	PCT	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES		PCT/US00/41243

PATENT SCHEDULE

No.	Country	Title	Patent No. or Publication No.	Application No.
25	Australia	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES	771129	21137/01
26	Canada	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES		2387807
27	Europe	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES	1242891	00984535.5
28	Israel	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES		149157
29	Japan	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES	2003-523554	2001532399
30	Korea	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES		10-2002-7005035
31	New Zealand	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES	518400	

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PATENT SCHEDULE

No.	Country	Title	Patent No. or Publication No.	Application No.
32	Singapore	MEMORY MANAGEMENT METHOD AND APPARATUS FOR PARTITIONING HOMOGENEOUS MEMORY AND RESTRICTING ACCESS OF INSTALLED APPLICATIONS TO PREDETERMINED MEMORY RANGES		200202179-8
33	US	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL	6,219,291	09/561,710
34	PCT	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL		PCT/US01/13408
35	Europe	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL	1287530	01928883.6
36	Japan	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL	2003532967	2001581283
37	Korea	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL		10-2002-7014703
38	US	REDUCTION OF DATA DEPENDENT POWER SUPPLY NOISE WHEN SENSING THE STATE OF A MEMORY CELL	6,466,488	09/802,184
39	US	METHOD AND APPARATUS FOR DETECTING A TAMPER CONDITION AND ISOLATING A CIRCUIT THEREFROM	6,421,213	09/531,131
40	PCT	METHOD AND APPARATUS FOR DETECTING A TAMPER CONDITION AND ISOLATING A CIRCUIT THEREFROM		PCT/US01/08153
41	Europe	METHOD AND APPARATUS FOR DETECTING A TAMPER CONDITION AND ISOLATING A CIRCUIT THEREFROM	1281091	01922385.8
42	US	INTEGRATED CIRCUIT PROVIDED WITH MEANS FOR CALIBRATING AN ELECTRONIC MODULE AND METHOD FOR CALIBRATING AN ELECTRONIC MODULE OF AN INTEGRATED CIRCUIT	6,691,055	09/742,861

PATENT
REEL: 015503 FRAME: 0032

PATENT SCHEDULE

No.	Country	Title	Patent No. or Publication No.	Application No.
43	Europe	INTEGRATED CIRCUIT PROVIDED WITH MEANS FOR CALIBRATING AN ELECTRONIC MODULE AND METHOD FOR CALIBRATING AN ELECTRONIC MODULE OF AN INTEGRATED CIRCUIT	1111508	
44	Japan	INTEGRATED CIRCUIT PROVIDED WITH MEANS FOR CALIBRATING AN ELECTRONIC MODULE AND METHOD FOR CALIBRATING AN ELECTRONIC MODULE OF AN INTEGRATED CIRCUIT	20011235517	2000000390048
45	US	METHOD AND SYSTEM FOR DYNAMICALLY CLOCKING DIGITAL SYSTEMS BASED ON POWER USAGE	6,639,428	10/027,665
46	PCT	METHOD AND SYSTEM FOR DYNAMICALLY CLOCKING DIGITAL SYSTEMS BASED ON POWER USAGE	WO 03/054674	PCT/US02/39998

PATENT
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Pending U.S. Applications

No.	Country	Title	Patent No.or Publication No.	Application No.
47	US	ON-CHIP METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR CIRCUITS	20020133771	09/809,897
48	PCT	ON-CHIP METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR CIRCUITS		PCT/US02/08215
49	Europe	ON-CHIP METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR CIRCUITS	1378080	02715144.8
50	US	SINGLE CHIP EMBEDDED MICROCONTROLLER HAVING MULTIPLE NON-VOLATILE ERASABLE PROMS SHARING A SINGLE HIGH VOLTAGE GENERATOR		09/394,757
51	PCT	SINGLE CHIP EMBEDDED MICROCONTROLLER HAVING MULTIPLE NON-VOLATILE ERASABLE PROMS SHARING A SINGLE HIGH VOLTAGE GENERATOR		PCT/US00/40782
52	Europe	SINGLE CHIP EMBEDDED MICROCONTROLLER HAVING MULTIPLE NON-VOLATILE ERASABLE PROMS SHARING A SINGLE HIGH VOLTAGE GENERATOR	1242889	00982591.0
53	US	SINGLE CHIP EMBEDDED MICROCONTROLLER HAVING MULTIPLE NON-VOLATILE ERASABLE PROMS SHARING A SINGLE HIGH VOLTAGE GENERATOR	20030145154	10/376,682
54	US	PROGRAMMABLE SERIAL INTERFACE FOR A SEMICONDUCTOR CIRCUIT	20040049623	10/238,757
55	PCT	PROGRAMMABLE SERIAL INTERFACE FOR A SEMICONDUCTOR CIRCUIT		PCT/US03/28104
56	US	METHOD AND APPARATUS FOR DETECTING AN UNUSED STATE IN A SEMICONDUCTOR CIRCUIT		10/339,218
57	PCT	METHOD AND APPARATUS FOR DETECTING AN UNUSED STATE IN A SEMICONDUCTOR CIRCUIT		PCT/US03/41590
58	US	METHOD AND APPARATUS FOR AVOIDING GATED DIODE BREAKDOWN IN TRANSISTOR CIRCUITS		10/338,551
59	PCT	METHOD AND APPARATUS FOR AVOIDING GATED DIODE BREAKDOWN IN TRANSISTOR CIRCUITS		PCT/US03/41594
60	US	METHOD AND APPARATUS FOR EMULATING AN ELECTRICALLY ERASABLE PROGAM-MABLE READ ONLY MEMORY (EEPROM) USING NON-VOLATILE FLOATING GATE MEMORY CELLS		10/340,342

No.	Country	Title	Patent No. or Publication No.	Application No.
61	PCT	METHOD AND APPARATUS FOR EMULATING AN ELECTRICALLY ERASABLE PROGAM-MABLE READ ONLY MEMORY (EEPROM) USING NON-VOLATILE FLOATING GATE MEMORY CELLS		PCT/US03/41581
62	Malaysia	METHOD AND APPARATUS FOR EMULATING AN ELECTRICALLY ERASABLE PROGAM-MABLE READ ONLY MEMORY (EEPROM) USING NON-VOLATILE FLOATING GATE MEMORY CELLS		PI20040015
63	Taiwan	METHOD AND APPARATUS FOR EMULATING AN ELECTRICALLY ERASABLE PROGAM-MABLE READ ONLY MEMORY (EEPROM) USING NON-VOLATILE FLOATING GATE MEMORY CELLS		093100538
64	US	METHOD AND APPARATUS FOR INITIALIZING A SEMICONDUCTOR CIRCUIT FROM AN EXTERNAL INTERFACE		10/339,223
65	PCT	METHOD AND APPARATUS FOR INITIALIZING A SEMICONDUCTOR CIRCUIT FROM AN EXTERNAL INTERFACE		PCT/US03/41592
66	US	TRANSISTOR CIRCUITS FOR SWITCHING HIGH VOLTAGES AND CURRENTS WITHOUT CAUSING SNAPBACK OR BREAKDOWN		60/436,702
67	US	SWITCHING TRANSISTOR CIRCUITS TRANSISTOR CIRCUITS FOR SWITCHING HIGH VOLTAGES AND CURRENTS WITHOUT CAUSING SNAPBACK OR BREAKDOWN		10/378,413
68	PCT	SWITCHING TRANSISTOR CIRCUITS TRANSISTOR CIRCUITS FOR SWITCHING HIGH VOLTAGES AND CURRENTS WITHOUT CAUSING SNAPBACK OR BREAKDOWN		PCT/US03/40792
69	US	METHOD AND APPARATUS FOR DETECTING EXPOSURE OF A SEMICONDUCTOR CIRCUIT TO ULTRA-VIOLET LIGHT		10/378,414
70	PCT	METHOD AND APPARATUS FOR DETECTING EXPOSURE OF A SEMICONDUCTOR CIRCUIT TO ULTRA-VIOLET LIGHT		PCT/US04/06202
71	US	METHOD AND APPARATUS FOR MULTI-MODE OPERATION IN A SEMICONDUCTOR CIRCUIT		10/448,944

No.	Country	Title	Patent No. or Publication No.	Application No.
72	PCT	METHOD AND APPARATUS FOR MULTI-MODE OPERATION IN A SEMICONDUCTOR CIRCUIT		Not available
73	US	METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS		09/840,447
74	US	MICROPROCESSOR AND DISASSOCIATED SPECIAL CO-PROCESSOR ON A SINGLE IC		09/109,168
75	US	METHOD FOR TESTING AN INTEGRATED CIRCUIT INCLUDING HARDWARE AND/OR SOFTWARE PARTS HAVING A CONFIDENTIAL NATURE	20011001080	09/764,683
76	Europe	METHOD FOR TESTING AN INTEGRATED CIRCUIT INCLUDING HARDWARE AND/OR SOFTWARE PARTS HAVING A CONFIDENTIAL NATURE	1120662	2000000101502
77	Japan	METHOD FOR TESTING AN INTEGRATED CIRCUIT INCLUDING HARDWARE AND/OR SOFTWARE PARTS HAVING A CONFIDENTIAL NATURE	2001264396	