	11-17-20	04 —	Docket No.: 866	54-M (page 1 of 4)
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☐ Security Agreement ☐	Change of Name	City: Montreal	State/Pro	v.: Quebec
Other		Country: CANAD	<u>A</u> Z	ZIP: H4A 3M2
Execution Date: October 14, 2004		Additional name(s) &	address(es)	☐ Yes ☒ No
4. Application number(s) or patent number If this document is being filed together	` ,	the execution date	of the application i	s:
Patent Application No. Filing	date	B. Patent	No.(s)	
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Name: Stephan P. Georgiev		7. Total fee (37 Cl	FR 3.41):	\$ 520.00
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Stephan P. Georgiev, Reg. No. 37,563

Name of Person Signing 11/16/2004 DBYRNE 00000148 10330069

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**PATENT** 

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November 11, 2004

Date

	PE	Docket	t No.: 86654-M (page 2 of 4)
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4. Application number(s) or pate If this document is being filed Patent Application No.  10/330,231 10/330,232 10/330,234 10/330,067	December 30, 2002	B. Patent No.(s)	pplication is:
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Additional numbers	☑ Yes ☐ No
5. Name and address of party to whom correspondence concerning document should be mailed: Name:	6. Total number of applications and patents involved:  7. Total fee (37 CFR 3.41):\$
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Docket No.: 86654-M (page 4 of 4)

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4. Application number(s) or patent numbers(s):  If this document is being filed together with a new application  Patent Application No. Filing date  October 3, 2003	B. Patent No.(s)
Additional numbers	s ☐ Yes ☒ No
Name and address of party to whom correspondence concerning document should be mailed:	6. Total number of applications and patents involved:
Name:	7. Total fee (37 CFR 3.41):\$
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Statement and signature.	T USE THIS SPACE mation is true and correct and any attached copy is a true copy
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Page 1

#### **ASSIGNMENT**

WHEREAS,

**HYPERCHIP INC.** (acting through RSM RICHTER INC., interim receiver for Hyperchip Inc. pursuant to court orders dated July 13, 2004 and September 20, 2004)

hereinafter referred to as Assignor, whose full post office address is,

2 Place Alexis Nihon, Montreal, Quebec, H3Z 3C2

is the owner of the Intellectual Property as fully set forth and described in the Letters Patents and Patent Applications listed on Schedule A hereto attached,

hereinafter referred to as The Invention(s);

AND WHEREAS.

4198638 Canada Inc.

hereinafter referred to as Assignee, whose full post office address is,

4028 Marlowe, Montreal, Quebec, H4A 3M2

desires to acquire Assignor's entire right, title and interest in and to The Invention(s);

NOW THEREFORE, in consideration of the sum of One Dollar (\$1.00) and other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, and pursuant to the terms and conditions of the Sale Agreement dated September 17, 2004, Assignor does hereby sell, assign, transfer and set over to Assignee, its successors, assigns, or legal representatives, its entire right, title and interest for Canada, the United States and all other countries throughout the World in and to The Invention(s), together with its entire right, title and interest to any and all Letters Patent that have issued or may issue for The Invention(s), including any and all divisions, reissues, continuations and extensions of The Invention(s), to the full end of the term for which each said Letters Patent may be granted, and including any right to claim priority based on The Invention(s), and including the right to bring suit and recover damages for past infringement, the same to be held and enjoyed as fully and completely as the same would have been held and enjoyed by Assignor had this Assignment not been made;

AND ASSIGNOR, on behalf of itself and its executors and administrators, does hereby covenant and agree to do all such lawful acts and things and to execute without further consideration such further lawful assignments, documents, assurances, applications and other instruments as may reasonably be required by said Assignee, its successors, assigns, or legal representatives, to obtain any and all Letters Patent for The Invention and vest the same in said Assignee, its successors, assigns, or legal representatives.

THE PARTIES agree to this Assignment being drawn up in the English language.

Witness
Janet Kamoutsis
Signature //
Jawfanoutty /
Date
October 14 <sup>th</sup> 2004

THE UNDERSIGNED Assignee hereby accepts the Assignment of the Invention(s) and associated Letters Patent and Patent Applications.

Assignee	Witness
Frances Layden	Name
Per	LINDA HUBERT
4198638 CANADA INC.	ZINDIT INDIZIZI
Signature 1 0	Signature
Thank	G. Hutert
Date	Date
October 14, 2004	October 14, 2004

# Petabit Router (PBR) Patents

### PBR Data Plane

Inventor (1)	Category	Fie Number	Application	Description 1 Total Control of the C	Status	FILINGS	
				PBR LOGICAL ROUTERS			
Daniel G. Clemmensen	PBR- Software	P(US)2002-109 US 10/299,857 P(WO)2003-015 PCT/CA03/017	Ξ	Forwarding System With Multiple Logical Sub-Systems	Pending	20/11/2002	
	Manhali narwa wa wanga maya maya maya maya maya ka			PBR TRAFFIC MANAGEMENT			
Steve Rochon, et al.	PBR-TM	P(US)2001-041 US 09/963,487 P(CN)2004-004 P(EP)2004-005		Congestion Avoidance in Packet Switching Devices	Pending	27/09/2001	
Marcelo A.R. De Maria, et al.	PBR-TM	P(US)2001-102 US 09/943,004		Congestion Management for Packet Routers	Pending	31/08/2001	
John Haughey	PBR-TM	P(US)2003-004 US 10/446,707		Forwarding Data Packets Over Multiple Parallel Paths	Pending	29/05/2003	
John Haughey	PBR-TM	P(US)2003-005 US 10/446,884		Forwarding Data Packets Over Multiple Parallel Paths	Pending	29/05/2003	
Richard Norman, et al. PBR-TM	PBR-TM	P(US)2003-006   US 10/448,196		Forwarding Data Packets Over Multiple Parallel Paths	Pending	30/05/2003	
Mohammed Sammour, PBR-TM et al.	PBR-TM	P(WO)2003-014	PCT/CA03/01353	P(WO)2003-014 PCT/CA03/01353 Packet Flow Regulation and Verification of Switching Entity Pending	ending	03/09/2003	
		*					000

## PBR Data Plane (Continued)

Inventor (1)	* Category	File Number	Application inumber	Loudidiosed.	Status	FIIIngs.	
				PBR SWITCH FABRIC (Matrix, OIM)			
Richard Norman, et al. PBR-Fabric	I. PBR-Fabric	P(US)2001-044 P(EP)2003-017 P(CN)2003-018 P(CA)2003-019	US 09/870,766 02 729 739.9	Switch Fabric Architecture Implemented on a Single Chip	Pending	01/06/2001	THE COLUMN TWO IS NOT
Richard Norman, et al. PBR-Fabric	. PBR-Fabric	P(US)2001-045	US 09/870,800	Switch Fabric with Distributed Scheduling	Pending	01/06/2001	
Richard Norman, et al. PBR-Fabric	. PBR-Fabric	P(US)2001-046	US 09/870,703	Switch Fabric with Distributed Arbitration	Pending	01/06/2001	
Richard Norman, et al. PBR-Fabric	l. PBR-Fabric	P(US)2001-047 US 09/870,767		Switch Fabric with Inter-Cell Control for Regulating Packet Flow	Pending	01/06/2001	
Richard Norman, et al. PBR-Fabric	PBR-Fabric	P(US)2001-048 US 09/870,841		Switch Fabric with Control for Regulating Injection of Packets	Pending	01/06/2001	
René Toutant, et al.	PBR-Fabric	P(US)2001-139	US 09/994,017	Programmable Interconnect System for Scalable Router	Pending	27/11/2001	
				PBR MECHANICAL (Matrix, OIM)			
Dorinel Patriche, et al. PBR-Mech	. PBR-Mech	P(US)2000-094	US 09/871,959	Compact Shelf Unit for Electronic Equipment Rack	Issued	04/06/2001	OR
Emmanuel Stathopoulos, et al.	PBR-Mech	P(US)2000-153	US 09/871,942	Insertion and Extraction Aid for Printed Circuit Card	Issued	04/06/2001	OR
Dorinel Patriche	PBR-Mech	P(US)2001-068	US 09/870,842	Midplane for Data Processing Apparatus	Issued	01/06/2001	
Nicolas Villeneuve	PBR-Mech	P(US)2003-002   US 10/445,315	- ин	Apparatus and Method for Inspecting Optical Fiber end Face	Pending	27/05/2003	OR
Daniel Tasse	PBR-Mech	P(US)2003-007	US 10/447,329	Circuit Breaker Module Safety Device and Method	Pending	29/05/2003	OR

### PBR Control Plane

Inventor (1)	Category	Category File Number	Application number	Description	Status	Priodly Date:
Richard Norman, et al. PBR - Control P(US)2001-078 US 09/916. Plane	PBR - Control Plane	P(US)2001-078	US 09/916,200	5,200 Storage and Processing of Routing Information	Pending	27/07/2001
Jérôme Duplaix, et al. PBR - Control P(US)2001-079 US 09/915, Plane	PBR - Control Plane	P(US)2001-079	US 09/915,332	,332 Router with a Distributed Routing Architecture	Pending	27/07/2001
John Haughey	PBR - Control Plane	PBR - Control P(US)2001-110 US 09/981. Plane	US 09/981,883	,883 Executing Multiple Tasks in a Task Set	Pending	19/10/2001
Jérôme Duplaix, et al. PBR - Control P(EP)2004-002 Plane	PBR - Control   Plane	P(EP)2004-002		Scalable Router	Pending	

#### Orphaned IP

Inventor (1)	Category	File Number	Application number	Description	Status	Filing	
				LARGE AREA (LA) IC – DEFECT TOLERANCE	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		
Richard Norman	LAIC-DT	$\sim$		Efficient Direct Cell Replacement Fault Tolerance	Pending		OR
		P(JP)1996-004			Pending		•
		P(KR)1996-005 P(US)1999-009	705245/96 US 09/376.194		Issued		****************
			US 09/679,168		Issued		<del></del>
Richard Norman	LAIC-DT	P(EP)1996-003  95912116.1	95912116.1	Defect Tolerance with Use of Unassigned Spare Cells	Issued	22/03/1995	
Richard Norman	LAIC-DT	P(US)1996-001 US 08/618,397	US 08/618,397	Direct Replacement Cell Fault Tolerance	Issued	22/03/1995	OR
Richard Norman	LAIC-DT	P(US)2002-124 US 10/330,069	US 10/330,069	Array of Discrete Modules Fabricated on a Wafer	Allowed	30/12/2002	
Richard Norman, et al. LAIC-DT	LAIC-DT	P(US)2002-133	US10/324,071	Bus For Parallel Processing System	Pending	20/12/2002	OR
Yvon Savaria, et al.	LAIC-DT	P(US)2002-134 US 10/324,1	US 10/324,110	Large Scale Signal Paths in Parallel Processing System	Pending	20/12/2002	OR
Yvon Savaria, et al.	LAIC-DT	P(US)2002-135 US 10/323,896	US 10/323,896	Fault Tolerant Scan Chain for a Parallel Processing System	Pending	20/12/2002	OR
Richard Norman	LAIC-DT	P(US)2003-001 US10/368,003	US10/368,003	Fault Tolerant Cell Array Architecture	Pending	19/02/2003	OR
				LA IC – INTER-RETICLE STITCHING			And the second second
Richard Norman	LAIC/IRS	P(US)1998-004 US 09/144,695	US 09/144,695	Integrated Circuit Having Lithographic Array Interconnections	Issued	01/09/1998	OR
Richard Norman, et al. LAIC-IRS	LAIC-IRS	P(US)2002-131 US 10/330,068	US 10/330,068	Wave-Front Clock Synchronization	Pending	30/12/2002	
Richard Norman, et al. LAIC-IRS	LAIC-IRS	P(US)2003-011	US 10/462,283	Bus Architecture with Efficient Use of Integrated Circuit Area	Pending	17/06/2003	
				LA IC – INPUT/OUTPUT			
Richard Norman	LAIC-I/O	P(US)1994-002 US 08/323,580	US 08/323,580	Massively-Parallel Array with Outputs from Individual Processors	Issued	17/10/1994	OR
Richard Norman	LAIC-I/O	P(EP)1999-013 00110048.6 P(GB)2003-003 00110048.6	00110048.6 00110048.6	Massively Parallel System w/ Photovoltaic Cells Display Architecture with Integrated Power Supply	Issued Validated	22/03/1995	OR
Richard Norman	LAIC-I/O	P(US)2001-183 US 10/000,8	US 10/000,813	Output and/or Input Coordinated Processing Array	Issued	30/11/2001	OR
				LA IC – SIGNAL INTERGRITY			

Inventor (1)	Category	File Number Application number	Description	snjejs,	Filings Date	
Karl Fecteau, et al. Yvon Savaria, et al.	LAIC-SI	P(US)2001-199 US 10/022,856 P(US)2001-200 US 10/022,852	Method for Reducing Interference on Nearby Conductors	Pending Allowed	20/12/2001	OR OR
Claude Thibeault et al.		P(US)2001-201   US 10/023,478   P(US)2001-019   US 10/022,851		Pending Pending	70000000000000000000000000000000000000	OR
Richard Norman	LAIC-SI	P(US)2002-130 US 10/330,230	Reference Wires for an Electrical Bus	Pending	30/12/2002	
Richard Norman	LAIC-SI	P(US)2003-016 US 10/739,047	Conductive Fabric with Balanced Mutual Interference	Pending	19/12/2003	
**************************************			LA IC – MECHANICAL/PACKAGING			
Richard Norman	LAIC-Mech	LAIC-Mech P(US)2002-125 US 10/330,231	High-Performance Interconnect for Discrete Modules	Pending	30/12/2002	
Richard Norman	LAIC-Mech	P(US)2002-126 US 10/330,232	Connector Between Contact Pads on Two Surfaces	Pending	30/12/2002	
Richard Norman, et al. LAIC-Mech	LAIC-Mech	P(US)2002-127 US 10/330,234	Reduced Thermal Expansion Effects	Pending	30/12/2002	
Richard Norman	LAIC-Mech	P(US)2002-128 US 10/330,067	Defect Tolerant Method of Mounting Chip to Substrate	Pending	30/12/2002	
Richard Norman	LAIC-Mech	P(US)2002-129 US 10/330,233	Compound Semiconductor Structure	Pending	30/12/2002	
Richard Norman	LAIC-Mech	P(US)2002-132 US 10/330,319	Architecture for a Microelectronic Complex on a Planar Body	Pending	30/12/2002	
Richard Norman	LAIC-Mech	P(US)2003-008 US 10/458,734	Method for Continuous Linear Production of Integrated Circuits	Pending	11/06/2003	OR
Norman, et al.	LAIC-Mech	Richard Norman, et al. LAIC-Mech P(US)2003-009 US 10/606,886	Flexible Device for Interfacing with a Wafer	Pending	27/06/2003	
Richard Norman	LAIC-Mech	P(US)2003-012	Connectors with Fault Tolerance	Pending	03/10/2003	
Richard Norman	LAIC-Mech	LAIC-Mech P(US)2003-013 US 10/677.292	Cooling Multiple Discrete Functional Modules	Pending	03/10/2003	

PATENT
RECORDED: 11/12/2004 REEL: 015983 FRAME: 0685