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RECORDATION FORM COVER SHEET

PATENTS ONLY

To the Director of the U.S. Patents and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)/Execution Date(s):
Silicon Service Consortium, Inc.

Execution Date(s) January 27, 2005

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Name: Cerian Technology Ventures, LLC

Internal Address:

Street Address: 5405 Morehouse Drive

Suite 245

City: San Deigo

State: California

Country United States of America Zip 92121

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
Other

4. Application number(s) or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s): 08/718,215; 09/016,078; 09/059,612; 09/059,534; 09/093,818; 08/718,215; 09/139,935; 09/150,973; 10/894,754

B.

Additional numbers attached? ☐ Yes ☒ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Bo-In Lin (Reg. No. 33,948)

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Street Address: 13445 Mandoli Drive

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State: CA Zip: 94022

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Email Address:

6. Total number of applications and patents involved: 9

7. Total fee (37 CFR 1.21(h) & 3.41) $360.00

☐ Authorized to be charged by credit card
☒ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

B. Deposit account number: 23-2415 (Attorney docket no. 30532-008)

Authorized User Name Wilson Sonsini Goodrich & Rosati

9. Signature.

Signature

4/4/05
Date

Shirley Chen (Reg. No. 44,608)
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 6

Documents to be recorded (including cover sheet) should be faxed to (703) 306-5995, or mailed to:
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CH $380.00 232415 09016078

EXHIBIT B

PATENT ASSIGNMENT AGREEMENT

THIS PATENT ASSIGNMENT is made as of the 27 day of January 2005, from Silicon Service Consortium, Inc., a corporation organized under the laws of Texas, with an address at 3500 Comsouth Drive, Suite 100, Austin, Texas 78744 ("Assignor") to Cerian Technology Ventures, a company existing pursuant to the laws of Delaware, with an address at 5965 Mayerhofer Dr San Diego ("Assignee")

WHEREAS, Assignor is the owner of the patents and patent applications (the "Patents") set forth in Exhibit A attached hereto.

WHEREAS, Assignor and Assignee have entered into a Patent Purchase Agreement dated as of January 24th, 2005 pursuant to which Assignor has agreed, *inter alia*, to grant and assign to Assignee all of Assignor's right title and interest in and to the Patents and Assignee desires to acquire the entire right, title and interest in and to the Patents.

NOW, THEREFOR, in consideration of the foregoing and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

I. Assignor hereby irrevocably sells, transfers, conveys and assigns unto Assignee, its successors and assigns, Assignor's entire right, title and interest in and to the Patents and any continuations, continuation-in-parts, divisions, reissues, re-examinations or extensions of the Patents, including all past and future income, royalties, damages and payments due (including, rights to damages and payments for past, present or future infringements or misappropriations) with respect thereto, in each case, of Assignor in all countries relating to the Patents.

II. Assignor hereby authorizes the Commissioner of Patents and Trademarks of the United States and other empowered officials of the United States Patent and Trademark Office and/or the appropriate empowered officials other relevant jurisdictions outside the United States to record the transfer of the Patents to Assignee as assignee of Assignor's entire right, title and interest therein, in accordance with this Patent Assignment, and to issue to Assignee all letters patent which may issue with respect to the Patents.

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[Signature Page Attached]

IN WITNESS WHEREOF, Assignor has caused these presents to be duly executed in a manner appropriate thereto as of the date first above written.

Assignor: _____

By: _____

Name: John M. Smith

Title: President SSC, Inc.

ACKNOWLEDGMENT

State of Texas)
) ss:
County of Travis)

On this 27th day of Jan 2005 before me, the undersigned, personally appeared John M. Smith ☐ personally known to me - OR - ☐ proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

Signature: _____ (Seal)
Notary Public

DORISANN HILL
MY COMMISSION EXPIRES
June 16, 2008

EXHIBIT A

PURCHASED PATENTS AND PATENT APPLICATIONS

1. **US Issued Patents**

	Patent #	Filed	Title
1	5,668,026	5/26/97	DMOS fabrication process implemented with reduced number of masks
2	5,729,037	4/26/96	MOSFET structure and fabrication process for decreasing threshold voltage
3	5,731,611	1/30/96	MOSFET transistor cell manufactured with selectively implanted punch through prevent and threshold reduction zones
4	5,747,853	8/7/96	Semiconductor structure with controlled breakdown protection
5	5,763,914	7/16/97	Cell topology for power transistors with increased packing density
6	5,763,915	2/27/96	DMOS transistors having trenched gate oxide
7	5,767,567	9/10/96	Design of device layout for integration with power MOSFET packaging to achieve better lead wire connections and lower on resistance
8	5,844,277	2/20/96	Power MOSFETs and cell topology
9	5,877,528	3/3/97	Structure to provide effective channel-stop in termination areas for trenched power transistors
10	5,877,529	11/26/97	MOSFET termination design and core cell configuration to increase breakdown voltage and to improve device ruggedness
11	5,883,410	7/13/97	Edge wrap-around protective extension for covering and protecting edges of thick oxide layer
12	5,883,416	1/31/97	Gate-contact structure to prevent contact metal penetration through gate layer without affecting breakdown voltage
13	5,894,150	12/8/97	Cell density improvement in planar DMOS with farther-spaced body regions and novel gates
14	5,895,951	4/5/96	MOSFET structure and fabrication process implemented by forming deep and narrow doping regions through doping trenches
15	5,907,169	4/18/97	Self-aligned and process-adjusted high density power transistor with gate sidewalls provided with punch through prevention and reduced JFET resistance
16	5,907,776	7/11/97	Method of forming a semiconductor structure having reduced threshold voltage and high punch-through tolerance
17	5,923,065	6/12/96	Power MOSFET device manufactured with simplified fabrication processes to achieve improved ruggedness and product cost savings

	Patent #	Filed	Title
18	5,930,630	7/23/97	Method for device ruggedness improvement and on-resistance reduction for power MOSFET achieved by novel source contact structure
19	5,960,275	10/28/96	Power MOSFET fabrication process to achieve enhanced ruggedness, cost savings, and product reliability
20	5,973,361	9/15/97	DMOS transistors with diffusion merged body regions manufactured with reduced number of masks and enhanced ruggedness
21	5,986,304	1/13/97	Punch-through prevention in trenched DMOS with poly-silicon layer covering trench corners
22	5,998,266	12/19/96	Method of forming a semiconductor structure having laterally merged body layer
23	6,005,271	11/5/97	Semiconductor cell array with high packing density
24	6,025,230	11/6/97	High speed MOSFET power device with enhanced ruggedness fabricated by simplified processes
25	6,031,265	10/16/97	Enhancing DMOS device ruggedness by reducing transistor parasitic resistance and by inducing breakdown near gate runners and termination area
26	6,046,078	4/28/97	Semiconductor device fabrication with reduced masking steps
27	6,048,759	2/11/98	Gate/drain capacitance reduction for double gate-oxide DMOS without degrading avalanche breakdown
28	6,049,104	11/28/97	MOSFET device to reduce gate-width without increasing JFET resistance
29	6,051,468	9/15/97	Method of forming a semiconductor structure with uniform threshold voltage and punch-through tolerance
30	6,104,060	2/20/96	Cost savings for manufacturing planar MOSFET devices achieved by implementing an improved device structure and fabrication process eliminating passivation layer and/or field plate
31	6,172,398	8/11/97	Trenched DMOS device provided with body-dopant redistribution-compensation region for preventing punch through and adjusting threshold voltage
32	6,262,453	4/24/98	Double gate-oxide for reducing gate-drain capacitance in trenched CMOS with high-dopant concentration buried-reguin under trenched gate
33	6,281,547	5/8/97	Power transistor cells provided with reliable trenched source contacts connected to narrower source manufactured without a source mask
34	6,404,025	10/2/97	MOSFET power device manufactured with reduced number of masks by fabrication simplified processes

	Patent #	Filed	Title
35	6,426,260	9/5/00	Switching speed improvement in DMO by implanting lightly doped region under gate

2. US Applications

	App #	Status	Filed	Title
1	08/718,215	Abandoned	9/20/96	Semiconductor Cell Structure Defined by Intersecting Trenches with Compensated Cell Corners
2	09/016,078	Abandoned	1/30/98	Planar DMOS Cell Array with High Packing Density
3	09/059,612	Abandoned	4/13/98	High-Frequency Switching Power MOSFET Device
4	09/059,534	Abandoned	4/13/98	Structure with Non-Orthogonal Polygram for Power ...
5	09/093,818	Pending	6/3/98	Electrical Contacting Scheme of a Trench Semiconductor
6	08/718,215	Abandoned	6/23/98	Semiconductor Cell Structure Defined by Intersecting Trenches with Compensated Cell Corners
7	09/139,935	Pending	8/5/98	Gate Contacting Scheme of a Trench MOSFET Structure
8	09/150,973	Abandoned	9/10/98	Structure and Method of Improving Device Ruggedness ...
9	10/894,754	Pending	7/19/04	Semiconductor Circuit with Built-In Regulated Protections