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PATENTS ONLY 2001 Staas & Halsey LLP To the Director of the U.S. Patent and Trademark Office: Please record the attached original documents or copy thereof. Name of conveying party(ies): Hirotaka MORITA Shinii FUKASAWA 2. Name and Address of receiving party(ies): **FUJITSU LIMITED** 1-1, Kamikodanaka 4-chome Nakahara-ku, Kawasaki-shi Kanagawa 211-8588 Japan 3. Nature of conveyance: Assignment \_X\_ Merger Security Agreement Change of Name Other: Execution Date(s): November 22, 2004 4. Application number(s) or patent number(s): ☐ This document is being filed together with a new application: The execution date(s) of the application is/are: November 22, 2004 (a) (b) The title is: LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, LAYOUT PROGRAM FOR SEMICONDUCTOR INTEGRATED CIRCUIT AND LAYOUT SYSTEM FOR SEMICONDUCTOR INTEGRATED CIRCUIT OR ☐ This document is being filed after filing of the application: Patent Application No(s). \_\_/\_\_\_, filed \_ (a) (b) , issued Patent No(s). 5. Name and address of party to whom correspondence concerning document should be mailed: STAAS & HALSEY LLP Our Docket: 1460.1050 Attention: H. J. Staas 1201 New York Ave., N.W., Suite 700 Washington, D.C. 20005 6. Total number of applications and patents involved: 1 7. Total fee (37 CFR 3.41)..... (\$ 40.00 per Assignment) **Enclosed** Х Authorized to be charged to deposit account. Deposit Account No.: 19-3935 (Any underpayment is authorized to be charged to this Deposit Account) 8. (Attach duplicate copy of this page if paying by deposit account) 9. Statement and signature. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. H. J. Staas, Reg. No. 22,010 December 29, 2004 Name of Person Signing Signature Date Total number of pages including cover sheet: 2 DO NOT USE THIS SPACE /04/2006 HTECKLU1 00000019 11023516

**PATENT** 

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## **U.S. ASSIGNMENT**

S&H 1/00

FUJITSU LIMITED		
1-1, Kamikodanaka 4-Chome, Nakahara-ku,	– Kawasaki-shi, Kanagawa 211-8588 Ja	ipan
1 1, Manufacture v Chamber value		
(hereinaster, "ASSIGNEE"), the receipt of which is he ASSIGNEE the entire and exclusive right, title and in (Title of Invention)  LAYOUT METHOD FOR SEMICONDUCTOR	terest to the invention entitled	
INTEGRATED CIRCUIT AND LAYOUT SYSTE	M FOR SEMICONDUCTOR INTEC	JRATED CIRCUIT
relating to International Patent Application PCT/JP_executed on even date herewith or, if not so executed		lication for Letters Patent of the United States was
(a) executed on	; (Insert date of execution	n of application, if not concurrent)
(b) filed on		of STAAS & HALSEY LLP, 700 Eleventh Street,
Serial No;	N.W., Washington, D.C. insert in (b) the specified	. 20001 (202/434-1500) is hereby authorized to d data, when known.
and to said application and all Letters Patent(s) of the substitute, reissue or reexamination application based including any extensions thereof (collectively, herein:  The ASSIGNOR agree(s), when requested by said which the ASSIGNEE may deem necessary, desirable including in the preparation and prosecution of said a	thereon, for the full term or terms for after, "said application(s) and Letters leads a substitution of the substitution of th	which the said Letters Patent(s) may be granted and Patent(s)").  ut at the expense of said ASSIGNEE, to do all acts ing and enforcing protection for said invention, Letters Patent(s), in any interference, reissue, ch may arise or be declared in relation to same, such
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**RECORDED: 12/29/2004**