PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Patent Security Agreement (Second Lien)

CONVEYING PARTY DATA

Name	Execution Date
Stratus Technologies Bermuda Ltd.	03/29/2006

RECEIVING PARTY DATA

Name:	Deutsche Bank Trust Company Americas
Street Address:	60 Wall Street
City:	New York
State/Country:	NEW YORK
Postal Code:	10005

PROPERTY NUMBERS Total: 37

Property Type	Number
Patent Number:	6842823
Patent Number:	6691225
Patent Number:	6813721
Patent Number:	6948010
Patent Number:	6802022
Patent Number:	6886171
Patent Number:	6766479
Patent Number:	6718474
Patent Number:	6970892
Patent Number:	6996750
Patent Number:	6766413
Patent Number:	6874102
Patent Number:	6901481
Patent Number:	6862689
Patent Number:	6971043

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Patent Number:	6928583
Patent Number:	6735715
Patent Number:	6708283
Patent Number:	6355991
Patent Number:	6820213
Patent Number:	6633996
Patent Number:	6687851
Patent Number:	6691257
Application Number:	09819883
Application Number:	11095173
Application Number:	11143259
Application Number:	11267462
Application Number:	11146864
Application Number:	11145784
Application Number:	11118869
Application Number:	11193928
Application Number:	11337697
Application Number:	10997409
Application Number:	11125884
Application Number:	11329244
Application Number:	11202526
Application Number:	11207289

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NAME OF SUBMITTER:	Anna T. Kwan

Total Attachments: 14
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PATENT SECURITY AGREEMENT

Patent Security Agreement, dated as of March 29, 2006 (as amended, restated or otherwise modified from time to time, the "Patent Security Agreement"), between each of the signatories hereto ((together with any other entity that may become a party hereto as provided in the Collateral Agreement (as defined below), the "Grantors"), and Deutsche Bank Trust Company Americas ("DBTCA"), in its capacity as administrative agent for the Secured Parties (together with any successors and assigns thereto in such capacity, the "Administrative Agent").

WITNESSETH:

WHEREAS, Grantors are party to a Collateral Agreement dated as of March 29, 2006 (the "Collateral Agreement") between each of the Grantors and the other grantors thereto and the Administrative Agent pursuant to which the Grantors are required to execute and deliver this Patent Security Agreement;

NOW, THEREFORE, in consideration of the premises and to induce the Lenders (as defined below) to enter into the Second Lien Credit Agreement, dated as of March 29, 2006 among Stratus Technologies, Inc., Stratus Technologies Bermuda Ltd., Stratus Technologies International, S.á r.l., the lenders from time to time parties thereto (the "Lenders"), Goldman Sachs Credit Partners L.P. ("GSCP"), as syndication agent, DBTCA, as administrative agent, and GSCP and Deutsche Bank Securities Inc., as joint lead arrangers and joint bookrunners, the Grantors hereby agree with the Administrative Agent, as follows:

SECTION 1. Defined Terms. Unless otherwise defined herein, terms defined in the Collateral Agreement and used herein have the meaning given to them in the Collateral Agreement.

SECTION 2. Grant of Security Interest in Patent Collateral. Each Grantor hereby pledges and grants to the Administrative Agent, for the benefit of the Secured Parties, a security interest in all of such Grantor's right, title and interest in, to and under the following, whether presently existing or hereafter created or acquired (collectively, the "Patent Collateral"):

(a) all United States and foreign patents and certificates of invention, or similar industrial property rights, and applications for any of the foregoing (collectively, "Patents"), including, but not limited to: (i) each patent and patent application referred to on Schedule I hereto (as such schedule may be amended or supplemented from time to time), (ii) all reissues, divisions, continuations, continuations-in-part, extensions, renewals, and reexaminations thereof, (iii) all rights corresponding thereto throughout the world, (iv) all inventions and improvements described therein, (v) all rights to sue for past, present and future infringements thereof, (vi) all licenses, claims, damages, and proceeds of suit arising therefrom, and (vii) all Proceeds of the foregoing, including, without limitation, licenses, royalties, income, payments, claims, damages, and proceeds of suit; and

(b) all agreements providing for the granting of any right in or to Patents (whether such Grantor is licensee or licensor thereunder) including those referred to on Schedule I hereto (collectively, "Patent Licenses").

SECTION 3. Security Agreement. The security interest granted pursuant to this Patent Security Agreement is granted in conjunction with the security interest granted to the Administrative Agent for the Secured Parties pursuant to the Collateral Agreement and Grantors hereby acknowledge and affirm that the rights and remedies of the Administrative Agent with respect to the security interest in the Patent Collateral made and granted hereby are more fully set forth in the Collateral Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein. In the event that any provision of this Patent Security Agreement is deemed to conflict with the Collateral Agreement, the provisions of the Collateral Agreement shall control.

SECTION 4. Applicable Law. This Patent Security Agreement and the rights and obligations of the parties hereunder shall be governed by, and shall be construed and enforced in accordance with, the laws of the State of New York, without regard to its conflicts of law provisions (other than Section 5-1401 and Section 5-1402 of the New York General Obligation Laws).

SECTION 5. Counterparts. This Patent Security Agreement may be executed in any number of counterparts, each of which when so executed and delivered shall be deemed an original, but all such counterparts together shall constitute but one and the same instrument.

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IN WITNESS WHEREOF, each Grantor has caused this Patent Security Agreement to be executed and delivered by its duly authorized officer as of the date first set forth above.

STRATUS TECHNOLOGIES BERMUDA LTD.

By: _____

Name: SHARON WARD

Title: SECRETARY

Accepted and Agreed:

DEUTSCHE BANK TRUST COMPANY AMERICAS,
as Administrative Agent

By: Paul O'Leary
Name: Paul O'Leary
Title: Vice President

By: Lana Gifas
Name: Lana Gifas
Title: Vice President

SCHEDULE I
to
PATENT SECURITY AGREEMENT

PATENT REGISTRATIONS AND APPLICATIONS

See attached.

Stratus Technologies International, S.A.R.L.
(f/k/a Stratus Computer Systems, S.A.R.L.)

ISSUED PATENTS:

	Kirkpatrick Ref. No	Stratus Ref. No.	Title	Date Issued	Patent No.
1	SRT-001	S8	Methods and Apparatus for Persistent Volatile Computer Memory	Jan. 11, 2005	6,842,823
2	SRT-003	S12	Method and Apparatus for Deterministically Booting a Redundant Fault-Tolerant System	Feb. 10, 2004	6,691,225
3	SRT-008	H21	Methods and Apparatus for Generating High-Frequency Clocks Deterministically From a Low-Frequency System Reference Clock	Nov. 2, 2004	6,813,721
4	SRT-009	H3/13	A Method and Apparatus for Efficiently Moving Portions of a Memory Block	Sept. 20, 2005	6,948,010
5	SRT-010	S11	Maintenance of Consistent, Redundant Mass Storage Images	October 5, 2004	6,802,022
6	SRT-011	H7	Caching For I/O Virtual Address Translation And Validation Using Devise Drivers	April 26, 2005	6,886,171
7	SRT-012	H5	Apparatus and Methods for Identifying Bus Protocol Violations	July 20, 2004	6,766,479
8	SRT-013	H26	Method and Apparatus for Clock Management Based on Environmental Conditions	April 6, 2004	6,718,474
9	SRT-014	S32	Implementing Standards-Based File Operations in Proprietary Operating Systems	Nov. 29, 2005	6,970,892
10	SRT-016	H8	Methods And Apparatus for Computer Bus Error Termination	February 7, 2006	6,996,750
11	SRT-019	S34	Systems and Methods for Caching With File-Level Granularity	July 20, 2004	6,766,413
12	SRT-020	H27	Coordinated Recalibration Of High Bandwidth Memories in a Multiprocessor Computer	March 29, 2005	6,874,102
13	SRT-021	S33	A Method and Apparatus for Storing Transactional Information in Persistent Memory	May 31, 2005	6,901,481
14	SRT-023	S35	A Method and Apparatus for Managing Session Information	March 1, 2005	6,862,689
15	SRT-024	H42	Apparatus and Method for Accessing a Mass Storage Device in a Fault-Tolerant Server	Nov. 29, 2005	6,971,043
16	SRT-025	H40	Apparatus and Method for Two Computing Elements in a Fault-Tolerant Server to Execute Instructions In Lockstep	August 9, 2005	6,928,583
17	SRT-029	S9	System and Method for Operating a SCSI Bus With Redundant SCSI Adaptors	May 11, 2004	6,735,715
18	SRT-030	H15/16/19	System and Method for Operating a System With Redundant Peripheral Bus Controllers	March 16, 2004	6,708,283
19	SRT-031	H10	Hot Plug Switch Mechanism	March 12, 2002	6,355,991
20	SRT-032	H1	Fault-Tolerant Computer System With Voter Delay Buffer	Nov. 16, 2004	6,820,213

	Kirkpatrick Ref. No	Stratus Ref. No.	Title	Date Issued	Patent No.
21	SRT-033	S3A	Fault-Tolerant Maintenance Bus Architecture	October 14, 2003	6,633,996
22	SRT-034	H12	Method and System for Upgrading Fault-Tolerant Systems	February 3, 2004	6,687,851
23	SRT-035	S3B	Fault-Tolerant Maintenance Bus Protocol and Method for Using The Same	Feb. 10, 2004	6,691,257

PENDING PATENT APPLICATIONS:

	Kirkpatrick Ref. No.	Stratus Ref. No.	Title	Filing Date	Application No.
1	SRT-022	H39	Apparatus And Methods for Fault-Tolerant Computing Using a Switching Fabric	March 28, 2001	09/819,883
2	SRT-050	H58/59	Systems and Methods for Maintaining Synchronicity During Signal Transmission.	March 31, 2005	11/095,173
3	SRT-050CP	H58/59	Systems and Methods for Maintaining Synchronicity During Signal Transmission. (CIP)	June 2, 2005	11/143,259
4	SRT-053	H70	Apparatus and Method for Translating Addresses	November 4, 2005	11/267,462
5	SRT-055	S53	Methods for Ensuring Safe Component Removal	June 7, 2005	11/146,864
6	SRT-057	H60-64, H66-68	Computer Rack Mounting System	June 6, 2005	11/145,784
7	SRT-059	H78	Systems And Methods For Checkpointing	April 29, 2005	11/118,869
8	SRT-061	H80	Systems and Methods for Checkpointing	July 29, 2005	11/193,928
9	SRT-062	H81	Apparatus and Method for High Performance Checkpointing and Rollback of Network Operations	January 23, 2006	11/337,697
10	SRT-064	H85	Tracking Modified Pages on a Computer System	November 23, 2004	10/997,409
11	SRT-065	H87	Systems and Methods for Ensuring High Availability	May 10, 2005	11/125,884
12	SRT-067	H75	Handling Non-Deterministic Errors in a Fault Tolerant System	January 10, 2006	11/329,244
13	SRT-068	H83	Hardware Checkpointing System	August 12,2005	11/202,526
14	SRT-070	S60	Systems and Methods for Split Mode Operation of Fault-Tolerant Computer Systems	August 19, 2005	11/207,289

Licensed Patents (Stratus Computer, Inc. (OldCo) Patents licensed under the Asset Purchase of Stratus Computer Inc. by Stratus Computer Systems International Sarl of February 26, 1999. (divestiture agreement).

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
06/762,039	**4,654,857**	**Digital Data Processor with High Reliability**	**USA**	**03/31/87**	**03/31/04**
	0,077,154	Digital Data Processor with High Reliability	EPO	10/12/86	09/30/02
	1,830,325	Digital Data Processor with High Reliability	Japan	03/15/94	
	1,178,712	Digital Data Processor with High Reliability	Canada	11/27/84	11/27/01
06/904827	**4,750,177**	**Digital Data Processor Apparatus w/Pipelined with Fault Tolerant Bus Protocol**	**USA**	**06/07/88**	**09/08/06**
	0,077,153	Digital Data Processor with Fault Tolerant Bus Protocol	EPO	03/04/87	09/30/02
	1,180,453	Digital Data Processor with Fault Tolerant Bus Protocol	Canada	01/02/85	01/02/02
57-169959		Digital Data Processor with Fault Tolerant Bus Protocol	Japan		
06/307,525	**4,453,215**	**Central Processing Apparatus for Fault Tolerant Computing**	**USA**	**06/05/84**	**10/01/01**
06/698,257	**4,597,084**	**Computer Memory Apparatus**	**USA**	**06/24/86**	**02/04/05**
06/307,524	**4,486,826**	**Computer Peripheral Control Apparatus**	**USA**	**12/04/84**	**10/01/01**
	1,606,955	Computer Peripheral Control Apparatus	Japan	06/13/91	09/30/08
	0,076,655	Computer Peripheral Control Apparatus	EPO	09/17/86	09/30/02
	1,178,374	Computer Peripheral Control Apparatus	Canada	11/20/84	11/20/01
06/927,746	**4,816,990**	**Method and Apparatus for Fault Tolerant Computer Systems**	**USA**	**03/28/89**	**11/05/06**
		Having Expandable Processor Section			
	0 267 011	Method and Apparatus for Fault Tolerant Computer Systems	EPO		
		Having Expandable Processor Section			
	0 267 011	Method and Apparatus for Fault Tolerant Computer Systems	Switzerland		
		Having Expandable Processor Section			
	0 267 011	Method and Apparatus for Fault Tolerant Computer Systems	Italy		
		Having Expandable Processor Section			
	0 267 011	Method and Apparatus for Fault Tolerant Computer Systems	Germany		
		Having Expandable Processor Section			
62-278458	262 3261	Method and Apparatus for Fault Tolerant Computer Systems	Japan	04/11/97	11/05/07
		Having Expandable Processor Section			
08325843		Method and Apparatus for Fault Tolerant Computer Systems	Japan		

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
		Having Expandable Processor Section			
07/227,471	**4,866,604**	**Digital Data Processing Apparatus with Pipeland Memory Cycles**	**USA**	**09/12/89**	**08/01/08**
P62-201966		Digital Data Processing Apparatus with Pipeland Memory Cycles	Japan		
	0256864	Digital Data Processing Apparatus with Pipeland Memory Cycles	EPO	02/23/94	08/14/07
07/003,732	**5,020,024**	**Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism**	**USA**	**05/28/91**	**05/28/08**
	0349539	Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	EPO		
	E88028B	Method and Apparatus for Digital Logic Synchronization Monitoring	Austria	01/14/88	
	0,349,539	Method and Apparatus for Digital Logic Synchronization Monitoring	Belgium	04/07/93	
	P3880132T2	Method and Apparatus for Digital Logic Synchronization Monitoring	Germany	04/07/93	
	614277	Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	Australia	01/08/92	01/14/01
	68044/BE/93	Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	Italy	01/21/93	01/14/01
	0349539	Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	Sweden	04/07/93	01/14/01
	2573508	Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	Japan	10/24/96	01/14/01
PCT/US88/00065		Method and Apparatus for Detecting Selected Absence of Digital Logic Synchronism	Patent Co-op Treaty		
07/018,629	**4,920,540**	**Fault-Tolerant Digital Timing Apparatus and Method**	**USA**	**04/24/90**	**02/25//07**
		Fault-Tolerant Digital Timing Apparatus and Method	Japan		
88102650.4	0 280 258	Fault-Tolerant Digital Timing Apparatus and Method	EPO	03/30/95	02/23/08
88102650.4	0 280 258	Fault-Tolerant Digital Timing Apparatus and Method	France	03/30/95	02/23/08
88102650.4	3853734.6-08	Fault-Tolerant Digital Timing Apparatus and Method	Germany	03/30/95	02/23/08
88102650.4	0 280 258	Fault-Tolerant Digital Timing Apparatus and Method	UK	03/30/95	02/23/08
07/079,297	**4,926,315**	**Digital Data Processor with Fault Tolerant Peripheral Bus Comm.**	**USA**	**05/15/90**	**07/29/07**
	1323442	Digital Data Processor with Fault Tolerant Peripheral Bus Comm.	Canada	04/19/93	06/20/09
07/368,125	**4,974,150**	**Fault Tolerant Digital Data Processor w/Improved I/O Controller**	**USA**	**11/27/90**	**06/16/09**
	1,323,441	Fault Tolerant Digital Data Processor w/improved I/O Controller	Canada	10/19/93	06/20/09
		Fault Tolerant Digital Data Processor w/improved I/O Controller	EPO		
		Fault Tolerant Digital Data Processor w/improved I/O Controller	Japan		

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
07/368,124	**4,974,144**	**Digital Data Processor with Fault Tolerant Peripheral Interface**	**USA**	**11/27/90**	**06/10/09**
	1 319754	Digital Data Processor with Fault Tolerant Peripheral Interface	Canada	06/29/93	06/20/09
		Digital Data Processor with Fault Tolerant Peripheral Interface	EPO		
		Digital Data Processor with Fault Tolerant Peripheral Interface	Japan		
07/079,218	**4,931,922**	**Method and Apparatus for Monitoring Peripheral Device Communications**	**US**	**06/05/90**	**07/29/07**
	1323440	Method and Apparatus for Monitoring Peripheral Device Communications	Canada	10/19/93	06/20/09
		Method and Apparatus for Monitoring Peripheral Device Communications	EPO		
		Method and Apparatus for Monitoring Peripheral Device Communications	Japan		
07/079,223	**4,939,643**	**Fault Tolerant Digital Data Processor w/Improved Bus Protocol**	**USA**	**07/03/90**	**07/29/07**
	1323443	Fault Tolerant Digital Data Processor w/improved Bus Protocol	Canada	10/19/93	06/20/09
		Fault Tolerant Digital Data Processor w/improved Bus Protocol	EPO		
		Fault Tolerant Digital Data Processor w/improved Bus Protocol	Japan		
07/884,257	**5,243,704**	**Multinodal Interconnection System; Optimized Interconnect Network**	**USA**	**09/07/93**	**05/19/12**
2016193-1		Multinodal Interconnection System;Optimized Interconnect Network	Canada		
	0398678	Multinodal Interconnection System;Optimized Interconnect Network	EPO		
	0398678	Multinodal Interconnection System;Optimized Interconnect Network	France		
	DE69031011T2	Multinodal Interconnection System; Optimized Interconnect Network	Germany	10/09/97	
	0398678	Multinodal Interconnection System; Optimized Interconnect Network	Netherlands		
	0398678	Multinodal Interconnection System; Optimized Interconnect Network	U. K.		
02-130098		Multinodal Interconnection System;Optimized Interconnect Network	Japan		
414,107	**5,049,701**	**EMI Cabinet with Improved Inteerference Suppression**	**USA**	**09/17/91**	**09/28/09**
	0420278	EMI Cabinet with Improved Inteerference Suppression	EPO	09/21/94	
	DE 6901272572	EMI Cabinet with Improved Inteerference Suppression	Germany		
		EMI Cabinet with Improved Inteerference Suppression	France		
		EMI Cabinet with Improved Inteerference Suppression	U. K.		
2-256788		EMI Cabinet with Improved Inteerference Suppression	JP		

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
2024790-8			Canada		
743,992	5,379,381	I/O Controller Apparatus & Method for Transferring Data between a Host Processor & Multiple I/O Units	USA	01/03/95	08/12/11
07/743,691	5,257,383	Programmable Interrupt Priority Encoder Method & Apparatus	USA	10/26/93	08/12/11
92110499.8	0528139	Programmable Interrupt Priority Encoder Method & Apparatus	EPO	07/01/98	06/22/12
		Programmable Interrupt Priority Encoder Method & Apparatus	Netherl		
		Programmable Interrupt Priority Encoder Method & Apparatus	France		
2,07 2,720		Programmable Interrupt Priority Encoder Method & Apparatus	Canada	06/29/92	
98101193.6	HK1002145	Programmable Interrupt Priority Encoder Method & Apparatus	HK	07/31/98	06/22/12
04-231595		Programmable Interrupt Priority Encoder Method & Apparatus	Japan		
898,157	5,475,860	Input/Output Control system and Method for Direct Memory Transfer According to Location Addresses Provided by the Source Unit and Destination Addresses Provided by the Destination Unit (as amended)	USA	12/12/95	06/15/12
2098350		Improved IO Control System and Method	CANADA		
931095533	0578013	Improved IO Control System and Method	EPO	03/18/98	
	69317481.1	Improved IO Control System and Method	Germany		
	0578013	Improved IO Control System and Method	France		
	0578013	Improved IO Control System and Method	U. K.		
	0578013	Improved IO Control System and Method	Netherlands		
723,065	5,220,668	Digital Processor w/maintenance & Diagnostic System	USA	06/15/93	06/28/11
882,474	5,423,024	Fault tolerant Processing Section with Dynamically reconfigurable voting	USA	06/06/95	05/13/12
2068048		Fault tolerant Processing Section with Dynamically	Canada		
4-142228		Dynamically reconfigurable voting	Japan		
34,145	5,390,081	Fault-tolerant Power Distribution Apparatus	USA	07/14/95	03/22/13
23,346	5,367,668	Method & Apparatus for Fault-Detection	USA	11/22/94	02/26/13
309,210	5,630,056	Digital Data Processing methods and Apparatus for Fault Detection and Fault Tolerance	USA	05/13/97	09/20/14
759,099	5,838,900	Digital Data Processing methods and Apparatus for Fault Detection and Fault Tolerance	USA	11/17/98	12/03/16
297,795	5,479,648	Method and Apparatus for Switching Clock Signals in a Fault-Tolerant Computer System	USA	12/26/95	12/26/12
08/356,561	5,586,253	Method and Apparatus for Validating I/O Addresses in a Fault-Tolerant Computer System	USA	12/17/96	12/21/14
360,414	5,555,372	Fault-Tolerant Computer System Employing an Improved Error-Broadcast Mechanism	USA	09/10/96	12/21/14

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
08/565,145	5,802,265	Transparent Fault tolerant Computer System	USA	09/01/98	12/01/15
PCT/US96/18584		Transparent Fault tolerant Computer System	PCT		
09/116,770		Transparent Fault tolerant Computer System	USA		
710,135	5,781,910	System & Method For Performing Concurrent transactions in a replicated database environment	USA	07/14/98	09/13/16
09/069,025		Circuit Board Chasis	USA		
09/069,026		Circuit Board Chasis	USA		
08/514,196	5,625,681	Method and Apparatus for Telephone Number Portability	USA	04/29/97	08/11/15
95-304733.9		Method and Apparatus for Switching Clock Signals in a Fault Tolerant Computer System	Europe		
95305981.3		Digital Data Processing Methods and Apparatus for Fault Detection and Fault Tolerance	EPO		
08/366,414	5,559,459	Clock Signal Generation Arrangement Including Digital Noise Reduction Circuit for Reducing noise in a Digital Clocking Signal	USA	09/24/96	12/29/14
08/546,347	5,694,541	System Console Terminal for Fault Tolerant Computer System	USA	12/02/97	10/20/15
08/546,234	5,815,649	Distributed Fault Tolerant Digital Data Storage Subsystem for Fault Tolerant Computer System	USA	09/29/98	10/20/15
658,563	5,838,899	Digital Data Processing Methods and Apparatus for Fault Isolation	USA	11/17/98	06/05/06
57/169959	2122979	Digital Data Processing w/Fault Tolerant Bus Protocol	Japan	12/20/96	09/30/02
PCT/US96/09781		Digital Data Processing Methods and Apparatus for Fault Isolation	AU, CA, JP, EPO		
		EMI Cabinet with Improved Inteerference Suppression	*Canada*		
		Hierarchical Memory Management Apparatus & Method	*USA*		
		Fault-Tolerant UNIX-Type Digital Data Processing Method Apparatus	*USA*		
		I/O Controller Apparatus & Method for Transferring Data between a Host Processor & Multiple I/O Units	*Japan*		
18310192		*Programmable Interrupt Priority Encoder Method & Apparatus*	*AU*		
		Dynamically reconfigurable voting	*EPO*		
		Computer Apparatus and Method for Digital Processing Systems	*US*		
		Method and Apparatus for Digital Data Back-	*USA*		

APPLICATION/ SERIAL NO.	PAT NO	DESCRIPTION	COUNTRY	ISSUED	EXPIRES
		up Controller			
		Computer Apparatus and Method for Output Comparison	*USA*		
		Apparatus & Method for a Set Assoc. Shared Cache Memory	*USA*		
		Write back and Read Replacement Stratus Tracking with Snoop Detection	*USA*		
		Computer Method and Apparatus for Atomic Operation	*USA*		
		Computer Apparatus and Method for Block Transfer	*USA*		
		Power Surge Protection Method & Apparatus for Replaceable Electronic Devices			