

RECORDATION FORM COVER SHEET
PATENTS ONLY

U.S. DEPARTMENT OF COMMERCE

U.S. Patent And Trademark Office

To the Honorable Commissioner For Patents: Please record the attached original documents or copy thereof:

1. Name of conveying party(ies):

JP Morgan Chase Bank, N.A. (formerly The Chase
Manhattan Bank)

Additional name(s) of conveying party(ies) attached?

☐ Yes☒ No

3. Nature of Conveyance:

☐ Assignment☐ Merger☐ Security Agreement☐ Change of Name☒ Other: Release of Security InterestExecution Date: May 12, 2006

2. Name and address of receiving party(ies):

Name: Lexar Media, Inc.

Internal Address:

Street Address: 47421 Bayside ParkwayCity: FremontState: CA Zip: 94538

Additional name(s) & address(es) attached?

☐ Yes☒ No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: _____

A. Patent Application No.(s):

See attached

B. Patent No.(s):

See attachedAdditional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: John T. McNelisInternal Address: Fenwick & West LLPStreet Address: Silicon Valley Center
801 California StreetCity: Mountain View State: CA Zip Code: 940416. Total number of applications and patents involved: 587. Total fee (37 CFR 3.41): \$2,320.00☐ Check Enclosed☐ Fee Transmittal Enclosed☒ Charge the indicated fees to the below mentioned
deposit account.8. Deposit Account No.: 19-2555

DO NOT USE THIS SPACE

9. Statement and signature:

*To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.*John T. McNelis, Reg. No. 37,186

Name of Person Signing

Signature

Date

Total number of pages including cover sheet, attachments, documents: 21Mail documents to be recorded with required cover sheet information to: Mail Stop Assignment Recordation Services, Director of the U.S. Patent and Trademark Office, P.O. Box 1450,
Alexandria, VA 22313-1450.Case Docket No.: 21165-00023

700264351

PATENT 21165/01000/DOCS/1623107.1
REEL: 017626 FRAME: 0820

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Name of Conveying party (ies):

JP Morgan Chase Bank, N.A. (formerly The Chase Manhattan Bank)

Name and Addresses of receiving party(ies):

Lexar Media, Inc.

47421 Bayside Parkway

Fremont, CA 94538

Nature of Conveyance:

Release of Security Interest

Application Numbers:**Issued Patents:**

5,388,083

5,479,638

5,485,595

5,596,526

5,606,660

5,818,350

5,818,781

5,835,935

5,838,614

5,845,313

5,907,856

5,924,113

5,928,370

5,930,815

5,953,737

6,018,265

6,034,897

6,040,997

6,041,001

6,076,137

6,081,878

6,084,483

6,115,785

6,122,195

6,125,435

6,128,695

6,145,051

6,182,162

6,202,138

6,374,337

6,385,667

6,411,546

Continued**RECORDATION FORM COVER SHEET
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To the Honorable Commissioner For Patents: Please record the attached original documents or copy thereof:

Name of Conveying party (ies):

JP Morgan Chase Bank, N.A. (formerly The Chase Manhattan Bank)

Name and Addresses of receiving party(ies):

Lexar Media, Inc.

47421 Bayside Parkway

Fremont, CA 94538

Nature of Conveyance:

Release of Security Interest

Pending Applications:

09/520,905

09/565,517 now issued as 6,411,546

08/988,844 now issued as 6,076,137

09/264,340 now issued as 6,145,051

09/156,951 now issued as 6,128,695

60/108,872

09/440,986 now issued as 6,374,337

08/976,557 now issued as 6,125,435

09/030,697 now issued as 6,081,878

09/487,865 now issued as 6,202,138

09/311,202

09/311,045 now issued as 6,115,785

09/265,192 now issued as 6,084,483

09/330,278 now issued as 6,122,195

60/146,451

09/034,173 now issued as 6,182,162

09/234,430 now issued as 6,385,667

Foreign Applications:

PCT/US98/06335

PCT/US96/05107

PCT/US98/21107

PCT/US98/25342

PCT/US98/26307

PCT/US98/04247

PCT/US99/15259

PCT/US99/04634

PCT/US99/04633

RELEASE OF SECURITY INTEREST AGREEMENT

This Release of Security Interest Agreement ("**Agreement**") is made and entered into as of the date set forth below between Lexar Media, Inc. ("**Lexar**") and JPMorgan Chase Bank, N.A. (formerly known as The Chase Manhattan Bank) (the "**Bank**"). Lexar and the Bank are sometimes referred to in this Agreement, individually, as a "party" and, collectively, as the "parties."

RECITALS

A. Lexar, as Borrower, and the Bank, as Administrative Agent, entered into a Guarantee and Collateral Agreement dated June 30, 2000 ("**Collateral Agreement**").

B. The parties now wish to terminate and release any and all security interests to any of Lexar's intangible property and intellectual property granted pursuant to the Collateral Agreement.

NOW THEREFORE, in consideration of the mutual covenants set forth herein, the parties hereby agree as follows:

1. Termination and Release of Security Interest. The parties agree and acknowledge that the Bank no longer claims and hereby terminates any and all security interests it had or may have had in any of Lexar's intangible property or intellectual property granted pursuant to the Collateral Agreement, including without limitation, the intangible property and intellectual property set forth in **Exhibit A**. Without limiting the generality of the preceding sentence, the Bank hereby terminates any and all security interests in the patents and patent applications listed in **Exhibit A** to this Agreement ("**Exhibit A Patents**") in addition to (a) all provisional, utility, divisional, continuation, substitute, renewal, reissue, and other applications related thereto which have been or may be filed in the United States or elsewhere in the world; (b) all patents (including reissues and re-examinations) which may be granted on the Exhibit A Patents and the applications set forth in (a) above; and (c) all right of priority in the Exhibit A Patents and in any underlying provisional or foreign application, together with all rights to recover damages for infringement of provisional rights.

2. General Provisions. On a continuing basis, each party shall take any and all such reasonable action (including, without limitation, execution of agreements, affidavits or other documents) at the expense of the Borrower to give effect to, perfect or carry out the intent and purpose of the parties as specified in this Agreement. This Agreement will bind and inure to the benefit of each Party's permitted successors and assigns. Neither party may assign this Agreement, in whole or in part, without the other party's prior written consent. Any attempt to assign this Agreement in violation of this Section will be null and void. This Agreement will be governed by and construed in accordance with the substantive laws of the State of New York without regard to or application of provisions relating to conflicts of law. The captions to sections of this Agreement have been inserted for identification and reference purposes only and

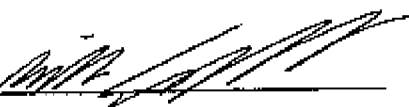
21165/00023/DOCS/1606375.2
444511:v2

shall not be used to construe or interpret this Agreement. This Agreement may be executed in counterparts, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument. This Agreement constitutes the complete and entire agreement and understanding between the parties and supersedes all prior and contemporaneous agreements, understandings and memoranda, written or oral, between the parties concerning the subject matter hereof. No amendments or supplements to this Agreement will be effective for any purpose except by a written agreement signed by both parties. If any provision of this Agreement is found invalid or unenforceable, that provision will be enforced to the maximum extent permissible so as to effect the intent of the parties and the remainder of this Agreement will remain in full force and effect, provided however, that if the invalidation or unenforceability of a provision frustrates the intent of the parties, the parties shall take any and all reasonable further action (at Borrower's expense) to carry out the intent of the parties and purposes of this Agreement. Failure by either party, at any time, to require performance by the other party or to claim a breach of any provision of this Agreement will not be construed as a waiver of any right accruing under this Agreement, nor will it affect any breach or the effectiveness of this Agreement or any part hereof, or prejudice either party with respect to any action. A waiver of any right accruing to either party pursuant to this Agreement will not be effective unless given in writing. Each Party hereby waives, to the fullest extent permitted by applicable law, any right it may have to a trial by jury in any legal proceeding directly or indirectly arising out of or relating to this Agreement.

IN WITNESS WHEREOF, Lexar and the Bank have caused this Release of Security Interest Agreement to be executed by their duly authorized representatives and to be effective as of the date last entered below (the "*Effective Date*").

LEXAR MEDIA, INC.

JPMORGAN CHASE BANK, N.A.

By: 
Title: CFO
Date: 5-12-06


Name: 
Title: Tracey Navin Ewing
Vice President
Date: _____

Exhibit A

COPYRIGHTS

The Company has no registered copyrights

PATENTS

The Company has supplementally provided schedules listing the Company's patents and patent applications as of June 21, 2000. Such schedules are hereby incorporated by reference herein.

TRADEMARKS AND TRADENAMES

Japan Pending Applications:

1. Japan -- JUMPSHOT (App. No. 11-87713) in Class 9 filed 9/27/99
2. Japan -- JUMPSHOT & DESIGN (App. No. 11-87714) in Class 9 filed 9/27/99
3. Japan -- LEXAR MEDIA & DESIGN (App. No. 11-5289) in Class 9 filed 1/21/99

United States Pending Applications and Registration:

1. MICELLANEOUS DESIGN (FILM LOGO) (Reg. No. 2,273,926) Registered
2. LEXAR MEDIA & DESIGN (Reg. No. 2,295,266) Registered
3. LEXAR MEDIA & DESIGN (Ser. No. 75/622,308) Pending
4. JUMPSHOT & DESIGN (Ser. No. 75/791,829) Pending
5. JUMPSHOT (Ser. No. 75/738,455) Pending
6. DIGITAL PHOTO FINISHER (Ser. No. 75/497,377) Pending

21165/00017/DOCS/1061090.1

LICENSES

1. Lexar entered into a Software Assignment Agreement with Cirrus Logic ("Cirrus") dated as of December 9, 1996 pursuant to which Lexar agreed to assign certain software to the Company and pay administrative fees to Lexar for such assignment.

2. Lexar entered a Software License Agreement and a Software Maintenance Agreement with Cadence Design Systems on October 22, 1996. Lexar also entered into an Electronic Transmission Agreement with Cadence on December 30, 1999. These Agreements automatically renew for 1-year terms unless terminated by either party with 30 days written notice. /d/

3. Lexar entered into a Development License Agreement with Hitachi Ltd., a Japanese corporation dated as of November 7, 1996 for the term of five years.

4. Lexar entered into a License and Sublicense Agreement with CompactFlash Association, a California non-profit corporation dated as of October 7, 1997.

5. Lexar entered into a Cross License Agreement dated as of September 18, 1996 with Cirrus Logic, Inc. and Cirrus Logic International, Ltd. (the Cirrus Agreement). Pursuant to the Cirrus Agreement, Lexar granted a license to the patents acquired from the Cirrus Logic Entities back to the Cirrus Logic Entities. In addition, the Cirrus Logic Entities granted Lexar a worldwide, perpetual, non-exclusive, royalty-free license with the right to sublicense with respect to certain Cirrus patents to Flash Memory Products (as defined therein). Except with respect to Flash Memory Products, Lexar and each of its Affiliates agree that they will not for a period of four years from the Effective Date utilize any of the Transferred Patents in connection with the design, manufacture, use or sale of any products which are or compete with magnetic or CDROM storage applications.

6. Lexar entered into a Software Licensing Agreement with Arcsoft on December 8, 1996. Either party has the right to terminate this Agreement immediately, upon notice of the other.

7. Lexar entered into a Software Maintenance Agreement with Viewlogic Systems, Inc. dated as of June 30, 1998 for the term of one year and automatically renews for one year periods.

8. Lexar entered into a Software License Agreement with Sterling Commerce dated February 17, 1999. The term of this agreement shall automatically renew on an annual basis unless terminated.

9. Lexar entered into an Intellectual Property Licensing Agreement with Stargate Solutions, Inc. on August 4, 1999. The term of this agreement shall automatically renew on an annual basis unless terminated.

21165/00017/DOCS/1061090.1

10. Lexar entered into a Development Agreement with Stargate Solutions, Inc. on February 22, 1999. Lexar may terminate this Agreement at any time, upon 15 days written notice.

11. Lexar entered into a SONY Technology License Agreement and a Lexar Technology License Agreement with SONY Corporation on March 21, 2000. The term of these Agreements runs indefinitely.

21165/00017/DOCS/1061090.1



Patent
Status Report
 As of 6/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0001	US		Allowed	08/958,844	12/11/97		
Title: A Method and Apparatus for Storing Location Identification Information within Non-Volatile Memory Devices							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0001 CPA	US		Filed		5/26/00		
Title: A Method and Apparatus for Storing Location Identification Information within Non-Volatile Memory Devices							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0002	US		Granted	08/509,706	7/31/95	5,845,313	12/1/98
Title: Direct Logical Block Addressing Flash Memory Mass Storage Architecture							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0003	US	1	Granted	08/748,887	11/13/96	5,818,781	10/6/98
Title: Automatic Voltage Detection in Multiple Voltage Applications							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0003EP	European Patent Off.		Pending	95941337.6	11/13/96		
Title: Automatic Voltage Detection in Multiple Voltage Applications							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0003JP	Japan		Pending	820605/97	11/13/96		
Title: Automatic Voltage Detection in Multiple Voltage Applications							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0010US	US		Granted	08/527,454	9/13/95	5,835,836	11/10/98
Title: Method of An Architecture for Controlling System Data with Automatic Wear Leveling in a Semiconductor Non-Volatile Mass Storage Memory							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							
38979-0010JP	Japan		Pending	812147/97	9/12/96		
Title: Method of An Architecture for Controlling System Data with Automatic Wear Leveling in a Semiconductor Non-Volatile Mass Storage Memory							
Remarks: Respectively, the first and second memory devices are connected to a common data bus and a common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus. The first memory device is connected to the common data bus and the common address bus. The second memory device is connected to the common data bus and the common address bus.							



Patent
Status Report
As of 6/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0011US	US		Granted	05/531,266	3/31/97	5,907,856	5/26/99
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0011G1	US	G1	Pending	09/264,340	3/8/99		
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0011PCT	Patent Cooperation Treaty		Published	US98/06335	3/31/98		
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0011EP	Europe		Pending	98914371.4	10/28/99		
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0011KR	Korea		Pending	10-1999-7008898	9/29/99		
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0011JP	Japan		Pending	10-541928	10/22/99; Int'l 3/31/98		
Title: Moving Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0014	US		Granted	05/558,847	5/19/97	5,838,614	11/17/98
Title: Identification and Verification of a Sector within a Block of Mass Storage Flash Memory							
Remarks: [REDACTED]							



**Patent
Status Report
As of 6/15/00**

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0014B	US	Con	Allowed	08/158,951	9/18/98		
Title: Identification and Verification of a Sector Within a Block of Mass Storage Flash Memory							
Remarks: [REDACTED]							
38979-14CPA	US						
Title: Identification and Verification of a Sector Within a Block of Mass Storage Flash Memory							
Remarks: [REDACTED]							
38979-0017CA	Canada		Pending	2,161,315	3/23/94		
Title: Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0019	US		Granted	08/037,893	3/28/93	5,479,638	12/28/95
Title: Flash Memory Mass Storage Architecture Incorporating Wear Leveling Techniques							
Remarks: [REDACTED]							
38979-0021CA	Canada		Pending	2,161,344	3/23/94		
Title: Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0022EP	European Patent Off		Pending	94912854.0	3/23/94		
Title: Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0023	US		Granted	08/131,495	10/4/93	5,485,595	1/16/98
Title: Flash Memory Mass Storage Architecture Incorporating Wear Leveling Technique Without Using CAM Cells							
Remarks: [REDACTED]							
38979-0025EP	European Patent Off		Pending	94928189.3	9/23/94		
Title: Flash Memory Mass Storage Architecture Using Less Data Storage							
Remarks: [REDACTED]							
38979-0027	US		Granted	08/328,584	10/21/94	5,608,550	2/25/97
Title: Method and Apparatus for Combining Controller Firmware Storage and Controller Logic in a Mass Storage System							
Remarks: [REDACTED]							



**Patent
Status Report
As of 6/15/00**

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0028	US		Granted	08/420,239	4/11/95	5,818,350	10/8/98
Title: High Performance Method of and System for Selecting One of a Plurality of IC Chips While Requiring Minimal Select Lines							
Remarks: [REDACTED]							
38979-0030IS	Israel		Pending	117681	4/11/96		
Title: High Performance Method of and System for Selecting One of a Plurality of IC Chips While Requiring Minimal Select Lines							
Remarks: [REDACTED]							
38979-0031	US		Granted	08/515,188	8/15/95	5,595,526	1/21/97
Title: Non-Volatile Memory System of Multi-Level Transistor Cells and Methods Using Same							
Remarks: [REDACTED]							
38979-0032JP	Japan		Pending	509467/97	8/14/96		
Title: Multi-Level Non-Volatile Data Storage							
Remarks: [REDACTED]							
38979-0032KR	Korea, South		Pending	701130/1998	8/14/98		
Title: Multi-Level Non-Volatile Data Storage							
Remarks: [REDACTED]							
38979-0033	US		Granted	08/795,072	2/5/97	5,925,370	7/27/99
Title: Method and Apparatus for Verifying Erasure of Memory Blocks within a Non-Volatile Memory Structure							
Remarks: [REDACTED]							
38979-0034P2	US	P2	Converted	60/108,872	11/17/95		
Title: Flash Memory Circuit							
Remarks: [REDACTED]							
38979-0034	US		Pending	09/440,986	11/16/99		
Title: Flash Memory Circuit							
Remarks: [REDACTED]							
38979-0034PCT	Patent Cooperation Treaty		Pending		11/16/99		
Title: Flash Memory Circuit							
Remarks: [REDACTED]							



Patent Status Report As of 6/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0035	US		Granted	08/946,331	10/7/97	5,930,815	7/27/99
Title: Moving Sequential Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0036PCT	Patent Cooperation Treaty		Published	US98/21107	10/6/98		
Title: Moving Sequential Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0035EP			Pending	98559353.7	5/10/00		
Title: Moving Sequential Sectors within a Block of Information in a Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0038	US		Pending/ File FWC/ Abandoned (see 38979-38CPA)	08/976,557	11/24/97		
Title: Alignment of Cluster Address to Block Addresses within a Semiconductor Non-Volatile Mass Storage Memory							
Remarks: [REDACTED]							
38979-0038CPA	US		Pending	08/976,557	12/14/99		
Title: Alignment of Cluster Address to Block Addresses within a Semiconductor Non-Volatile Mass Storage Memory							
Remarks: [REDACTED]							
38979-38CPA2	US		Pending	08/520,905	3/7/00		
Title: Alignment of Cluster Address to Block Addresses within A Semiconductor Non-Volatile Mass Storage Memory							
Remarks: [REDACTED]							
38979-0038PCT	Patent Cooperation Treaty		Published	US98/25342	11/24/98		
Title: Alignment of Cluster Address to Block Addresses within a Semiconductor Non-Volatile Mass Storage Memory							
Remarks: [REDACTED]							



**Patent
Status Report
As of 6/15/00**

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0039	US	1	Granted	08/052,038	3/30/98	6,018,265	1/25/00
Title: Internal CMOS Reference Generator and Voltage Regulator							
Remarks: [REDACTED]							
38979-0039PCT	Patent Cooperation Treaty		Pending	US98/26307	12/10/98		
Title: Internal CMOS Reference Generator and Voltage Regulator							
Remarks: [REDACTED]							
38979-0041	US		Pending	09/042,427	2/25/99		
Title: Increasing Memory Performance in Flash Memory Devices by Performing Simultaneous Write Operation to Multiple Devices							
Remarks: [REDACTED]							
38979-0041CPA	US		Pending	09/047,665	1/26/00		
Title: Increasing The Memory Performance of Flash Memory Devices By Writing Sectors Simultaneously to Multiple Flash Memory Devices							
Remarks: [REDACTED]							
38979-0041CPA2	US		Pending				
Title: Increasing the Memory Performance of Flash Memory Devices by Writing Sectors Simultaneously to Multiple Flash Memory Devices							
Remarks: [REDACTED]							
38979-0041PCT	Patent Cooperation Treaty		Pending	US99/04247	2/25/99		
Title: Increasing Memory Performance in Flash Memory Devices by Performing Simultaneous Write Operation to Multiple Devices							
Remarks: [REDACTED]							
38979-41EP	Europe		Pending				
38979-41JP	Japan		Pending				
38979-0047	US		Granted	08/111,414	7/7/98	5,953,737	9/14/98
Title: Method and Apparatus for Performing Erase Operations Transparent to a Solid State Storage System							
Remarks: [REDACTED]							



Patent
Status Report
As of 5/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0047C1	US	C1	Pending	09/311,202	5/12/99		
Title: Method and Apparatus for Performing Erase Operations Transparent to a Solid State Storage System							
Remarks: [REDACTED]							
38979-0047PCT	Patent Cooperation Treaty		Pending	US99/15259	7/6/99		
Title: Method and Apparatus for Performing Erase Operations Transparent to a Solid State Storage System							
Remarks: [REDACTED]							
38979-0057	US		Granted	08/038,868	3/28/93	5,358,083	2/7/95
Title: Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0058C1	US	C1	Granted	09/057,720	5/29/98	5,924,113	7/13/99
Title: Direct Logical Block Addressing Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0058C2	US	C2	Pending	09/311,045	5/13/99		
Title: Direct Logical Block Addressing Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-58CPA	US		Allowed				
Title: Direct Logical Block Addressing Flash Memory Mass Storage Architecture							
Remarks: [REDACTED]							
38979-0050	US		Allowed	09/265,192	3/10/99		
Title: Internal Oscillator							
Remarks: [REDACTED]							



Patent
Status Report
As of 6/16/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0085	US		Allowed	00/283,728	4/1/00	6,034,897	3/7/00
Title: Space Management for Managing High Capacity Non-Volatile Memory							
Remarks: [REDACTED]							
38979-65CPA	US		Pending		3/6/00		
Title: Space Management for Managing High Capacity Non-Volatile Memory							
Remarks: [REDACTED]							
38979-66PCT			Pending				
Title: Space Management for Managing High Capacity Non-Volatile Memory							
Remarks: [REDACTED]							
38979-0069	-US		Pending	00/330,278	6/11/00		
Title: Method and Apparatus for Decreasing Block Write Operation Times Performed on Non-Volatile Memory							
Remarks: [REDACTED]							
38979-68CPA	US						
Title: Method and Apparatus for Decreasing Block Write Operation Times Performed on Non-Volatile Memory							
Remarks: [REDACTED]							
38979-66PCT			Unfiled				
Title: Method and Apparatus for Decreasing Block Write Operation Times Performed on Non-Volatile Memory							
Remarks: [REDACTED]							
38979-0069	US	revisions	Pending	60/146,451	7/29/99		
Title: Removable Data Storage Module Incorporating a Display							
Remarks: [REDACTED]							
38979-0070	US		Unfiled				
Title: Method and Apparatus for Maintaining Track of Status of Blocks within Non-Volatile Memory in a Separate Location for Increasing System							
Remarks: [REDACTED]							
38979-0071	US		Pending		2/8/00		
Title: Enhanced Compact Flash Memory Card							
Remarks: [REDACTED]							

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Patent
Status Report
As of 5/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
38979-0072	US		Pending		9/3/00		
Title: Organization of Blocks Within a Non-Volatile Memory Unit to Effectively Decrease Sector Write Operation Time							
Remarks: [REDACTED]							
38979-0073	US		Unfiled				
Title: Audio Cassette for Storage and Delivery of Digital Audio							
Remarks: [REDACTED]							
38979-0074	US		Unfiled				
Title: Fast Electronic Image Transfer							
Remarks: [REDACTED]							
38979-0075	US		Pending	09/555,517	5/5/00		
Title: Nonvolatile Memory Device Using Flexible Erasing Methods and Method and System for Using Same							
Remarks: [REDACTED]							
LEXA-00100	US		Granted	09/047,798	3/25/98	6,040,997	
Title: Flash Memory Leveling Architecture Having No External Latch							
Remarks: [REDACTED]							
LEXA-00101EP	European Patent Application			99 915 037.8			
Title: Flash Memory Leveling Architecture Having No External Latch							
Remarks: [REDACTED]							
LEXA-00101GB	United Kingdom Patent Application						
Title: Flash Memory Leveling Architecture Having No External Latch							
Remarks: [REDACTED]							
LEXA-00101JP	Japanese Patent Application						
Title: Flash Memory Leveling Architecture Having No External Latch							
Remarks: [REDACTED]							
LEXA-00200	US		Pending	09/034,173	3/2/00		
Title: Improved Compact Flash Memory Card and Interface							
Remarks: [REDACTED]							



Patent
Status Report
As of 6/15/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
LEXA-00201	CIP		Pending	09/234,430	1/20/99		
Title: Flash Memory Card with Enhanced Operating Mode Detection and User-Friendly Interfacing System							
Remarks: [REDACTED]							
LEXA-00202			Closed	PCT/US/99/04634			
Title: Improved Compact Flash Memory Card and Interface							
Remarks: [REDACTED]							
LEXA-00202DE	German Patent Application			199 80 546.8			
Title: Improved Compact Flash Memory Card and Interface							
Remarks: [REDACTED]							
LEXA-00202GB	United Kingdom			9925229.8			
Title: Improved Compact Flash Memory Card and Interface							
Remarks: [REDACTED]							
LEXA-00202JP	Japanese Patent Application						
Title: Improved Compact Flash Memory Card and Interface							
Remarks: [REDACTED]							
LEXA-00203			Closed	PCT/US99/04633			
Title: Flash Memory Card with Enhanced Operating Mode Detection and User-Friendly Interfacing System							
Remarks: [REDACTED]							
LEXA-00203DE	German Patent Application			199 80 546.8			
Title: Flash Memory Card with Enhanced Operating Mode Detection and User-Friendly Interfacing System							
Remarks: [REDACTED]							
LEXA-00203GB	United Kingdom			9925231.4			
Title: Flash Memory Card with Enhanced Operating Mode Detection and User-Friendly Interfacing System							
Remarks: [REDACTED]							
LEXA-00203JP	Japanese Patent Application						
Title: Flash Memory Card with Enhanced Operating Mode Detection and User-Friendly Interfacing System							
Remarks: [REDACTED]							



Patent
Status Report
As of 6/16/00

Case Number	Country	SubCase	Status	Appl Number	Filing Date	Patent #	Issue Date
LEXA-00300	US						
Title: Flash Memory Architecture Implementing LBA to PBA Correlation within Flash Memory Array							
Remarks: [REDACTED]							
LEXA-00301	CIP						
Title: Flash Memory Architecture Implementing LBA to PBA Correlation within Flash Memory Array							
Remarks: [REDACTED]							
LEXA-00400	US		Granted	09/255,163	2/25/99	6,041,001	
Title: Method of Increasing Data Reliability of a Flash Memory Device without Compromising Compatibility							
Remarks: [REDACTED]							
LEXA-00500	US						
Title: Output Driver with Self Adjusting Output Drive Capacity							
Remarks: [REDACTED]							
LEXA-00600	US						
Title: Integrated Circuit Having On-Board Clock Calibration Circuit Tunable During Manufacturing							
Remarks: [REDACTED]							
LEXA-00700							
Title: Infringement Opinion Re: U.S. Patent # 5,602,967							
Remarks: [REDACTED]							
LEXA-00800	US						
Title: Flash Memory Architecture having Separate Wells for Data and Overhead							
Remarks: [REDACTED]							
LEXA-00900	US						
Title: Simultaneously Programming Multiple Memory Banks							
Remarks: [REDACTED]							

Appendix to Chase Release

Issued Patents:

5,388,083

5,479,638

5,485,595

5,596,526

5,606,660

5,818,350

5,818,781

5,835,935

5,838,614

5,845,313

5,907,856

5,924,113

5,928,370

5,930,815

5,953,737

6,018,265

6,034,897

6,040,997

6,041,001

6,076,137

6,081,878

6,084,483

6,115,785

6,122,195

6,125,435

6,128,695

6,145,051

6,182,162

6,202,138

6,374,337

6,385,667

6,411,546

Z1165/00023/DOCS/1606096.1

Pending Applications:

09/520,905

09/565,517 now issued as 6,411,546

08/988,844 now issued as 6,076,137

09/264,340 now issued as 6,145,051

09/156,951 now issued as 6,128,695

60/108,872

09/440,986 now issued as 6,374,337

08/976,557 now issued as 6,125,435

09/030,697 now issued as 6,081,878

09/487,865 now issued as 6,202,138

09/311,202

09/311,045 now issued as 6,115,785

09/265,192 now issued as 6,084,483

09/330,278 now issued as 6,122,195

60/146,451

09/034,173 now issued as 6,182,162

09/234,430 now issued as 6,385,667

Foreign Applications:

PCT/US98/06335

PCT/US96/05107

PCT/US98/21107

PCT/US98/25342

PCT/US98/26307

PCT/US98/04247

PCT/US99/15259

PCT/US99/04634

PCT/US99/04633

21165/00023/DOC'S/1606096.1