Form PTO-1595 (Rev. 07/05)
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United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

VeriSilicon Holdings (Cayman Islands) Co., Ltd.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: LSI Logic Corporation
Internal Address: MS AD-106
Street Address: 1621 Barber Lane
City: Milpitas
State: California
Country: USA Zip: 95035

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s)

☐ Assignment ☐ Merger
☑ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)	B. Patent No.(s)
5,966,529 08/440,993	5,900,025 08/528,509

Additional numbers attached? ☑ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Andrew Hughes, Esq.
Internal Address: LSI Logic Corporation, MS AD-106
Street Address: 1621 Barber Lane
City: Milpitas
State: California Zip: 95035
Phone Number: 408 954 3108
Fax Number: 408 433 7770
Email Address: andrew.hughes@lsil.com

6. Total number of applications and patents involved: 52

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged by credit card
☑ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number 50-3420
Authorized User Name Kevin O'Brien

9. Signature:

Signature 7-7-06 Date

Deborah L. Fields, Corporate Paralegal, Baker & McKenzie LLP
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 13

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CH $2040.00 503420 08440993

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4. Application or Patent Number(s)

A. Patent Applications

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
1	09/993,114		Mechanism and Method For Conditionally Executing Instructions and Digital Signal Processor Incorporating The Same	11/5/2001	
2	10/002,817	7,013,382	Mechanism And Method For Reducing Pipeline Stalls Between Nested Calls and Digital Signal Processor Incorporating The Same	11/2/2001	3/14/2006
3	10/007,498		Pipelined Multiply-Accumulate Unit and Out-Of-Order Completion Logic For A Superscalar Digital Signal Processor And Method Of Operation Thereof	11/13/2001	
4	10/066,147		Mechanism for Resource Allocation in a Digital Signal Processor and Method of Operation Thereof	10/26/2001	
5	10/066,150		A Method For Instruction Prefetch In A Four-Way Superscalar Harvard Architecture DSP With A Small Direct-Mapped Instruction Cache	10/26/2001	
6	10/231,948		System and Method for Conditionally Executing Software Program Instructions	8/30/2002	
7	10/256,410	7,020,765	System and Method for Simultaneously Executing Multiple Conditional Execution Instruction Groups	9/27/2002	3/28/2006
8	10/256,864		System And Method For Conditionally Executing An Instruction Dependent On A Previously Existing Condition	9/27/2002	
9	10/262,414		System and Method For Selectively Updating Pointers Used In Conditionally Executed Load/Store With Update Instructions	9/30/2002	
10	10/277,339		System, Circuit, and Method for Adjusting Prefetch Instruction Rate	10/22/2002	
11	10/279,344		In-Circuit Emulation Debugger and Method of Operation Thereof	10/24/2002	
12	10/299,532		Processor Having a Unified Register File with Multipurpose Registers for Storing Address and Data Register Values, and Associated Register Mapping Method	11/18/2002	
13	10/303,610		Method for Grouping Non-Interruptible Instructions Prior to Handling an Interrupt Request	11/25/2002	
14	10/396,265		System and Method for Evaluating and Efficiently Executing Conditional Instructions	3/25/2003	

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No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
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16	10/437,485		System and Method For Cooperative Operation Of A Processor And Coprocessor	5/14/2003	
17	10/603,303	7,051,146	Data Processing Systems including High-Performance Buses and Interfaces, and Associated Communication Methods	6/25/2003	5/23/2006
18	10/613,128		Processor and Method for Convolutional Decoding	7/3/2003	
19	10/844,941		Hardware Looping Mechanism and Method for Efficient Execution of Discontinuity Instructions	5/13/2004	
20	11/006,102		Four Issue Quad Load/Store Multiply-Accumulate Unit for a Digital Signal Processor and Method of Operation Thereof	12/7/2004	
21	11/081,424		Single-Issue Digital Signal Processor Architecture Having Backwards-Compatible Instruction Set and Method of Operation Thereof	3/16/2005	
22	11/083,575		DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONED DISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR	3/18/2005	
23	11/083,646		DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONEDDISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR	3/18/2005	
24	11/128,740		System and Method for Reducing the Addressable Memory Required to Execute a Computer Program	5/13/2005	
25	11/222,533		Branch Predictor For A Processor And Method Of Predicting A Conditional Branch	9/9/2005	
26	11/246,595		Processor Implementing Conditional Execution and Including a Serial Queue	10/7/2005	
27	11/273,679		System and Method for Simultaneously Executing Multiple Conditional Execution Instruction Groups	11/14/2005	
28	LSI Docket # 05-1230		Floating point data format for fast execution on fixed point processors		
29	LSI Docket # 05-1990		A Processor Independent Cache Management Mechanism		

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No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
30	LSI Docket # 05-2212		Floating Point Hardware Accelerator-Coprocessor for Fixed-Point Processors based on the ZSP Fast Floating Point Format (ZSPFF)		

B. (Issued) Patent Numbers

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
1	08/528,509	5,900,025	A processor having a hierarchical control register file and methods for operating the same	9/12/1995	5/4/1999
2	08/440,993	5,966,529	Auxiliary operand register file and complementary arrangements for non-disruptively performing adjunct execution by a processor having a virtually addresssable primary operand register file	5/15/1995	10/12/1999
3	08/845,817	5,987,603	An apparatus and method for reversing bits using a shifter	4/29/1997	11/16/1999
4	08/841,415	5,987,638	An Apparatus and method for computing the results of a viterbi equation in a single cycle	4/22/1997	11/16/1999
5	08/401,411	6,081,880	Processor having a scalable uni/multidimensional and virtually/physically addresses operand register file	3/9/1995	6/27/2000
6	09/036,403	6,260,112	Register Memory Linking	3/5/1998	7/10/2001
7	09/235,417	6,523,055	Circuit and method for multiplying and accumulating the sum of two products in a single cycle	1/20/1999	2/18/2003
8	09/467,939	6,622,154	Alternate Booth Partial Product Generation for a Hardware Multiplier	12/21/1999	9/16/2003
9	09/847,849	6,687,773	Bridge For Coupling Digital signal Processor To On-Chip Bus As Master	4/30/2001	2/3/2004
10	09/993,431	6,715,038	Efficient Memory Management Mechanism for Digital Signal Processor and Method of Operation Thereof	11/5/2001	3/30/2004
11	09/847,850	6,789,153	Using AMBA For Signal Processor Core Integration	4/30/2001	9/7/2004
12	10/028,698	6,813,704	Changing Instruction Order By Reassigning Only Tags In Order Tag Field In Instruction Queue	12/20/2001	11/2/2004
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14	09/924,178	6,889,318	Instruction Fusion For Digital Signal Processor	8/7/2001	5/3/2005
15	10/310,234	6,922,760	Distributed Result System for High-Performance Wide-Issue Superscalar Processor	12/5/2002	7/26/2005
16	10/701,775	6,956,788	Asynchronous Date Structure for Storing Data Generated by a DSP System	11/5/2003	10/18/2005

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No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
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19	09/901,455	6,963,961	Increasing DSP Efficiency by Independent Issuance of Store Address and Data	7/9/2001	11/8/2005
20	10/277,341	6,968,430	Circuit and Method for Improving Instruction Fetch Time from a Cache Memory Device	10/22/2002	11/22/2005
21	10/408,387	6,973,630	System and Method for Reference-Modeling a Processor	4/7/2003	12/6/2005
22	10/047,515	6,976,156	Pipeline Stall Reduction in Wide Issue Processor by Providing Mispredict PC Queue and Staging Registers to Track Branch Instructions in Pipeline	10/26/2001	12/13/2005

PATENT SECURITY AGREEMENT

This PATENT SECURITY AGREEMENT (this "Agreement"), dated as of June 30, 2006, is entered into between VeriSilicon Holdings (Cayman Islands) Co., Ltd., an exempted company with limited liability under the laws of the Cayman Islands ("Grantor"), which has a mailing address at P.O. Box 309 GT, Ugland House, South Church Street, Georgetown Grand Cayman, Cayman Islands, and LSI Logic Corporation, a Delaware Corporation ("Secured Party") having its principal office at 1621 Barber Lane, Milpitas, California, 95035.

RECITALS

A. Contemporaneously herewith, Grantor is executing and delivering that certain Secured Promissory Note, dated as of June 30, 2006 (the "Note"), in favor of Secured Party;

B. In connection with the Note, it is contemplated that Grantor and Secured Party are, contemporaneously herewith, entering into that certain Security Agreement, dated as of June 30, 2006 (the "Security Agreement"); and

C. In connection with the Security Agreement, it is contemplated that Grantor's obligations be secured, on and subject to the terms hereof, by a security interest in certain intellectual property, identified below.

NOW THEREFORE, the parties hereto mutually agree as follows:

1. GRANT OF SECURITY INTEREST.

To secure the complete and timely payment and performance of the Secured Obligations, as such term is defined in the Security Agreement, Grantor hereby grants, assigns, and conveys to Secured Party a security interest in all of Grantor's right, title, and interest in, to and under the following properties and assets owned or held by Grantor or in which Grantor otherwise has any interest, now existing or hereafter acquired or arising (the "Collateral"):

(i) all patents and applications therefor listed in Schedule A, and all reissues, divisions, renewals, extensions, provisionals, continuations and continuations-in-part thereof (collectively, the "Patents"), all licenses relating to any of the foregoing and all income and royalties with respect to any licenses, all rights to sue for past, present or future infringement thereof, all rights otherwise arising therefrom and pertaining thereto;

(ii) all books, records and other written, electronic or other documentation in whatever form maintained now or hereafter by or for Grantor or evidencing or containing information about the Collateral, including: (1) inventions disclosure materials and data, prosecution files and other documentation evidencing the Patents or claims hereunder or proceedings or actions in respect thereof, (2) all computer-prepared or electronically stored, collected or reported information comprising any of the foregoing and all media and equipment containing or necessary to access such information; and

(iii) all accounts, all commercial tort claims and all intangible property and other general intangibles in each case arising from any of the aforementioned properties and all proceeds of any of the property listed in paragraphs (i) through (iii).

2. GENERAL PROVISIONS.

2.1 Rights Under Security Agreement. This Agreement has been granted in conjunction with the security interest granted to Secured Party under the Security Agreement. The rights and remedies of Lender with respect to the security interests granted herein are without prejudice to, and are in addition to those set forth in the Security Agreement, all terms and provisions of which are incorporated herein by reference.

2.2 Binding Effect; Assignment. This Agreement shall be binding upon, inure to the benefit of and be enforceable by Grantor, Secured Party and their respective successors and assigns; provided, however, that Grantor may not assign this Agreement or any of its obligations or rights hereunder without the prior written consent of Secured Party. With or without Grantor's consent, Secured Party may assign this Agreement, its rights hereunder and to the Collateral and its obligations hereunder, in each case in whole or in part proportional to any concurrent assignment of its rights and interests in the Secured Obligations.

2.3 Amendment. This Agreement shall not be amended except by the written agreement of the parties.

2.4 Governing Law. THIS AGREEMENT SHALL BE CONSTRUED IN ACCORDANCE WITH AND GOVERNED BY THE INTERNAL LAWS OF THE STATE OF CALIFORNIA WITHOUT GIVING EFFECT TO ANY CHOICE OF LAW RULE THAT WOULD CAUSE THE APPLICATION OF THE LAWS OF ANY JURISDICTION OTHER THAN THE INTERNAL LAWS OF THE STATE OF CALIFORNIA. GRANTOR HEREBY IRREVOCABLY SUBMITS TO THE JURISDICTION AND VENUE OF ANY COURT WITHIN SANTA CLARA COUNTY, CALIFORNIA, AND AGREES THAT PROCESS MAY BE SERVED UPON IT IN ANY MANNER AUTHORIZED BY THE LAWS OF THE STATE OF CALIFORNIA, FOR PURPOSES OF RESOLVING ANY DISPUTES ARISING IN CONNECTION WITH THIS AGREEMENT, AND GRANTOR HEREBY WAIVES AND COVENANTS NOT TO ASSERT OR PLEAD ANY OBJECTION THAT IT MIGHT OTHERWISE HAVE TO SUCH JURISDICTION, VENUE OR PROCESS.

IN WITNESS WHEREOF, the parties have duly executed this Agreement as of the date first above written.

GRANTOR	SECURED PARTY
VeriSilicon Holdings (Cayman Islands) Co., Ltd.	LSI Logic Corporation
By: Wayne Dai	By:
Name: Wayne Dai	Name:
Title: President & CEO	Title

IN WITNESS WHEREOF, the parties have duly executed this Agreement as of the date first above written.

GRANTOR	**SECURED PARTY**
VeriSilicon Holdings (Cayman Islands) Co., Ltd.	LSI Logic Corporation
By:_____	By: Bryon Look
Name:	Name: Bryon Look
Title:	Title EVP & CFO

Schedule A

PATENTS

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
1	08/528,509	5,900,025	A processor having a hierarchical control register file and methods for operating the same	9/12/1995	5/4/1999
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4	08/841,415	5,987,638	An Apparatus and method for computing the results of a viterbi equation in a single cycle	4/22/1997	11/16/1999
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9	09/847,849	6,687,773	Bridge For Coupling Digital signal Processor To On-Chip Bus As Master	4/30/2001	2/3/2004
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19	09/901,455	6,963,961	Increasing DSP Efficiency by Independent Issuance of Store Address and Data	7/9/2001	11/8/2005
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22	10/047,515	6,976,156	Pipeline Stall Reduction in Wide Issue Processor by Providing Mispredict PC Queue and Staging Registers to Track Branch Instructions in Pipeline	10/26/2001	12/13/2005

PATENT APPLICATIONS

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			MULTIPLY/ACCUMULATE UNIT THEREFOR		
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27	11/273,679		System and Method for Simultaneously Executing Multiple Conditional Execution Instruction Groups	11/14/2005	
28	LSI Docket # 05-1230		Floating point data format for fast execution on fixed point processors		
29	LSI Docket # 05-1990		A Processor Independent Cache Management Mechanism		
30	LSI Docket # 05-2212		Floating Point Hardware Accelerator-Coprocessor for Fixed-Point Processors based on the ZSP Fast Floating Point Format (ZSPFF)		