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SUBMISSION TYPE:		NEW ASSIGNMENT				
NATURE OF CONVEYANCE:		ASSIGNMENT				
CONVEYING PARTY DA	ATA .					
Name Execution Date						
TimeLab Corporation		11/07/2	2006			
RECEIVING PARTY DAT	ΓΑ					
Name:	Itera Corporation					
Street Address: 10	01 Innovation Drive	9				
City:	City: San Jose					
Postal Code: 95	5134					
]			
Property Type		Number				
Patent Number:		7106115				
Application Number:	10964	10964777				
Application Number:	11044	11044336				
Application Number:	11044	11044315				
Application Number:	60543	60543041				
Application Number:	11052	11052926				
Application Number:	60642	60642505				
Application Number:	60683	60683789				
Application Number:	11326	11326423				
Application Number:	60644	60644024				
Application Number:	11332	290				
Application Number:		60677356				
Application Number:		11414225				
Application Number:		60690129				
Application Number: 6		0689543				
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Application Number:	60696	543			
Application Number:	60698	3940			
Application Number:	60807	60807768			
CORRESPONDENCE DA	ATA (301)762-4056				
	nce will be sent via US Mail when the fax attempt is unsuccessful.				
Phone:	301-424-3640				
Email:	epatent@usiplaw.com				
Correspondent Name:	D. Andrew Floam				
Address Line 1:	1901 Research Boulevard, Suite 400				
Address Line 4:	Rockville, MARYLAND 20850				
ATTORNEY DOCKET NU	ATTORNEY DOCKET NUMBER: 2053.0109M				

ATTORNEY DOCKET NUMBER:	2053.0109M	
NAME OF SUBMITTER:	D. Andrew Floam	
Total Attachments: 4 source=AssignmenttoAlterafromTimeLab#p source=AssignmenttoAlterafromTimeLab#p source=AssignmenttoAlterafromTimeLab#p source=AssignmenttoAlterafromTimeLab#p	age2.tif age3.tif	

EXHIBIT 3.02(b)

PATENT ASSIGNMENT

ASSIGNMENT AND TRANSFER OF PATENTS

WHEREAS, TimeLab Corporation, a Delaware corporation, with offices at 600 Federal Street, Andover, MA 01810 ("<u>Assignor</u>") owns certain patent applications and/or registrations, as listed in <u>Exhibit A</u> attached hereto and incorporated herein by this reference ("<u>Patents</u>"); and

WHEREAS, Altera Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, CA 95134 ("<u>Assignee</u>"), desires to acquire all of the right, title and interest of Assignor in, to and under the Patents;

WHEREAS, Assignor and Assignee have entered into a certain Asset Purchase Agreement, dated as of November 7, 2006 ("<u>Assignment Agreement</u>"), assigning, among other things, all right, title and interest in and to the Patents and in and to the registrations for same from Assignor to Assignee;

NOW, THEREFORE, for good and valuable consideration described in the Assignment Agreement, the receipt and sufficiency of which are hereby acknowledged, Assignor does hereby irrevocably sell, assign, transfer and convey unto Assignee all of its right, title and interest in and to the Patents, including all divisions, continuations, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the Patents (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the Patents throughout the universe, including without limitation all foreign counterparts and foreign equivalents of any of the foregoing.

Assignor authorizes and requests the patent officials in the United States and in any and all foreign jurisdictions to issue any and all letters patent and foreign counterparts or equivalents thereof to Altera Corporation, as assignee of the entire interest of Assignor therein, and covenants that Assignor has full right to convey the entire interest herein assigned and that Assignor has not executed and will not execute any agreements in conflict herewith.

Assignor further agrees, for itself, its successors and assigns, to execute such further documents and to perform such further lawful acts as may reasonably be required to effectuate this assignment.

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EXHIBIT 3.02(b) PAGE 1

> PATENT REEL: 018668 FRAME: 0384

IN WITNESS WHEREOF, Assignor has caused this assignment to be duly executed by an authorized officer on this 7th day of November, 2006.

TIMELAB CORPORATION

Maimer Thomas By: Name: THOMAS MARMEN CEO Title:

 STATE OF Massachusetts
)

 OUNTY OF Middlesex
)

On November 7, 2006, before me, the undersigned notary public in and for said County and State, personally appeared ______ Thomas Marmen

_____ personally known to me [or]

x proved to me on the basis of satisfactory evidence

Witness my hand and official seal.

Maria S. Corcoran

My commission expires on

09

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EXHIBIT 3.02(b) PAGE 2

> PATENT REEL: 018668 FRAME: 0385

EXHIBIT A

PATENTS

Ref No.	Title	Inventor(s)	Filing Date	Application Number	Grant Date	Patent Number	Status
	Arbitrary Waveform						
	Synthesizer Using a Free-	Carley,					
0001US1	Running Ring Oscillator	Allen	6/29/00	US09/607078	4/23/02	US6377094	Granted
	Arbitrary Waveform						
	Synthesizer Using a Free-	Carley,					
0001US2	Running Ring Oscillator	Allen	4/24/02	US10/131606	12/16/03	US6664832	Granted
	Arbitrary Waveform				1		
	Synthesizer Using a Free-	Carley,					
0001US3	Running Ring Oscillator	Allen	12/2/03	US10/726163			Abandoned
	Arbitrary Waveform						
	Synthesizer Using a Free-	Carley,					
0001US4	Running Ring Oscillator	Allen	9/27/04	US10/951435			Pending
	Arbitrary Waveform						
	Synthesizer Using a Free-	Carley,				-	
0001P2	Running Ring Oscillator	Allen	10/25/04	US60/614459			Expired
	Arbitrary Waveform				1		
• • • • ·	Synthesizer to Generate One	Carley,					
0001US5	or More Arbitrrary Waveforms	Allen	9/30/05	US11/239108	9/12/06	US7106115	Granted
	Clock Distributor Circuit for		1		1		1
	Maintaining a Phase						
	Relationship between						
	Remore Operating Nodes		}				
	and a Reference Clock on a				1		
0002P	Chip	Carley	8/8/02	US60/402031			Expired
	Clock Distributor Circuit for						
	Maintaining a Phase						
	Relationship between						
	Remore Operating Nodes						
0000010	and a Reference Clock on a	Oralia	0/7/00	11040/00000			
0002US	Chip	Carley	8/7/03	US10/636863			Pending
	Clocktree Tuning Shims and				1		
0003P	Shims Tuning Method	Mandry	2/25/03	US60/450076	L		Expired
0000000	Clocktree Tuning Shims and			110 10/705000			
0003US	Shims Tuning Method	Mandry	2/24/04	US10/785829			Pending
	Clock and Data Recovery		1				
0006US	Method and Apparatus	Allen	3/4/04	US10/793149			Pending
	Apparatus and Methods for		1		1		
00015	Securing Information in	l			1		
0004P	Storage Media	Allen	7/30/03	US60/491091			Expired
	Apparatus and Methods for						
	Securing Information in				1		
0004US	Storage Media	Allen	7/30/04	US10/909274			Pending
	Spread Spectrum Clock						
00441-0	Signal Generation System	Carley,					_
0011US	and Method	Allen	10/15/04	US10/964777	ļ		Pending
	Delay Circuit for						
	Synchronizing Arrival of a	Carley,	1				
	Clock Signal at Different	Allen,	1				
0008US	Circuit Board Points	Mandry	1/28/05	US11/044336	L		Pending
	Digitally Programmable Delay	Carley,					
	Circuit with Process Point	Allen,					
0009US	Tracking ("Vernier")	Mandry	1/28/05	US11/044315			Pending
	High Speed Serializer-						
0014P	Deserializer ("Serdes")	Carley	2/9/04	US60/543041			Expired

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Exhibit 3.02(b) PAGE 3

> PATENT REEL: 018668 FRAME: 0386

0014US	High Speed Serializer- Deserializer ("Serdes")	Carley	2/9/05	US11/052926	Pending
	Power Management of Components Having Clock				
0015P	Processing Circuits Power Management of Components Having Clock	Allen	1/11/05	US60/642505	Expired
0015P	Processing Circuits	Allen	5/24/05	US60/683789	Pending
0015US	Power Management of Components Having Clock Processing Circuits	Allen	1/6/06	US11/326423	Pending
0013P	Low Noise Switching Voltage Regulator and Methods for Therefor	Machesney	1/18/05	US60/644024	Expired
0013US	Low Noise Switching Voltage Regulator and Methods for Therefor	Machesney	1/17/06	US11/332290	Pending
0016P	Dense-Tap Transversal Filter With Elementary Coefficients	Machesney	5/24/05	US60/677356	Pending
0016US	Dense-Tap Transversal Filter With Elementary Coefficients	Machesney	5/1/06	US11/414225	Pending
0017P	Splitting Power Domains and Ground Domains for a Digital Clock Integrated Circuit	Carley, Allen, Mandry	6/14/05	US60/690129	Expired
0018P	Frequency Selective Voltage Regulator for Free Running Oscillator Loop	Carley, Allen, Mandry	6/13/05	US60/689543	Expired
0019P	Jitter Built-in-self-test Function for Digital Clock Generator Integrated Circuit	Carley, Allen, Mandry	7/6/05	US60/696543	Expired
0020P	Clock Signal Frequency Adjustment to Reduce Electromagnetic Interference	Carley, Allen	7/14/05	US60/698940	Expired
0021P	Marginable Integrated Circuit Clocking Device for System Development Verification and Operation	Carley, Allen	7/19/06	US60/807768	Pending

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EXHIBIT 3.02(b) PAGE 4

PATENT REEL: 018668 FRAME: 0387

RECORDED: 12/22/2006