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To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

**1. Name of conveying party(ies)**

CYPRESS SEMICONDUCTOR  
CORPORATION

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

**3. Nature of conveyance/Execution Date(s):**

Execution Date(s) 2/15/2006

- ☒ Assignment ☐ Merger  
☐ Security Agreement ☐ Change of Name  
☐ Joint Research Agreement  
☐ Government Interest Assignment  
☐ Executive Order 9424, Confirmatory License  
☐ Other

**2. Name and address of receiving party(ies)**

Name: Netlogic Microsystems, Inc.

Internal Address:

Street Address: 1875 Charleston Road

City: San Jose

State: CA

Country: United States Zip: 94043

Additional name(s) & address(es) attached? ☐ Yes ☒ No

**4. Application or patent number(s):**

☐ This document is being filed together with a new application.

A. Patent Application No.(s)  
10/931,960

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

**5. Name and address to whom correspondence concerning document should be mailed:**

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**6. Total number of applications and patents involved:** 1

**7. Total fee (37 CFR 1.21(h) & 3.41) \$ 40.00**

- ☐ Authorized to be charged by credit card  
☐ Authorized to be charged to deposit account  
☒ Enclosed  
☐ None required (government interest not affecting title)

**8. Payment Information**

a. Credit Card Last 4 Numbers \_\_\_\_\_  
Expiration Date \_\_\_\_\_

b. Deposit Account Number 50-2087

Authorized User Name Bradley T. Sako

**9. Signature:**

Bradley T. Sako  
Signature

December 19, 2006

Date

Bradley T. Sako

Total number of pages including cover sheet, attachments, and documents:

8

Name of Person Signing

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:  
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, V.A. 22313-1450

## ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

THIS ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS (this "*Assignment*") is made as of February 15, 2006 (the "*Assignment Date*") by Cypress Semiconductor Corporation, a Delaware corporation (the "*Assignor*"), to NetLogic Microsystems, Inc., a Delaware corporation (the "*Assignee*").

### RECITALS

A. Pursuant to the Agreement for the Purchase and Sale of Assets, dated January 25, 2006, by and between Assignor and Assignee (the "*Purchase Agreement*"), Assignor agreed to sell, assign, transfer, convey and deliver to Assignee certain assets, including all of Assignor's right, title and interest in and to the Patent and Patent Applications (as defined below).

B. The obligation of Assignee to consummate the transactions contemplated by the Purchase Agreement is conditioned in part on the execution and delivery of this Assignment.

### ASSIGNMENT

For good and valuable consideration, the receipt, adequacy and legal sufficiency of which are hereby acknowledged:

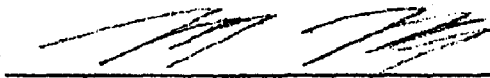
Assignor hereby sells, assigns, transfers, conveys and delivers to Assignee, its successors and assigns, (a) all worldwide right, title and interest in, to and under the patents and patent applications listed on Schedule A to this Assignment (collectively, the "*Patents and Patent Applications*"), including but not limited to all patent applications, patents, or similar legal protections that have been, or will be, obtained, based on any of said Patents and Patent Applications, (b) all right, title and interest in any provisional application of which any of the Patents and Patent Applications claims the benefit (c) all rights to obtain renewals, extensions, continuations, continuations-in-part, reissues, re-examinations, divisions, substitutes, or equivalents thereof, based on any of said Patents and Patent Applications, in the United States and all foreign countries, and (d) all past, present and future claims, counterclaims, causes of action, choses in action, rights of recovery, rights of set off, and rights of recoupment in or with respect to any of the Patents and Patent Applications.

Assignor grants the attorney of record the power to insert on this Assignment any further identification that may be necessary to comply with the rules of the United States Patent and Trademark Office, or rules of other entities, including United States or foreign governments or patent offices, for recordation of this document.

Assignor shall execute or cause to be delivered to Assignee such instruments and other documents, and shall take such other actions, as Assignee may reasonably request after the Assignment Date, that are necessary for the purpose of carrying out or evidencing the assignment of the Patents and Patent Applications pursuant to this Assignment.

IN WITNESS WHEREOF, Assignor has caused its duly authorized officer to execute this Assignment of Patents and Patent Applications as of the Assignment Date.

CYPRESS SEMICONDUCTOR CORPORATION

By: \_\_\_\_\_

Name: Brad Buss

Title: Chief Financial Officer

**SCHEDULE A****PATENTS AND PATENT APPLICATIONS**

METHOD AND APPARATUS FOR PRECHARGING MATCH OUTPUT IN A CASCADED CONTENT ADDRESSABLE MEMORY SYSTEM	235,663 – USP 5,621,677
FULLY STATIC CAM CELLS WITH LOW WRITE POWER AND METHODS OF MATCHING AND WRITING TO THE SAME	281,436 – USP 5,452,243
INTEGRATED CONTENT ADDRESSABLE MEMORY ARRAY WITH PROCESSING LOGICAL AND A HOST COMPUTER INTERFACE	284,347- USP 5,849,149
INSTRUCTION SET FOR A CONTENT ADDRESSABLE MEMORY ARRAY WITH READ/WRITE CIRCUITS AND AN INTERFACE REGISTER LOGIC BLOCK	284,372 – USP 5,860,085
MEMORY DEVICE AND SENSE AMPLIFIER CIRCUIT WITH FASTER SENSING SPEED AND IMPROVED INSENSITIVIES TO FABRICATION PROCESS VARIATIONS	SERIAL NUMBER NOT RECEIVED
DIFFERENTIAL DYNAMIC CONTENT ADDRESSABLE MEMORY AND HIGH SPEED NETWORK ADDRESS FILTERING	885,909 – USP 5,949,696
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CONTENT ADDRESSABLE MEMORY HAVING REDUNDANCY CAPABILITIES	09/661,630 – USP 6,751,755
CONTENT ADDRESSABLE MEMORY CELL	09/934,813 – USP 6,480,406
COMPACT DATA STRUCTURES FOR PIPELINED MESSAGE FORWARDING LOOKUPS	09/826,556
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HIGH SPEED TRANSMISSION SYSTEM WITH CLOCK INCLUSIVE BALANCED CODING	10/024,609 – USP 6,690,309
METHOD AND APPARATUS FOR CONTENT ADDRESSABLE MEMORY TEST MODE	10/026,141 – USP 6,697,275
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SEARCH METHOD AND APPARATUS FOR SEARCH ENGINE DEVICE	10/197,298
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A CIRCUIT AND METHOD TO ALLOW SEARCHING BEYOND A DESIGNATED ADDRESS OF A CONTENT ADDRESSABLE MEMORY	10/202,526
METHOD AND APPARATUS FOR PARALLEL PARITY CHECKING IN CAM DEVICE	10/208,225
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CONTENT ADDRESSABLE MEMORY (CAM) DEVICE HAVING SELECTABLE ACCESS AND METHOD THEREFOR	10/264,667

METHOD AND APPARATUS FOR IDENTIFYING CONTENT ADDRESSABLE MEMORY DEVICE RESULTS FOR MULTIPLE REQUESTING SOURCES	10/264,883 – USP 6,876,558
A MAGNITUDE COMPARATOR CIRCUIT FOR CONTENT ADDRESSABLE MEMORY WITH PROGRAMMABLE PRIORITY SELECTION	10/266,953
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DATA PRECLASSIFIER METHOD AND APPARATUS FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE	10/320,049 – USP 6,906,936
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SYSTEM AND METHOD FOR EFFICIENTLY SEARCHING A FORWARDING DATABASE THAT IS SPLIT INTO A BOUNDED NUMBER OF SUB-DATABASES HAVING A BOUNDED SIZE	10/402,887
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STAGGERED COMPARE ARCHITECTURE FOR CONTENT ADDRESSABLE MEMORY (CAM)	10/746,899 – USP 6,958,925

NETWORK DEVICE, CARRIER MEDIUM AND METHODS FOR INCREMENTALLY UPDATING A FORWARDING DATABASE THAT IS SPLIT INTO A BOUNDED NUMBER OF SUB-DATABASES HAVING A BOUNDED SIZE	10/809,244
ARCHITECTURE FOR NETWORK SEARCH ENGINES WITH FIXED LATENCY, HIGH CAPACITY, AND HIGH THROUGHPUT	10/841,607
A CIRCUIT, APPARATUS, AND METHOD FOR EXTRACTING MULTIPLE MATCHING ENTRIES FROM A CONTENT ADDRESSABLE MEMORY (CAM) DEVICE	10/866,353
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METHOD FOR ON-THE-FLY ERROR CORRECTION IN A CONTENT ADDRESSABLE MEMORY (CAM) AND DEVICE THEREFOR	11/043,391
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METHOD AND ARCHITECTURE FOR SMOOTHING CURRENT TRANSIENTS IN A CONTENT ADDRESSABLE MEMORY (CAM) DEVICE	11/085,399
DEVICE AND METHOD FOR ENSURING CURRENT CONSUMPTION IN SEARCH ENGINE SYSTEM	11/089,837
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RANDOM ACCESS MEMORY (RAM) METHOD OF OPERATION AND DEVICE FOR SEARCH ENGINE SYSTEMS	11/104,077
CONTENT COMPARATOR MEMORY (CCM) DEVICE AND METHOD OF OPERATION	11/146,639
METHOD AND SYSTEM FOR FINDING MAXIMAL STRIPES IN CACHE MEMORY WITH CONTENT ADDRESSABLE MEMORY	11/207,323
ROW EXPANSION REDUCTION BY INVERSION FOR RANGE REPRESENTATION IN TERNARY CONTENT ADDRESSABLE MEMORIES	11/218,366
PARTIAL ROW EXPANSION BY ORING FOR RANGE REPRESENTATION IN CONTENT ADDRESSABLE MEMORY	11/219,109
PSEUDO TERNARY CONTENT ADDRESSABLE MEMORY DEVICE HAVING ROW REDUNDANCY AND METHOD THEREFOR	11/281,227

Note: "USP" = U.S. Patent