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Docket No. <u>1026905-000032</u>

rk Office: Please record the attached documents or the new address(es) below.

METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT

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	Assignment					
4.	Application or patent number(s):					
	A. Patent Application No.(s) B. Patent No.(s) 11/486,107					

5. Name and address to whom correspondence concerning document should be mailed:

This document is being filed together with a new application.

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6. Total number of applications and patents involved: 1 11486107 11/09/2007 NJANNÁ

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Attorney's Docket No. <u>1026905-000032</u>

7. 2	Total fee (37 CFR 1.21(h) & 3.41) \$ 40		attached. Authorized to be charge Enclosed.	ged by credit card. PTO Form 2038 ged to deposit account 02-4800 interest not affecting title)	
) .	Signature:	Signature	 	January 5, 2007 Date	
		James A. LaBarre Name of Person Signing	Total number of pages includi	ng cover sheet, attachments, and documents: 3	7

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ASSIGNMENT

In consideration of the premises and other good and valuable consideration in hand paid, the receipt and sufficiency of which is hereby acknowledged, the undersigned,

(1) Yusaku ONO	(2) Osamu SUGA				
(3) Kazuyuki SAKATA	(4) Hirofumi TAGUCHI				
(5) Yushi OKUNO	(6) Toshiaki SUGIOKA				
(7) <u>Daisuke KONDO</u>					
who have made a certain new and useful invention, hereby	y sell, assign and transfer unto				
Renesas Technology Corp. 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-6334 JAPAN					
and					
Matsushita Electric Industrial Co., Ltd.					
1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501					
JAPAN					
and					
NEC Electronics Corporation					
1753 Shimonumabe.					
Nakahara ku, Kawasaki, Kanagawa, 211-8668					
<u>JAPAN</u>					
and					
FUJITSU LIMITED					
1·1, Kamikodanaka 4·chome, Nakahara·ku,					
Kawasaki shi, Kanagawa, 211-8588					
<u>JAPAN</u>					
and					
Kabushiki Kaisha Toshiba					
1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-0023					
<u>JAPAN</u>					
its successors and assigns (hereinafter designated "ASS	IGNEE") the entire right title and interest for the				
United States of America as defined in 35 U.S.C. 100 in th					
METHOD FOR DESIGNING SEMICONDUCTOR INTEG	RATED CIRCUIT LAYOUT				
for which an application for United States Letters Patent (Application No. 11/486,107 filed filed					
(Application No11/486,107, filed	July 14, 2006),				

and the undersigned hereby authorize and request the United States Commissioner of Patents and Trademarks to issue any and all United States Letters Patent which may be granted therefor and any and all extensions, divisions, reissues, substitutes, renewals, continuations, or continuations in part thereof, and the right to all benefits under the international Convention for the Protection of Industrial Property to the said ASSIGNEE, for its interest as ASSIGNEE, its successors, assigns and legal representatives; the undersigned agree that the attorneys of record in said application shall hereafter act on behalf of said ASSIGNEE;

AND the undersigned hereby agree to transfer a like interest, and to render all necessary assistance in making application for and obtaining original, divisional, reissued or extended Letters Patent of the United

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States, upon request of the said ASSIGNEE, its successors, assigns and legal representatives, and without further remuneration, in and to any improvements, and applications for patent based thereon, growing out of or related to the said invention; and to execute any papers by the said ASSIGNEE, its successors, assigns and legal representatives, deemed essential to ASSIGNEE's full protection and title in and to the invention hereby transferred.

 $SIGNED \ on \ the \ dates \ indicated \ aside \ our \ signatures:$

INVENTORS	DATE SIGNED
1) Name: Yusaku ONO	August 25, 2006
2) Samu Suga Name: Osamu SUGA	September 20, 2006
3) Kayuyulii Sakata Name: Kazuyuki SAKATA	August 31, 2006
4) Hivimi Tagnchi Name: Hirofumi TAGUCHI	Cct. 10. 2006
5) Yushi Okuno Name: Yushi OKUNO	atober, 30, 2006
6) Toshiaki Sugnicika	November 16, 2006
7) <u>Daisuke Kondo</u> Name: Daisuke KONDO	December: 4,2006