PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
QSPEED SEMICONDUCTOR, INC.	01/23/2007

RECEIVING PARTY DATA

Name:	SILICON VALLEY BANK
Street Address:	3979 Freedom Circle
Internal Address:	Suite 600
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 51

Property Type	Number
Patent Number:	6251716
Patent Number:	6674107
Patent Number:	6281705
Patent Number:	6304007
Patent Number:	6307223
Patent Number:	6355513
Patent Number:	6566936
Patent Number:	6750698
Patent Number:	6621722
Patent Number:	6486011
Patent Number:	6614289
Patent Number:	6349047
Patent Number:	6356059
Patent Number:	6542001

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Patent Number:	6580252
Patent Number:	6528880
Patent Number:	6549439
Patent Number:	6900506
Patent Number:	6921932
Patent Number:	6777722
Patent Number:	6661276
Patent Number:	6747342
Patent Number:	6696706
Patent Number:	6774417
Patent Number:	7075132
Patent Number:	6734715
Patent Number:	7098634
Patent Number:	7009228
Patent Number:	7038260
Patent Number:	6887768
Patent Number:	6975157
Patent Number:	6821079
Patent Number:	7122885
Patent Number:	7009229
Patent Number:	6995052
Patent Number:	7045397
PCT Number:	US0130497
Application Number:	10728449
Application Number:	10158326
Application Number:	10867972
Application Number:	10776487
Application Number:	60538741
Application Number:	10869718
Application Number:	11032272
Application Number:	60563596
Application Number:	60578963
Application Number:	60579020
Application Number:	60606676
Application Number:	60606810

Application Number:	60606814
Application Number:	60606776

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ATTORNEY DOCKET NUMBER:	220763.725 SECURITY AGMT
NAME OF SUBMITTER:	JAMES HUNT YANCEY, JR.

Total Attachments: 8

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of January 23, 2007 by and between SILICON VALLEY BANK ("Bank") and QSPEED SEMICONDUCTOR INC. ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor of even date herewith (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks and Patents to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents and Trademarks listed on Exhibits A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

QSPEED SEMICONDUCTOR INC.

3970 Freedom Circle
Santa Clara, California 95054
Attn: Michael Robinson

By: _____

Title: Vice President

BANK:

Address of Bank:

SILICON VALLEY BANK

3979 Freedom Circle, Suite 600
Santa Clara, California 95054
Attn: Samir Kaji

By: _____

Title: VP

SEARCHREV, INC.

EXHIBIT A

COPYRIGHTS

Description	Registration/ Application Number	Registration/ Application Date
None	N/A	N/A

EXHIBIT B

PATENTS

Title	Patent/Application Number(Publication Number)	Issue/Filing Date
NOVEL JFET STRUCTURE AND MANUFACTURE METHOD FOR LOW ON-RESISTANCE AND LOW VOLTAGE APPLICATION	6251716	06/26/2001
ENHANCEMENT MODE JUNCTION FIELD EFFECT TRANSISTOR WITH LOW ON RESISTANCE	6674107	01/06/2004
POWER SUPPLY MODULE IN INTEGRATED CIRCUITS	6281705	08/28/2001
SWITCHER FOR SWITCHING CAPACITORS	6304007	10/16/2001
COMPLEMENTARY JUNCTION FIELD EFFECT TRANSISTORS	6307223	10/23/2001
Asymmetric depletion region for normally off jfet	6355513	03/12/2002
TWO TERMINAL RECTIFIER USING NORMALLY OFF JFET	6566936	05/20/2003
CASCADE CIRCUITS UTILIZING NORMALLY-OFF JUNCTION FIELD EFFECT TRANSISTORS FOR LOW ON-RESISTANCE AND LOW VOLTAGE APPLICATIONS	6750698	06/15/2004
RECTIFIER CIRCUITS WITH LOW FORWARD VOLTAGE JFET DEVICE	6621722	09/16/2003
NOVEL JFET STRUCTURE AND MANUFACTURE METHOD FOR LOW ON-RESISTANCE AND LOW VOLTAGE APPLICATION	6486011	11/26/2002
STARTER DEVICE FOR NORMALLY OFF JFETS	6614289	09/02/2003
Full wave rectifier circuit using normally off JFETs	6349047	02/19/2002
Buck converter with normally off JFET	6356059	03/12/2002
POWER SUPPLY MODULE IN INTEGRATED CIRCUITS	6542001	04/01/2003
BOOST CIRCUIT WITH NORMALLY OFF JFET	6580252	06/17/2003
SEMICONDUCTOR PACKAGE FOR POWER JFET HAVING COPPER PLATE	6528880	03/04/2003

FOR SOURCE AND RIBBON CONTACT FOR GATE		
FULL WAVE RECTIFIER CIRCUIT USING NORMALLY OFF JFETS	6549439	04/15/2003
METHOD AND STRUCTURE FOR A HIGH VOLTAGE JUNCTION FIELD EFFECT TRANSISTOR	6900506	05/31/2005
JFET AND MESFET STRUCTURES FOR LOW VOLTAGE, HIGH CURRENT AND HIGH FREQUENCY APPLICATIONS	6921932	07/26/2005
METHOD AND STRUCTURE FOR DOUBLE DOSE GATE IN A JFET	6777722	08/17/2004
MOSFET DRIVER MATCHING CIRCUIT FOR AN ENHANCEMENT MODE JFET	6661276	12/09/2003
FLIP-CHIP PACKAGING	6747342	06/08/2004
STRUCTURE FOR A JUNCTION FIELD EFFECT TRANSITOR WITH REDUCED GATE CAPACITANCE	6696706	02/24/2004
ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUITS	6774417	08/10/2004
PROGRAMMABLE JUNCTION FIELD EFFECT TRANSISTOR AND METHOD FOR PROGRAMMING SAME	7075132	07/11/2006
TWO TERMINAL RECTIFIER USING NORMALLY OFF JFET	6734715	05/11/2004
BUCK-BOOST CIRCUIT WITH NORMALLY OFF JFET	7098634	08/29/2006
GUARD RING STRUCTURE AND METHOD FOR FABRICATING SAME	7009228	03/07/2006
DUAL GATE STRUCTURE FOR A FET AND METHOD FOR FABRICATING SAME	7038260	05/02/2006
METHOD AND STRUCTURE FOR COMPOSITE TRENCH FILL	6887768	05/03/2005
STARTER DEVICE FOR NORMALLY OFF JFETS	6975157	12/13/2005
METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE	6812079	11/02/2004
FLIP-CHIP PACKAGING	7122885	10/17/2006
ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUITS	7009229	03/07/2006

METHOD AND STRUCTURE FOR DOUBLE DOSE GATE IN A JFET	6995052	02/07/2006
JFET AND MESFET STRUCTURES FOR LOW VOLTAGE HIGH CURRENT AND HIGH FREQUENCY APPLICATIONS	7045397	05/16/2006
CASCADE DEVICE USING NORMALLY ON JFET	PCT/US01/30497	9/28/1996
FLIP-CHIP PACKAGING	10/728,449	12/4/1999
SPACER OXIDE TO REDUCE CAPACITANCE IN NORMALLY OFF JFET AND NORMALLY ON JFET	10/158,326	5/28/1998
METHOD AND STRUCTURE FOR DOUBLE DOSE GATE IN A JFET	10/867,972	6/13/2000
METHOD FOR FABRICATING A DUAL GATE STRUCTURE	10/776,487	2/9/2000
USING A SOURCE SENSE PIN ON JFET'S OR MosFet's TO IMPROVE SWITCHING TIMES	60/538,741	1/21/2000
SELF ADJUSTED SCHOTTKY BARRIER RECITFIERS FOR HIGH VOLTAGE APPLICATIONS	10/869,718	6/14/2000
METHOD OF MANUFACTURING A SCHOTTKY BARRIER RECTIFIER	11/023,272	12/21/2000
DEVICE STRUCTURES OF NORMALLY ON AND NORMALLY OFF JFETS	60/563,596	4/18/2000
MULTIPLE DOPED GATE VERTICAL FIELD EFFECT TRANSISTOR (FET) USING DEPOSTED LATERAL GATE	60/578,963	6/9/2000
VERTICAL FIELD EFFECT TRANSISTOR (FET) USING DEPOSITED LATERAL GATE		
JUNCTION EFFECT FIELD TRANSISTOR (JFET) GATED SCHOTTKY DIODE AS EMBEDDED BODY DIODE IN POWER MOS DEVICE	60/579,020	6/9/2000
A SUPER JFET DEVICE STRUCTURES	60/606,676	8/31/2000
A SUPER JFET DEVICE STRUCTURES		9/16/2000
USING AN ENHANCEMENT MODE JFET AS A SYNCHRONOUS RECTIFIER AND WAYS TO DRIVE IT	60/606,810	8/31/2000
VERTICAL FIELD EFFECT TRANSISTOR (FET) USING DEPOSITED LATERAL GATE	60/606,814	8/31/2000
JUNCTION EFFECT FIELD TRANSISTOR (JFET) GATED SCHOTTKY DIODE	60/606,776	8/31/2000
DEPLETION MODE POWER JFET AND ENHANCEMENT MODE N-CHANNEL MOSFET WITH ZENER DIODE		3/17/2001
High Voltage application		12/27/2005

EXHIBIT C

TRADEMARKS

Mark	Registration/ Application Number	Registration/Application Date
POWERJFET	2905178	11/23/2004
LVT & Design	2821479	03/09/2004
LOVOLTECH	2817788	02/24/2004