PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
Conexant Systems, Inc.	11/13/2006

RECEIVING PARTY DATA

Name:	The Bank of New York Trust Company, N.A., as Collateral Agent
Street Address:	227 West Monroe, Suite 2600
Internal Address:	ATTN: Corporate Trust Administration
City:	Chicago
State/Country:	ILLINOIS
Postal Code:	60606

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	11083080

CORRESPONDENCE DATA

Fax Number: (646)710-5433

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: (212) 408-5433
Email: DHopkins@Chadbourne.com
Correspondent Name: Dennis Hopkins
Address Line 1: Chadbourne & Parke LLP
Address Line 2: 30 Rockefeller Plaza
Address Line 4: New York, NEW YORK 10112

ATTORNEY DOCKET NUMBER:	14733.058
NAME OF SUBMITTER:	Dennis C. Hopkins

Total Attachments: 40
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**PATENT
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GRANT OF
SECURITY INTEREST IN PATENT RIGHTS

This GRANT OF SECURITY INTEREST IN PATENT RIGHTS ("Agreement"), effective as of November 13, 2006 is made by CONEXANT SYSTEMS, INC., a Delaware corporation, located at 4000 MacArthur Boulevard, Newport Beach, California, 92660 (the "Company"), in favor of THE BANK OF NEW YORK TRUST COMPANY, N.A., a national banking association, as Collateral Agent (the "Collateral Agent") for the holders of the notes (the "Holders") issued pursuant to the Indenture, dated as of November 13, 2006, (as amended, supplemented or otherwise modified from time to time, the "Indenture"), among the Company, the subsidiary guarantors parties thereto and The Bank of New York Trust Company, N.A., as trustee (the "Trustee").

W I T N E S S E T H:

WHEREAS, pursuant to the Indenture, the Company intends to issue to the Holders its Floating Rate Senior Secured Notes due 2010;

WHEREAS, in connection with the Indenture, the Company and certain other subsidiaries of the Company have executed and delivered the Security Agreement, dated as of November 13, 2006 (as amended, supplemented or otherwise modified from time to time, the "Security Agreement");

WHEREAS, pursuant to the Security Agreement, the Company and certain other subsidiaries pledged and granted to the Collateral Agent for the ratable benefit of the Collateral Agent and the Holders, a security interest in all Intellectual Property, including the Patents; and

WHEREAS, the Company has duly authorized the execution, delivery and performance of this Agreement;

NOW THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, and in order to guarantee the obligations of the Company with respect to the Notes and the Indenture, the Company agrees, for the benefit of the Collateral Agent and the Holders, as follows:

SECTION 1. Definitions. Unless otherwise defined herein or the context otherwise requires, terms used in this Agreement, including its preamble and recitals, have the meanings provided or provided by reference in the Indenture and in the Security Agreement.

SECTION 2. Grant of Security Interest. The Company hereby pledges and grants a continuing security interest in, and a right of setoff against, and agrees to assign, transfer and convey, upon written demand delivered to the Company upon the occurrence and during the continuance of an Event of Default without requiring further action by either party and to be effective upon such demand, all of the Company's right, title and interest in, to and under the Patents and Patent Licenses (including, without limitation, those items listed on Schedule A

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hereto) (collectively, the "Collateral"), to the Collateral Agent for the benefit of the Collateral Agent and the Holders to secure payment, performance and observance of the Obligations.

SECTION 3. Purpose. This Agreement has been executed and delivered by the Company for the purpose of recording the grant of security interest herein with the United States Patent and Trademark Office. The security interest granted pursuant to Section 2 hereof has been granted, and the agreement to assign, transfer and convey under Section 2 hereof has been entered into, in each case, in connection with the Security Agreement, and such grant and agreement to assign, transfer and convey are expressly subject to the terms and conditions of the Security Agreement. The Security Agreement (and all rights and remedies thereunder) shall remain in full force and effect in accordance with its terms.

SECTION 4. Acknowledgment. The Company does hereby further acknowledge and affirm that the rights and remedies of the Collateral Agent and the Holders with respect to the security interest in the Collateral granted hereby are more fully set forth in the Indenture and the Security Agreement, the terms and provisions of which (including the remedies provided for therein) are incorporated by reference herein as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

SECTION 5. Counterparts. This Agreement may be executed in counterparts, each of which will be deemed an original, but all of which together constitute one and the same original.

SECTION 6. Termination. Upon the occurrence of any of the events specified in Section 11.8 (a) of the Indenture, the Collateral Agent shall promptly cause to be released the security interest in the Patents granted pursuant to this Agreement in accordance with Section 11.14 of the Security Agreement.

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be duly executed and delivered by their respective officers thereunto duly authorized as of the day and year first above written.

CONEXANT SYSTEMS, INC.

By: _____

Name: Dennis E. O'Reilly

Title: Senior Vice President, Chief Legal Officer and Secretary

Date:

THE BANK OF NEW YORK TRUST COMPANY, N.A.
as Collateral Agent for the Holders

By: _____

Name:

Title:

Date:

State of California)
County of Orange)

CALIFORNIA ALL-PURPOSE
CERTIFICATE OF ACKNOWLEDGMENT

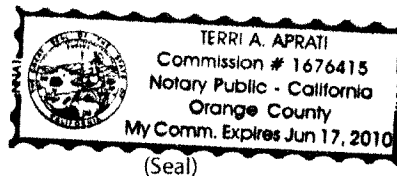On November 9, 2006, before me, Terri A Aprati,

personally appeared Dennis E O'Reilly

personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____

TERRI A. APRATI
Commission # 1676415
Notary Public - California
Orange County
My Comm. Expires Jun 17, 2010

(Seal)

OPTIONAL INFORMATION

Although the information in this section is not required by law, it could prevent fraudulent removal and reattachment of this acknowledgment to an unauthorized document and may prove useful to persons relying on the attached document.

Description of Attached Document

The preceding Certificate of Acknowledgment is attached to a document

titled/for the purpose of _____

_____

containing _____ pages, and dated _____

The signer(s) capacity or authority is/are as:
- [ ] Individual(s)
- [ ] Attorney-in-Fact
- [ ] Corporate Officer(s) _____
  Title(s)

- [ ] Guardian/Conservator
- [ ] Partner Limited/General
- [ ] Trustee(s)
- [ ] Other _____

representing: _____
Name(s) of Person(s) or Entity(ies) Signer is Representing

Additional Information

Method of Signer Identification
- [ ] Personally known to me
- [ ] Proved to me on the basis of satisfactory evidence
  - ( ) form(s) of identification ( ) credible witness(es)

Identification is detailed in notary journal on:

Page # _____   Entry # _____

Notary contact: _____

Other
- [ ] Additional Signer(s)   [ ] Signer(s) Thumbprint(s)
- [ ] _____

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be duly executed and delivered by their respective officers thereunto duly authorized as of the day and year first above written.

CONEXANT SYSTEMS, INC.

By:_____

Name:

Title:

Date:

THE BANK OF NEW YORK TRUST COMPANY, N.A.
as Collateral Agent for the Holders

By:_____

Name:

Title: JANICE OTT ROTUNNO
                VICE PRESIDENT

Date:

ACKNOWLEDGMENT OF COLLATERAL AGENT

STATE OF   ILLINOIS   )
) ss
COUNTY OF   **COOK**   )

On the _13_ day of November, 2006, before me personally came _Janeen Reilly_, who is personally known to me to be the _Vice President_ of THE BANK OF NEW YORK TRUST COMPANY, N.A., a national banking association; who, being duly sworn, did depose and say that she/he is the _Vice President_ in such association, the association described in and which executed the foregoing instrument; that she/he executed and delivered said instrument pursuant to authority given by the _____ of such association; and that she/he acknowledged said instrument to be the free act and deed of said association.
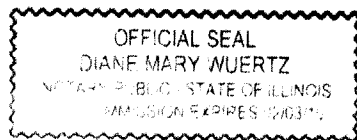
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Notary Public

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SCHEDULE A

United States Patent Applications:

Application Number	Filed Date	Application Title
10/786,921	02/25/04	Fully Integrated Broadband Tuner
09/617,587	07/18/00	Receiver Circuit
09/966,374	09/27/01	Method and Apparatus for Flexibly Filtering Scheduling Messages in a Communication System
10/012,684	11/13/01	System of and Method for Decoding Trellis Codes
09/870,926	05/30/01	SNR-Related Parameter Estimation Method and System
10/101,049	03/19/02	Method and Apparatus for Decoding Video Signals by Reusing Video Analog-to-Digital Converters to Demodulate Audio Information
09/892,069	06/26/01	Method and Apparatus for Scheduling Upstream Data Packets in a Broadband Communication System
10/464,361	06/17/03	Efficient communication system for reliable frame transmission over broad SNR ranges
10/099,556	03/13/02	Transmit Multiplexing and Receive Processing for Delay Spread Channels
10/389,272	03/14/03	Transmit Diversity Framing Structure fro Multipath Channels
10/376,824	02/28/03	Frequency Synthesizer with Automatic VCO Selection System
10/284,121	10/29/02	Subset Codes - a Low Complexity Multi-Rate Encoding and Decoding Scheme
10/600,163	06/19/03	Hypothetical Reference Decoder for Compressed Image and Video
11/013,963	12/16/04	Noise Reduction Systems and Methods
10/611,400	06/30/03	Satellite Transcoder
10/611,402	06/30/03	System for Data Encryption and Decryption of Digital Data Entering and Leaving Memory
10/611,325	06/30/03	Procedure For BPSK Modulation with Reduced Envelope Peaking

Application Number	Filed Date	Application Title
10/750,989	12/31/03	A Low-Cost High Performance Front-End Active Splitter for a System Containing Multiple Reception Units
10/751,013	12/31/03	DC Offset Correction for Direct Conversion Receiver
10/776,121	02/10/04	Comb Filter Design for Separating Luminance and Chrominance in Video Signals
10/776,075	02/10/04	Luminance and Chrominance Separation System
11/323,337	12/30/05	Video Auto Format Detection
10/776,121	02/10/04	Comb Filter Design for Separating Luminance and Chrominance in Video Signals
10/867,355	06/14/04	Method and Apparatus for Efficient Computation of Check Equations in Periodical Low Density Parity Check (LDPC) Codes
11/244,568	10/06/05	Systems and Method for a Highly Integrated, Multi-Mode Tuner
11/194,085	07/29/05	Delay-Locked Loop(DLL) Locking Scheme Using Phase-Frequency Detector(PFD) State Hopping Via Pulse Swallowing
11/194,107	07/28/05	System and Method For Detecting Known Sequence In Transmitted Sequence
11/460,298	07/27/06	Systems and Method for Automatic Quadrature Phase Imbalance Compensation Using Delay Locked Loop
11/096,217	03/31/05	High Linearity, Low Power, Double-Balanced Mixer Using A Folded Input Transconductor For Direct Conversion Transmitters
11/522,583	09/18/06	Multipath Processing Systems and Methods
11/303,449	12/16/05	Efficient Decoders for LDPC Codes
11/233,674	09/23/05	De-blocking and De-ringing Systems and Methods
11/303,876	12/16/05	Multi-Channel LDPC Decoder Architecture
	03/16/06	3D Comb Filter Using PC Host Memory
09/499,833	02/08/00	Small-Format Subsystem for Broadband Communication Services
09/021,589	02/10/98	Bit Stream Protocol for the Integration of Text and Graphics In Multi-Media Applications
10/892,738	07/16/04	Iterative Decoder Employing Multiple External Code Error Checks to Lower the Error Floor

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Application Number	Filed Date	Application Title
11/174,359	06/30/05	Frequency Synthesis Scheme to Avoid Gaps and VCO Pulling in DBS Systems
10/340,577	01/10/03	Signal Derotating Receiver
10/340,854	01/10/03	Guard Interval Analysis Method and Apparatus
09/887,877	06/21/01	Rate N/N Systematic, Recursive Convolutional Encoder and Corresponding Decoder
10/368,017	02/14/03	Symbol Reliability Determination and Symbol Pre-Selection Based on Reliability Criteria
10/108,054	03/25/02	Efficient, High Fidelity Transmission of Modulation Schemes Through Power-Constrained Remote Relay Stations by Local Transmit Predistortion and Local Receiver Feedback
10/250,353	06/27/03	Demodulator Circuit
10/170,165	06/12/02	Method and Apparatus for a Multicarrier Receiver Circuit and Guard Interval Size Detection
10/210,591	07/31/02	Integrated Programable Tuner
10/214,960	08/08/02	Cable Receiver Having In-Band and Out-Of-Band Tuners
10/677,110	10/01/03	Fast Channel Scanning and Acquisition Algorithms for Cable Modem Applications
10/882,083	06/29/04	Simultaneous Multiple Channel receiver
10/655,698	09/05/03	Hypothetical Reference Decoder for Compressed Image and Video
10/675,566	09/30/03	Architecture for a Flexible and High-Performance Gateway Cable Modem
11/026,670	12/31/04	Satellite Multi-Choice Switch System
10/676,900	09/30/03	TCP Acceleration System
10/952,435	09/29/04	Canceling Radio Frequency Interferers (RFI) in xDSL Signals
10/970,718	10/22/04	Hierarchical Trellis Coded Modulation
11/009,710	12/13/04	Method and System for Virtual Exchange Reference Impact (VERI) for Use in Mixed Spectrum Management in DSL
11/032,203	01/10/05	Systems and Methods for Achieving Improved ADSL Data Rates Over USB 1.1 Channel
11/031,020	01/10/05	Real-Time Formation of Optimal Power Spectral Density Masks

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Application Number	Filed Date	Application Title
11/035,422	01/14/05	Single End Loop Testing for DSL Provisioning and Maintenance
11/197,524	08/05/05	System and Method for Echo Cancellation
11/224,328	09/13/05	Multistage Signal Detection in MIMO Transmissions and Iterative Detection of Precoded OFDM
11/248,224	10/13/05	Method and System for Turbo Trellis Coded Modulation Scheme for Communication Systems
11/282,109	11/18/05	Method and System for Adaptive VDSL System with Variable Sampling Frequency and Time-Domain Equalizer
11/297,632	12/09/05	Method and System for Dynamic Interleaver Adaptation Scheme in VDSL
11/297,634	12/09/05	M&S for Dynamic Interleaver Adaptation Scheme
11/315,372	12/23/05	A New Bit-Loading Algorithm for a DMT Receiver
11/320,918	12/30/05	Time-Domain Equalizer for DMT-Based VDSL Systems with Cyclic Extension in Training Signals
	08/31/06	Techniques to Resolve SNR-Margin Difference between Fast and Interleave Channels under Colored Noise Condition for DMT-Based DSL System
	08/31/06	Minimum Power Leakage Windowing for VDSL Using Least Square Technique
60/789,648	04/05/06	Multi-Format Stream Remultiplexer for Multi-Pass, Multi-Stream, Multiplexed Transport Stream Processing
	04/26/06	Encoded Digital Video Content Protection Between Transport Demultiplexer and Decoder
10/054,359	01/17/02	Efficient Head Related Transfer Function Filter Generation
	08/30/06	Design Method for Reliable Head Related Transfer Function Filters
10/000,878	11/14/01	System and Method for Remote Translation of Data Packets
10/418,748	04/17/03	Method and Apparatus for Preamble Detection and Time Estimation in OFDM Communication Systems
10/079,188	02/20/02	MAC-Layer Priority Adjustment

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Application Number	Filed Date	Application Title
10/422,014	04/21/03	Circuit Connections for Sending Entertainment Content Over Local Area Networks
10/422,070	04/21/03	Effective Spectrum Control in OFDM
10/147,031	05/15/02	Method and Apparatus for Providing Life Line Service to Access Gateway Telephony Subscribers
10/137,601	04/29/02	Digital Isolation Barrier as Interface Bus for Modems
10/303,317	11/21/02	Power Proof Code Image Recovery
10/346,572	01/15/03	Web-Based Redirect Feature
10/697,819	10/31/03	Using a Transformer for Power, Timing, and Bidirectional Data
10/428,702	05/01/03	Compromise Equalizer for FSK Modulation Receiver
10/735,257	12/12/03	Method of Software Driver Delivery for Universal Serial Bus (USB) Devices
10/949,861	09/24/04	Circular Constellations with Coherent Gain/Differential Phase and Pilots
10/950,262	09/24/04	Frame Structure for OFDM Signaling, Including Beacons and Traffic
10/950,063	09/24/04	MAC Structure with Packet-Quasi-Static Blocks and ARQ
10/950,063	09/24/04	Broadcast with Redundant Coding
10/949,956	09/24/04	Channel Sounding and Channel Analysis
11/437,311	05/19/06	Spread Spectrum Clock Generation
11/492,505	07/24/06	Bandwidth Management In A Powerline Network
11/492,506	07/24/06	Flexible Scheduling Of Resources In A Noisy Environment
11/492,487	07/24/06	Communicating Schedule And Network Information In A Powerline Network
11/438,011	05/19/06	Inbound DSP Noice Cancellation Algorithm on VoIP Compression Stream
09/547,424	04/11/00	Modulation Switching for Splitterless DSL Transmission
09/290,854	04/13/99	An Image Processor that Performs Edge Enhancement Using a Dynamic Threshold
09/989,100	11/21/01	Integrated Transformer for Multiple Transceivers

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Application Number	Filed Date	Application Title
09/765,741	01/19/01	System and Method for Sensing a Sound System
10/245,982	09/18/02	Method and Apparatus for Automatically Detecting Virtual Circuit Settings and Encapsulation Types in a DSL Network
10/738,256	12/17/03	Design of a Lateral Metal Insulator Metal Capacitor in a Semiconductor Metal Process to Meet Density and Slotting Rules
10/990,641	11/16/04	ESD Network for Mixed Signal Integrated Circuits Using Ultra Thin Gate Oxides
11,107,206	04/15/05	MOSFET Having Increased Snap-Back Conduction Uniformity
09/295,562	04/21/99	Electronic Device Attachment Methods and Apparatus for Forming an Assembly
11/438,009	05/19/06	MODEM CALL FORWARDING AND THREE-WAY CALLING FEATURES FOR VOIP APPLICATIONS
11/438,005	05/19/06	Directory Sync Between Skype and Smart Phone
11/186,260	07/21/05	Packet Processing Systems and Methods
10/927,487	08/27/04	Modified OFDM Subcarrier Profile
11/121,743	05/04/05	Pilot Tone Processing Systems and Methods
11/215,563	08/29/05	Systems and Methods For Calibrating Transmission of an Antenna Array
11/185,665	07/20/05	Packet Generation Systems and Methods
10/995,188	11/24/04	Systems and Methods for Wireless Wake-On-LAN for Wireless LAN Devices
11/121,661	05/04/05	Cyclic Diversity Systems and Methods
11/159,812	06/22/05	Legacy Compatible Spatial Multiplexing Systems and Methods
11/448,603	06/06/06	Method of Coding Data
10/880,370	06/30/04	Event-Based Multichannel Direct Link
10/880,367	06/30/04	Uplink Direct Link Relay
10/880,325	06/30/04	Time-Scheduled Multichannel Direct Link
10/977,490	11/01/04	Location Awareness In Wireless Networks
10/977,469	11/01/04	Independent Direct Link Protocol
10/977,470	11/01/04	Automatic Peer Discovery

Application Number	Filed Date	Application Title
11/314,143	12/21/05	Client Connection Mechanism And Remote Configuration
11/105,909	04/13/05	Dual Mode Communication Systems and Methods
11/106,915	04/15/05	Packet Generation Systems and Methods
11/033,524	01/12/05	High Data-Rate Multi-Channel Architecture
11/410,707	04/25/06	Beamforming Systems and Methods
10/861,066	06/04/04	Stolen Vehicle Tracking Using Dedicated Short Range Communication
11/411,619	04/26/06	Systems and Methods for Transmitter Diversity Expansion
11/549,438	10/13/06	MAC Protection for Beamforming with U-APSD "ACK NAV"
60/735,024	11/08/05	Avoiding EIFS
60/750,114	12/13/05	Dual CTS Protection
60/752,291	12/19/05	More PSMP Indication
60/757,827	01/09/06	Symmetric TXOP Truncation
60/762,425	01/25/06	Tx Announcement
60/782,628	03/14/06	U-APSD and PS-Poll Power Save Improvement
60/784,971	03/20/06	Low Power Bursting for 802.11 Wireless Networks
60/798,993	05/08/06	Direct Link Suspension Method
60/801,299	05/18/06	Cold Roaming Improvements
60/801,300	05/18/06	Periodic AP Polling
60/798,994	05/08/06	Piggyback ACK Protocol
10/458,127	06/10/03	Technique for Mitigating Intererupt Latency in a Host-Based Wireless LAN Adapter
10/428,618	05/02/03	S&M for Personal Computer Implementing Wireless Network Adapter
10/442,606	05/21/03	Method for Minimizing Time Critical Transmit Processing for a Personal Computer Implementation of a Wireless Local Area Network Adapter
10/460,684	06/12/03	Method for Minimizing Receive Packet Processing for a Personal Computer Implementation of a Wireless Local Area Network Adapter

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Application Number	Filed Date	Application Title
10/625,799	07/23/03	Method for Mitigating Adverse Processor Loading in a Personal Computer Implementation of a Wireless Local Area Network Adapter
60/843,261	09/08/06	Simultaneous IBSS and BSS
60/843,666	09/12/06	Codec Rate Mapper
60/851,648	10/13/06	802.11 Power Savings During BT Transmissions
60/848,578	09/28/06	A Fragmenter in a Wireless Local Area Network Device
	11/07/06	Client Power Save during AP Vacations (PSMP-to-Self)
	11/07/06	Carrier Sense Set and Reset Mechanism
10/989,289	11/17/04	Wireless Access Point Simultaneously Supporting Basic Service Sets on Multiple Channels
09/808,652	03/15/01	Bandwidth Partitioning Using Emulated Weighted Fair Queuing (EWFQ)
09/824951	04/03/01	Single Switch Image for a Stack of Switches
09/866259	05/25/01	Data Network Node Having Enhanced Security Features
10/263880	10/03/02	Buffer Management Scheme
10/264016	10/03/02	A Fabric Based Matching Implementation in a Switching System with Enforced Traffic Balance
09/9699702	10/03/01	Method of Pacing of Synchronization of Routing Information in a Data Switching Environment
10/284,856	10/31/02	Method of High Availability Ethernet Backpane
10/285,952	11/01/02	Media Access Control for High Efficiency Ethernet Backplane
10/319,304	12/13/02	Scheduling Method for Combined Unicast and Multicast Queuing
10/729,804	12/05/03	Class-Based Rate Control Using Multi-threshold Leaky Bucket
10/326,352	12/20/02	Apparatus for Link Failure Detection on High Availability Ethernet Backplane
10/750,445	12/31/03	Space Efficient High Speed Search Engine
10/812,141	03/29/04	Compact Packet Switching Node Storage Architecture Employing Double Data Rate Synchronous Dynamic RAM

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Application Number	Filed Date	Application Title
10/881,226	06/30/04	Combined Pipelined Packet Classification and Address Search Method and Apparatus for Switching Envionments
10/901,873	07/29/04	Remote Control of an Ethernet Switching Node in a Stack of Switching Nodes
10/903,437	07/30/04	Methods and Apparatus Providing Rapid End-to End Failover in a Packet Switched Communications Network

United States Patents:

Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/641,406	08/17/00	6,728,401	04/27/04	Red Eye Removal Using Digital Color Image Processing
09/192,954	11/16/98	6,222,643	04/24/01	Probability Error Diffusion for Digital Image Printing
09/192,818	11/16/98	6,343,851	02/05/02	Black Replacement for Color Digital Image Printing
09/746,965	12/21/00	6,343,851	02/05/02	K Replacement for Color Digital Image Printing
09/192,616	11/16/98	6,449,664	09/10/02	Two-Dimensional Direct Memory Access to Maximize Processing Resources in Image Processing Systems
09/282,956	04/01/99	6,456,389	09/24/02	The Pipelined Retrieving and Filling Scheme for PIFLM1 BRB Rotation Buffer Memory
09/282,949	04/01/99	6,449,057	09/10/02	An Innovative Addressing Scheme for Bit Rotation Block in Print interface Chip PIFLM
09/283,876	04/01/99	6,636,328	10/21/03	Flexible Array Image Data Processing for Ink Jet Nozzle Data Control in Digital Image Printing Systems
09/780,054	02/09/01	7,002,978	02/21/06	SCHEDULING TECHNIQUES FOR A DATA CELL IN A DATA SWITCH
09/753,797	01/02/01	7,002,916	02/21/06	ASYNCHRONOUS TRANSFER MODE TRAFFIC SHAPERS
09/062,301	04/17/98	6,349,098	02/19/02	METHOD AND APPARATUS FOR FORMING A VIRTUAL CIRCUIT
09/060,228	04/14/98	6,198,723	03/06/01	Asynchronous Transfer Mode Traffic Shapers
08/872,530	06/11/97	6,229,812	05/08/01	SCHEDULING TECHNIQUES FOR DATA CELLS IN A DATA SWITCH
08959,056	10/28/97	6,069,893	05/30/00	ASYNCHRONOUS TRANSFER MODE SWITCHING ARCHITECTURES HAVING CONNECTION BUFFERS
09/898,640		6,798,870	07/03/01	Non-Real Time Facsimile System for a Computing Device
10/808,653	03/24/04	6,831,589	12/14/04	WIRELESS LAN RADAR

Application Number	Filed Date	Patent Number	Issued Date	Application Title
				DETECTOR MISSING PULSE CAPABILITY
10/855,951	05/28/04	6,974,740	12/13/05	Symmetric Inducting Device for an Integrated Circuit Having a Ground Shield
10/855,948	05/28/04	7,064,363	06/20/06	Symmetric Inducting Device for an Integrated Circuit Having a Ground Shield
10/855,953	05/28/04	7,084,481	08/01/06	Symmetric Inducting Device for an Integrated Circuit Having a Ground Shield
10/893,673	07/15/04	7,065,703	06/20/06	Sychronization of a Communications System

09/588,266	05/06/00	6,724,817	04/20/04	Adaptive Image Data Compression
09/736,891	12/13/00	6,785,700	08/31/04	Implementation of Wavelet Functions in Hardware
155,891	11/23/93	5,473,754	12/05/95	Branch Decision Encoding Scheme
568,045	12/06/95	5,828,692	10/27/98	Baseband Demodulator for Polar or Rectangular Modulated Signal in a Cordless Spread Spectrum Telephone
08/568,871	12/07/95	5,758,263	05/26/98	Selection of Communication Channel in a Digital Cordless Telephone
08/568,714	12/07/95	5,983,340	11/09/99	Microprocessor System With Flexible Instruction Controlled by Prior Instruction
08/568,840	12/07/95	5,852,561	12/22/98	Selective Configuration of Operating Programs Stored in an Application Specific Integrated Circuit
568,049	12/06/95	5,896,576	04/20/99	Audio Mute for Digital Cordless Telephone
766,817	09/26/91	5,150,077	09/22/92	Generation of Horizontal Sync Pulse
014,359	02/05/93	5,406,306	04/11/95	System for, and Method of Displaying Information From a Graphics Memory and a Video Memory on a Display Monitor
029,121	03/10/93	5,404,173	04/04/95	Method to Synchronize Video Modulation Using a Constant Time Base

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
320,166	03/10/93	5,638,131	06/10/97	Method to Synchronize Video Modulation Using a Constant Time Base
802,072	12/03/91	5,198,703	03/30/93	System for Detecting Voltage Pulses of a Particular Magnitude
619,400	11/29/90	5,163,019	11/10/92	Binary Carry Circuitry
986,723	12/08/92	5,521,539	05/28/96	A Delay Line Providing an Adjustable Delay
909,074	07/02/92	5,325,001	06/28/94	Negative Feedback Sense Pre-Amplifier
979,803	11/20/92	5,274,275	12/28/93	Comparator
884,472	07/11/86	4,875,046	10/17/89	Centroiding Algorithm for Networks Used in A/D and D/A Converters
354,864	05/22/89	4,983,973	01/08/91	Non-Linear Analog-to-Digital Converter
08/337,924	11/10/94	5,732,279	03/24/98	System and Method for Command Processing or Emulation in a Computer System Using Interrupts, Such as Emulation of DMA Commands Using Burst Mode . . .
337,939	11/10/94	5,715,437	02/03/98	System for, and Method of, Processing in Hardware Commands Received from Software Without Polling of the Hardware by the Software
543,236	10/13/95	5,717,904	02/10/98	Apparatus and Methods for Automatically Controlling Block Writes
07/850,544	03/13/92	5,325,401	06/18/94	L-Band Tuner With Quadrature Downconverter for PSK Data Applications
938,109	08/31/92	5,379,243	01/03/95	Method and Apparatus for Performing Finite Field Division
998,300	12/30/92	5,550,869	08/27/96	Demodulator for Consumer Uses PSK Demodulator (In Canada)
08/620,768	12/03/90	5,130,570	07/14/92	Constant-Current Integrated Power Supply
07/074,256	07/16/87	4,899,103	02/06/90	Current Meter
224,871	07/26/88	4,899,154	02/06/90	Flash Comparator

Application Number	Filed Date	Patent Number	Issued Date	Application Title
06/810,911	12/18/85	4,905,189	02/27/90	System for Reading and Writing Information
683,259	04/10/91	5,298,815	03/29/94	System for Reading and Writing Information
081,910	08/05/87	4,841,252	06/20/89	System for Compensating for Offset Voltages in Comparators
018,014	02/24/87	4,812,818	03/14/89	Digital-to-Analog Converter
921,530	10/21/86	4,813,023	03/14/89	System Employing Negative Feedback for Decreasing the Response Time of a Cell
333,973	11/03/94	5,541,598	07/30/96	Current Cell for Converting a Binary Value to an Analog Value
069,317	07/02/87	4,733,153	03/22/88	Switching System for Capacitor Charging/Discharging
08/319,427	10/06/94	5,542,041	07/30/96	Apparatus for, and Methods of, Providing a Universal Format of Pixels and for Scaling Fields in the Pixels
512,757	04/20/90	5,111,204	05/05/92	Apparatus for Converting Data Between Digital and Analog Values
106,179	10/07/87	4,794,282	12/27/88	Apparatus for Converting Data Between Digital and Analog Values
104,690	10/05/87	4,831,282	05/16/89	Apparatus for Converting Data Between Digital and Analog Values
07/225,055	07/26/88	4,904,922	02/27/90	Apparatus for Converting Data Between Digital and Analog Values
164,263	12/09/93	5,379,077	01/03/95	System for and Method of, Operating Upon NTSC and PAL Signals
006,823	01/21/93	5,367,203	11/22/94	System for Determining the Time at Which an Analog Voltage Crosses a Voltage Threshold
006,813	01/21/93	5,400,056	03/21/95	Apparatus for and Method of Processing and Converting Binary Informtion to Corresponding Analog Signals
09/358,299	07/21/99	6,272,681	08/07/01	Cable Modem Optimized for High-Speed Data Transmissions From the Home to the Cable Head
016,131	02/10/93	5,406,219	04/11/95	Differential-to-Single-Ended Converter
923,632	10/27/86	4,860,011	08/22/89	Flash Analog-to-Digital Converter

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
102,034	09/29/87	4,868,548	09/19/89	Clock Synchronization System
455,888	12/21/89	5,170,445	12/08/92	Document Decompressing System
023,359	02/26/93	5,406,285	04/11/95	Digital-to-Analog Converter
026,539	03/13/87	4,847,621	07/11/89	Apparatus for Converging Data Between Digital and Analog Values
382,677	02/02/95	5,554,950	09/10/96	Delay Line providing an Adjustable delay in Response to Binary Input Signals
08/537,491	10/02/95	5,805,173	09/08/98	System and Method for Capturing and Transferring Selected Portions of a Video Stream in a Computer
08/802,042	02/18/97	6,043,844	03/28/00	A Perceptually Motivated Constrained Trellis Based Rate Control Method and Apparatus for Low Bit Rate Video Coding
08/990,279	12/15/97	5,986,691	11/16/99	Cable Modem Optimized for High-Speed Data Transmissions From the Home to the Cable Head
08/798,240	02/12/97	6,359,654	03/19/02	Methods and Systems for Displaying Interlaced Video on Non-Interlaced Monitors
08/720,891	10/03/96	5,940,610	08/17/99	Using Prioritized Interrupt Callback Routines to Process Different Types of Multimedia Information
08/988,548	12/10/97	5,936,660	08/10/99	Digital Video Converter Box for Subscriber/Home With Multiple Television Sets
08/888,910	07/07/97	5,974,478	10/26/99	System and Method for Command Processing or Emulation in a Computer System Using Interrupts, Such as Emulation of DMA Commands Using Burst Mode . . .
08/650,820	05/20/96	6,181,350	01/30/01	Apparatus for, and Method of, Interpolating Between Graphics and Video Pixels in an Expanded Image
09/009,662	01/20/98	6,040,851	03/21/00	Small-Format Subsystem for Broadband Communication Services
08/980,654	12/01/97	6,111,914	08/29/00	Adaptive Entropy Coding in Adaptive Quantization Framework for Video Signal Coding Systems and Processes

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
08/845,594	04/25/97	5,983,315	11/09/99	System for, and Method of, Establishing Priorities in Transferring Data From a Memory to a Plurality of Stages
09/158,802	09/22/98	6,640,328	10/28/03	Method for Detecting Dropouts in Data Delivered Over a Bandwidth-Limited Bus
09/244,642	02/04/99	6,175,389	01/16/01	Comb Filtered Signal Separation
09/272,632	03/18/99	6,724,829	04/20/04	Automatic Power Control for Cable Modem Upstream
09/272,760	03/19/99	6,501,809	12/31/02	Clock/Data Smoother for FEC Decoder and Full Rate DDS Clock Generation
09/239,925	01/28/99	6,441,857	08/27/02	Method and Apparatus for Horizontally Scaling Computer Video Data for Display on a Television
09/239,501	01/28/99	6,819,305	11/16/04	Method and Apparatus for Detection of A Video Display Device
09/198,742	11/24/98	6,118,822	09/12/00	Adaptive Entropy Coding in Adaptive Quantization Framework for Video Signal Coding Systems and Processes
09/504,392	02/15/00	6,684,236	01/27/04	System of and Method For Efficiently Performing Computations Through Extended Booth Encoding Of the Operands Thereto
09/415,612	10/09/99	6,526,070	02/25/03	Method and Apparatus for Upstream Burst Transmission Synchronization in Cable Modems
09/409,820	09/30/99	6,532,511	03/11/03	Asochronous Centralized Multi-Channel DMA Controller
09/777,622	02/05/01	6,718,355	04/06/04	Systems and Methods for a Partial Sum Digital Fir Filter
09/492,962	01/28/00	6,606,724	08/12/03	Architecture and Method for the Improved Decoding of a Serially Concatenated Block and Convolutional Code
09/668,231	09/22/00	6,882,690	04/19/05	SoftTrellis Slicer for Improving the Performance of a Decision-Directed Phase Tracker
09/480,831	01/10/00	6,271,726	08/07/01	Wideband Variable Gain Amplifier

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/476,849	01/03/00	6,581,164	06/17/03	System for Adjusting Clock Frequency Based Upon Amount of Unread Data Stored in Sequential Memory When Reading a New Line of Data Within a Field of Data
09/776,970	02/05/01	6,665,021	12/16/03	System and Process for Filtering Single Tone Signals
09/487,138	01/19/00	6,578,093	06/10/03	Apparatus and Method for Synchronization of Read and Write Pointers in a FIFO
09/634,265	08/08/00	6,865,337	03/08/05	System and Method for Detecting Modifications of Video Signals Designed to Prevent Copying by Traditional Video Tape Recorders
11/096,214	03/31/05	7,123,103	10/17/06	Systems and Methods For Accurate Analog Quadrature Signal Generation Using a Delay Locked Loop
09/450,643	12/16/02	6,727,959	04/27/04	System of and Method for Gamma Correction of Real-Time Video
09/461,647	12/14/99	6,564,045	05/13/03	A Broadband, Quadrature Frequency Doubler and Quadrupler
09/265,277	03/09/99	6,339,658	01/15/02	Error Resilient Still Image Packetization Method and Packet Structure
09/398,376	09/17/99	6,392,672	05/21/02	Adding Method For Ordered Sorting Of A Group of Windows on a Display
09/409,823	09/30/99	6,590,938	07/08/03	A DCT Domain Conversion of a Higher Definition Signal to Lower Definition Signal
09/409,819	09/30/99	6,707,457	03/16/04	Microprocessor Extensions For Two-Dimensional Graphics Processing
09/409,824	09/30/99	6,442,643	08/27/02	System and Method for Resolving Data Transfer Incompatibilities Between PCI and Non-PCI Buses
09/432,992	11/03/99	6,603,813	08/05/03	Video Signal Coding Systems and Processes Using Adaptive Quantization
09/588,992	06/06/00	6,968,020	11/22/05	Frequency Synthesis Scheme to Avoid Gaps and VCO Pulling in DBS Systems

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/489,284	01/21/00	6,539,068	03/25/03	Receiver of Wideband Digital Signal in the Presence of a Narrow Band Interfering Signal
09/611,294	07/07/00	6,642,859	11/04/03	Calibrating for Errors in a Plurality of Signal Sources Such as Current or Voltage Sources
09/497,717	02/04/00	6,731,712	05/04/04	Fully Integrated Broadband Tuner
07/371,167	06/26/89	5,095,525	03/10/92	Memory Transformation Apparatus and Method
09/491,032	01/25/00	RE39,202	07/18/06	Digital Video Converter Box for Subscriber/Home With Multiple Television Sets
09/480,225	01/10/00	6,693,961	02/17/04	A System and Method of Video Frame Memory Reduction For Video Decoders
09/816,621	03/23/01	6,664,841	12/16/03	Method and Apparatus for Conditioning an Analog Signal
09/516,465	03/01/00	6,665,752	12/16/03	Interrupt Driven Interface Coupling a Programmable Media Access Controller and a Process Controller
09/516,284	03/01/00	7,010,802	03/07/06	Programmable Pattern Match Engine
09/516,373	03/01/00	6,629,288	09/30/03	A Single Clock Cycle CRC Engine
09/629,122	07/31/00	6,813,743	11/02/04	A Sliding Window Technique for Map Decoders
09/715,877	11/17/00	6,795,512	09/21/04	System for Carrier Phase Tracking of Coded Symbols Using Reliability Metrics for Symbol Estimates
09/729,652	12/04/00	6,856,656	02/15/05	Iterative Carrier Phase Tracking Decoding System
09/865,958	05/25/01	6,810,502	10/26/04	Iterative Decoder Employing Multiple External Code Error Checks to Lower the Error Floor
10/350,303	01/22/03	7,103,831	09/05/06	Burst Reliability and Error Locator for Trellis Codes
09/617,588	07/18/00	6,754,292	06/22/04	Receiver Circuit
09/698,567	10/26/00	6,765,623	07/20/04	Method and Apparatus For Correcting Phase Imbalance In Received In-Phase and Quadrature Signals

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/785,035	02/16/01	6,816,940	11/09/04	Cable Modem Having A Programmable Media Access Controller
09/788,171	02/14/01	6,769,093	07/27/04	Sychronization of a Communications System
07/990,524	12/15/92	5,272,661	12/21/93	Finite Field Parallel Multiplier
09/815,149	03/22/01	6,922,438	07/26/05	System for MPSK Symbol Hypothesis Testing
231,100	08/11/88	4,928,102	05/22/90	Flash Analog-to-Digital Converter With Logarithmic/Linear Threshold Voltages
597,511	10/12/90	5,059,980	10/22/91	Flash Analog-to-Digital Converter With Logarithmic/Linear Threshold Voltages
09/908,759	07/19/01	6,553,040	04/22/03	Method and Apparatus for Upstream Burst Transmission Synchronization in Cable Modems
09/909,044	07/19/01	6,556,591	04/29/03	Method and Apparatus for Upstream Burst Transmissions Synchronization in Cable Modems
09/992,769	11/06/01	6,895,232	05/17/05	Method and Apparatus for Receiving Radio Frequency Signals
10/013,490	12/13/01	6,973,615	12/06/05	System of and Method for Decoding Trellis Codes
10/013,492	12/13/01	6,865,711	03/08/05	System of and Method for Decoding Trellis Codes
10/105,731	03/22/02	7,106,810	09/12/06	Method and Apparatus for a Demodulator Circuit
10/749,571	12/31/03	7,068,202	06/27/06	Improved Architecture for an Analog-to-Digital Converter
10/749,570	12/31/03	7,088,275	08/08/06	Clocking Scheme for an Algorithmic Analog-to-Digital Converter
10/746,921	12/23/03	7,098,961	08/29/06	Horizontal Sync Pulse Detection Without Amplitude Assumption
10/676,803	09/30/03	6,943,635	09/13/05	Optimum RF VCO Structure
09/039,744	03/16/98	6,169,801	01/02/01	DIGITAL ISOLATION APPARATUS AND METHOD
527,626	05/23/90	5,004,308	04/02/91	Rugate Reflector
130,802	12/06/93	5,422,924	06/06/95	Gain and Offset Control for Charge Based Signals

Application Number	Filed Date	Patent Number	Issued Date	Application Title
08/702,780	08/20/96	5,920,853	07/06/99	SIGNAL-COMPRESSION USING INDEX MAPPING TECHNIQUE FOR SHARING OF QUANTIZATION TABLES
07/353,137	05/16/89	5,056,118	10/08/91	Method and Apparatus for Clock and Data Recovery with High Jitter Tolerance
08/287,017	08/08/94	5,655,132	08/05/97	Register File with Multi-Tasking Support
07/895,969	06/09/92	5,315,651	05/24/94	Active Surge Rejection Circuit
948,515	09/22/92	5,457,455	10/10/95	Real Time Keyboard Scanner
199,437	02/22/94	5,463,633	10/31/95	Use of AT Commands to Test Modem with HP3065
186,939	01/27/94	5,463,336	10/31/95	Supply Sensing Power-On Reset Circuit
270,538	07/05/94	5,541,990	07/30/96	Compensated Hybrid
196,354	02/15/94	5,574,452	11/12/96	Single Bit Bandpass Analog-to-Digital Converter
08/756,203	11/25/96	5,834,953	11/10/98	High Speed Current Sense Amplifier
531,992	09/21/95	5,612,996	03/18/97	Loop Gain Processing System for Speakerphone Applications
531,993	09/21/95	5,646,990	07/08/97	Efficient Speakerphone Anti-Howling System
699,269	08/19/96	5,742,679	04/21/98	Optimized Simultaneous Audio and Data Transmission Using QADM with Phase Randomization
616,421	03/15/96	5,686,847	11/11/97	Reduced Sensitivity Power-On Reset Circuitry
587,755	01/17/96	5,781,132	07/14/98	Error Correcting Decoder
09/028,210	02/23/98	6,161,203	12/12/00	Splitterless Digital Subscriber Line Communication System
09/028,023	02/23/98	6,430,219	08/06/02	Method of an Apparatus for Performing Line Characterization in a Subscriber Line Communication
09/028,141	02/23/98	6,263,077	07/17/01	Splitterless Digital Subscriber Line Communication System

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/028,016	02/23/98	6,445,733	09/03/02	Method of and Apparatus for Performing Line Characterization in a Non-Idle Mode in a Subscriber Line Communication System
09/408,455	09/30/99	6,388,467	05/14/02	High Voltage Tolerant Output Drive for Sustained Tri-State Signal Lines
09/213,961	12/17/98	5,949,819	09/07/99	Method and Apparatus for Training Linear Equalizers in a PCM Modem
09/409,369	09/30/99	6,728,308	04/27/04	Application of the Extended Symbol Rates and Symbol Rate Renegotiation
09/370,313	08/09/99	6,771,393	08/03/04	Transmission Rate Control for Continuous-Tone Facsimile
08/863,829	05/27/97	5,811,706	09/22/98	Synthesizer System Utilizing Mass Storage Devices for Real Time, Low Latency Access of Musical Instrument Digital Samples
08/653,185	05/24/96	5,867,560	02/02/99	Remote Hang Up Detector
09/626,057	07/26/00	6,647,100	11/11/03	Universal Serial Bus Data Pump Command Interpreter
08/828,482	03/31/97	5,909,426	06/01/99	Orthogonal LMS Algorithms for Fast Line Echo Canceler Training
08/721,149	09/26/96	5,870,438	02/09/99	Fast Resynchronization System for High-Speed Data Transmission
09/408,367	07/09/99	6,650,698	11/18/03	Non-Linear Equalization for the Upstream Data Connection of 56K PCM Modems
08/943,484	10/03/97	6,101,216	08/08/00	Splitterless Digital Subscriber Line Communication System
09/164,530	09/30/98	6,434,233	08/13/02	Method and Apparatus for Canceling Periodic Interference Signals in a Digital Data Communication System
08/992,034	12/17/97	6,272,184	08/07/01	A Non-Coherent Frequency Shift Keying Detection Scheme
08/925,552	09/08/97	6,067,326	05/23/00	4X4 Dimensional Block Modulation Code for a PAM-5 Constellation
08/982,400	12/02/97	6,212,227	04/03/01	Constant Envelope Modulation for Splitterless ADSL Transmission
08/982,421	12/02/97	6,151,335	11/21/00	Modulation Switching for Splitterless DSL Transmission

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/009,228	01/20/98	6,023,493	02/08/00	Method and Apparatus for Synchronizing a Data Communication System to a Periodic Digital Impairment
08/838,899	04/11/97	5,916,301	06/29/99	Sample Rate Conversion for Synchronous Variable Rate
09/165,592	09/30/98	6,466,584	10/15/02	System and Method for Performing Digital Subscriber Line (DSL) Modem Communication Over an AC Link Bus
09/164,256	09/30/98	6,263,429	07/17/01	Dynamic Microcode for Embedded Processors
09/162,493	09/29/98	6,414,990	07/02/02	Timing Recovery for a High Speed Digital Data Communication System Based on Adaptive Equalizer Impulse Response Characteristics
09/162,845	09/29/98	6,356,585	03/12/02	Power Cutback in Splitterless ADSL Systems
09/164,155	09/30/98	6,381,266	04/30/02	Method and Apparatus for Identifying the Encoding Type of a Central Office Codec
09/265,480	03/09/99	6,300,824	10/09/01	Analog Offset Cancellation Method and Circuit and Amplifier Using Such Circuit
09/340,255	06/30/99	6,157,257	12/05/00	Low Power Folding Amplifier
09/179,637	10/27/98	6,192,227	02/20/01	A Method for Detecting Nonlinear Distortion Using Moment Invariants
09/237,146	01/25/99	6,389,033	05/14/02	Modem Acceleration in a Multiple AC 97 2.x Codec Configuration
09/161,209	09/25/98	6,389,135	05/14/02	Method and Apparatus for Deriving Power From a Clock Signal Coupled Through Capacitors
09/312,412	05/14/99	6,731,749	05/04/04	Telephone Line Interface Circuit With Intelligent Line Current Control
09/153,952	09/16/98	6,104,230	08/15/00	Electronic Inductor Circuit Using Cascoded Transistors
09/312,218	05/14/99	6,647,114	11/11/03	Telephone Line Interface Circuit With Virtual Impedance
09/165,781	10/02/98	6,163,845	12/19/00	Apparatus and Method for Power Management of Embedded Subsystems

Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/339,353	06/23/99	6,556,622	04/29/03	Seamless Transition Between Communication Characteristics of Communication Devices
09/192,617	11/16/98	6,288,794	09/11/01	An Efficient Variable Sample Rate Converter by Rational Ratios Suitable for Fixed Point DSP or Hardware Implementation
09/274,990	03/23/99	6,385,756	05/07/02	Selection of Functions Within an Integrated Circuit
09/408,639	09/30/99	6,711,138	03/23/04	Braveheart - A Home Access Multiplexer With DSL and Phoneline Home Networking
09/409,368	09/30/99	6,359,972	03/19/02	Line in Use Detection
09/407,465	09/28/99	6,278,387	08/21/01	Method of Slowing and Speeding the Playback of Recorded Audio Sound Without Chanigng the Pitch
08/726,187	10/04/96	5,909,384	06/01/99	System for Dynamically Adapting the Length of a Filter
09/251,696	02/17/99	6,459,430	10/01/02	Efficient Implementation of Multi-Level Resolution Conversion Using Linear Interpolation
09/193,222	11/16/98	6,351,530	02/26/02	Modem Having a Digital High Voltage Isolation Barrier
09/608,233	06/30/00	6,684,319	01/27/04	System for Efficient Operation of a Very Long Instruction Word Digital Signal Processor
09/192,627	11/16/98	6,314,475	11/06/01	Method and Apparatus for Monitoring, Controlling and Configuring Local Communication Devices
09/409,360	09/30/99	6,768,720	07/27/04	Detection of Receive Event on Home Network to Verify Functional Media
09/543,201	04/05/00	6,307,408	10/23/01	Method and Apparatus for Powering Down a Line Driver
09/343,873	01/30/99	6,445,734	09/03/02	Method of Validating Equalizer Training
09/345,269	06/30/99	7,046,382	05/16/06	v.34 hdx fallback to g3 facsimile for t.38 gateways

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
09/309,205	05/10/99	6,195,766	02/27/01	system and method for providing soft audio and soft modem copy protection for hardware interfaces and software code
09/163,054	09/29/98	6,108,720	08/22/00	Communications System Utilizing Non-Fixed Buffer Size
09/250,458	02/16/99	6,351,846	02/26/02	Information Server for Kernel and Passive Mode Systems
09/432,434	11/02/99	6,529,975	03/04/03	Method and Apparatus for Addressing and Controlling Expansion Devices Through An AC-Link And A Codec
09/349,670	07/08/99	6,370,239	04/09/02	Standalone Telephone Answering Machine with Store and Forward Facsimile
09/379,994	08/24/99	6,490,637	12/03/02	Unique Serial Number Method for a System Device
09/224,762	01/04/99	6,075,845	06/13/00	System and Method for Performing Telephone Line-in-use Detection, Extension Pick-up Detection, and Remote Hang-up Detection in a Modem
09/618,336	07/18/00	6,714,645	03/30/04	Modem DAA Without Hookswitch Relay
09/432,141	11/02/99	6,434,633	08/13/02	Method and Apparatus For Facilitating AC-Link Communications Between A Controller and a Slow Peripheral of a Codec
09/406,954	09/28/99	6,452,424	09/17/02	Method and Apparatus for Multiple Channel Signal Processing
09/630,845	08/02/00	6,795,547	09/21/04	Full Duplex Speaker-Phone Providing Increased Loop Stability
09/416,482	10/12/99	6,785,371	08/31/04	Signaling Mechanism for Modem Connection Holding and Reconnecting
09/534,673	03/24/00	6,519,339	02/11/03	Method of Regulating Power Transfer Across an Isolation Barrier
07/521,783	05/10/90	5,051,869	09/24/91	Advanced Co-Fired Multichip/Hybrid Package
06/918,235	10/14/86	4,705,962	11/10/87	Solid State DC Rate of Rise Controlled Switch
09/592,707	06/13/00	6,731,726	05/04/04	Communication on Hold

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09/476,856	01/03/00	6,438,158	08/20/02	Method and Apparatus for Implementing Enhanced Multiple Modulus Conversion Techniques in a Signal Point Mapping Context
09/862,689	05/21/01	7,016,490	03/21/06	Circuit Board Capacitor Structure for Forming a High Voltage Isolation Barrier
09/532,346	03/21/00	6,662,321	12/09/03	Modem Using Phase Coherence to Adapt for Missing Transmission Samples
09/588,830	06/07/00	6,874,041	03/29/05	Autoconfiguration of Communication Device Input or Output Terminal
09/616,097	07/14/00	6,427,011	07/30/02	Modem Data Access Arrangement Without Diode Bridge
09/615,627	07/13/00	6,526,109	02/25/03	Method and Apparatus for Hybrid Smart Center Loop for Clock Date Recovery
09/679,414	10/05/00	6,373,377	04/16/02	Power Supply with Digital Data Coupling for Power-Line Networking
09/785,690	02/16/01	6,437,720	08/20/02	Code Independent Charge Transfer Scheme for Switched-Capacitor Digital-to-Analog Converter
09/603,042	06/26/00	6,356,124	03/12/02	Method and Apparatus For Generating A Digital Sine Wave Signal
09/557,233	04/24/00	6,704,399	03/09/04	Quick Connect Parameter Exchange
09/620,871	07/21/00	6,647,109	11/11/03	Network Telephony
09/678,983	10/04/00	6,741,162	05/25/04	Power Line Networking Apparatus and Method
09/781,617	02/12/01	6,728,817	04/27/04	Integrated Package Bus for Multiple Devices
09/638,995	08/14/00	6,429,870	08/06/02	Data Reduction and Representation Method for Graphic Articulation Parameters (GAPS)
09/573,040	05/17/00	6,301,341	10/09/01	System and Method for Performing Telephone Line-in-use Detection, Extension Pick-up Detection, and Remote Hang-up Detection in a Modem
09/817,827	03/26/01	6,856,607	02/15/05	System and Method for Detecting Valid Indicator Signals

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09/672,160	09/27/00	6,766,383	07/20/04	Packet-Based Direct Memory Access
09/644,806	08/23/00	6,690,776	02/10/04	Communication On Hold Notifier
09/734,848	12/11/00	6,473,870	10/29/02	system and method for providing soft audio and soft modem copy protection for hardware interfaces and software code
09/734,522	12/11/00	6,427,210	07/30/02	Apparatus and Method for Power Management of Embedded Subsystems
09/758,536	01/10/01	6,400,782	06/04/02	A Method of Frequency Domain Filtering Employing a Real To Analytic Transform
09/193,304	11/16/98	6,330,597	12/11/01	Method and Apparatus for Monitoring, Controlling, and Configuring Remote Communictions Devices
09/843,389	04/26/01	6,851,003	02/01/05	Integrated Packet Bus With Enhanced Bandwidth
10/016,194	11/02/01	7,006,623	02/28/06	Circuit for Reducing Voltage Peak in Interfacing With a Telephone Line
09/910,289	07/19/01	7,061,976	06/13/06	Multiple Symbol Rate Burst Equalizer Training
09/912,283	07/24/01	7,016,371	03/21/06	Multi-Mode Adaptive Filter
09/626,435	07/27/00	6,975,585	12/13/05	Slotted Synchronous Frequency Division Multiplexing for Multi-Drop Networks
09/849,500	05/04/01	RE38,678	12/28/04	Method and Apparatus for Synchronizing a Data Communication System to a Periodic Digital Impairment
09/876,454	06/06/01	6,854,059	02/08/05	Method and Apparatus for Medium Access Control in Powerline Communication Network Systems
09/976,883	10/12/01	6,480,533	11/12/02	Method and Apparatus for Receiving Control in a Data Communication System Having a Fully Digital Communication Channel
10/034,682	12/29/01	6,693,998	02/17/04	Error Correction and Compression Parameter Exchange During Modem Training Phase
10/352,754	01/27/03	6,985,566	01/10/06	Point of Sale for High-Speed Communications

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Application Number	Filed Date	Patent Number	Issued Date	Application Title
10/607,244	06/25/03	6,842,509	01/11/05	Signaling Mechanism for Modem Connection Holding and Reconnecting
10/640,102	08/12/03	6,922,467	07/26/05	Quick Connect Parameter Exchange
09/121,475	07/23/98	6,202,165	03/13/01	Photonic Clock Distribution Method and Apparatus for Electronic Systems
09/121,476	07/23/98	6,714,260	03/30/04	Monolithic Generation of RF for Wireless Transmission of Video
443,456	05/18/95	5,627,396	05/06/97	Micromachined Relay and Method of Forming the Relay
445,139	05/19/95	5,620,933	04/15/97	Micromachined Relay and Method of Forming the Relay
119,741	11/12/87	4,878,179	10/31/89	Interactive Diagnostic Methodology and Apparatus for Microelectronic Devices
08/280,417	07/26/94	5,440,162	08/08/95	ESD Protection for Submicron CMOS Circuits
08/715,234	09/18/96	5,764,074	06/09/98	System for, and Method of, Minimizing Noise in an Integrated Circuit Chip
338,012	11/10/94	5,596,284	01/21/97	System for, and Method of, Minimizing Noise in an Integrated Circuit Chip
012,055	02/01/93	5,479,042	12/26/95	Micromachined Relay and Method of Forming the Relay
08/665,783	06/18/96	6,121,087	09/19/00	Integrated Circuit Device with Embedded Flash Memory and Method for Manufacturing Same
09/094,735	06/15/98	6,037,743	03/14/00	A Battery Charger and Power Source Employing an Environmental Energy Extractor and a Method Related Thereto
09/045,276	03/20/98	5,949,218	09/07/99	Methods and Apparatus for Managing the Charging and Discharging of a Lithium Battery
09/163,776	09/30/98	6,421,757	07/16/02	Method and Apparatus for Controlling the Programming and Erasing of Flash Memory
09/143,584	08/31/98	6,166,585	12/26/00	Methods and Apparatus for a High Efficiency Charge Pump
09/411,417	10/01/99	6,550,046	04/15/03	Method for Automated Placement of Cells in an Integrated Circuit Layer

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09/467,532	12/20/99	6,104,654	08/15/00	High Speed Sensing of Dual Port Static RAM Cell
09/467,285	12/20/99	6,134,165	10/17/00	High Speed Sensing of Dual Port Static RAM Cell
931,324	11/17/86	4,740,414	04/26/88	Ceramic/Organic Multilayer Interconnection Board
645,428	01/24/91	5,097,121	03/17/92	Beveled Edge Impurity Band Conduction Detector
07/471,152	01/26/90	5,103,183	04/07/92	Method of Profiling Compensator Concentration in Semiconductors
310,034	02/10/89	5,366,934	11/22/94	Method for Sulfide Surface Passivation
07/416,192	10/02/89	5,055,805	10/08/91	High Speed Polarization Switch Array for Selecting a Particular Orthogonal Polarization
09/863,089	05/22/01	6,459,562	10/01/02	High Density Metal Insulator Metal Capacitors
08/732,752	10/18/96	5,654,862	08/05/97	Method and Apparatus for Coupling Multiple Independent On-Chip Vdd Busses to an ESD Core Clamp
09/672,165	09/27/00	6,643,109	11/04/03	Fully Synthesisable and Highly Area Efficient Very Large Scale Integration (VLSI) Electrostatic Discharge (ESD) Protection Circuit
09/667,364	09/21/00	6,518,604	02/11/03	Diode With Variable Width Metal Stripes for Improved Protection Against Electrostatic Discharge (ESD) Current Failure
09/879,142	06/12/01	6,728,942	04/27/04	Method and Systems for Predictive MOSFET Layout Generation with Reduced Design Cycle
10/029,476	10/24/01	6,839,887	01/04/05	Method and System for Predictive Multi-Component Circuit Layout Generation with Reduced Design Cycle
09/941,883	08/28/01	6,588,002	07/01/03	Method and System for Predictive Layout Generation for Inductors With Reduced Design Cycle
629,926	04/12/96	5,940,686	08/17/99	Method for Manufacturing Multi-Chip Modules Utilizing Direct Lead Attach

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10/005,564	11/08/01	6,534,854	03/18/03	A Pin Grid Array Package With Controlled Impedance Pins
10/325,618	12/20/02	6,925,627	08/02/05	Method and Apparatus for Power Routing in an Integrated Circuit
10/438,664	05/14/03	6,864,518	03/08/05	Bit cells having offset contacts in a memory array
10/637,324	08/08/03	6,927,458	08/09/05	Ballasting MOSFETs Using Staggered, Segmented Diffusions
08/861,669	05/22/97	6,101,228	08/08/00	Receiver of Wideband Digital Signal in the Presence of a Narrow Band Interfering Signal
994,931	12/23/92	5,521,499	05/28/96	Digital Controlled Phase Shifter
263,602	06/22/94	5,528,633	06/18/96	Tuner With Quadrature Downconverter for Pulse Amplitude Modulated Data Applications
846,545	04/03/86	4,899,153	02/06/90	Fast High-Resolution Analot-to-Digital Converter
09/146,057	09/02/98	6,055,024	04/25/00	Adaptive Method for Y-C Separation in Video Signals
09/087,736	05/29/98	6,100,937	08/08/00	Method and System for combining Multiple Images into a Single Higher-Quality Image
08/724,168	09/30/96	5,880,980	03/09/99	Sample Rate Conversion for Synchronous Variable Rate
09/358,999	07/22/99	6,353,413	03/05/02	Multi-Function Universal Controller and Locator Systems
08/912,547	08/18/97	5,922,052	07/13/99	Fast Ethernet Combination Chaining of Auto-Negotiations for Multiple Physical Layer Capability
09/095,519	06/10/98	6,008,446	12/28/99	Synthesizer System Utilizing Mass Storage Devices for Real Time, Low Latency Access of Musical Instrument Digital Samples
09/007,978	01/16/98	6,069,631	05/30/00	Coding of Facial Animation Parameters (FAPs) For Transmission of Synthetic Talking Head Video Over Band Limited Channels
09/127,466	07/31/98	6,130,679	10/10/00	Data Reduction and Representation Method for Graphic Articulation Parameters (GAPS)

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09/075,451	05/08/98	6,128,373	10/03/00	Programmable Data Access Arrangement Having Combined Command Signals
09/096,851	06/11/98	6,104,791	08/15/00	System and Method for Performing Telephone Line-in-use Detection, Extension Pick-up Detection, and Remote Hang-up Detection in a Modem
09/397,413	09/16/99	6,700,974	03/02/04	Switching Power Supply For Generating A Ringing Voltage
08/080,907	06/21/93	5,381,095	01/10/95	Method of Estimating Location and Orientation of Magnetic Dipoles Using Extended Kalman Filtering and Schweppe Likelihood Ratio Detection
510,365	04/17/90	5,113,399	05/12/92	Memory Test Methodology
07/580,042	09/10/90	5,058,265	10/22/91	Method for Packaging a Board of Electronic Components
031,733	03/30/87	4,740,386	04/26/88	Method for Depositing a Ternary Compound Having a Compositional Profile
09/106,325	06/29/98	6,028,801	02/22/00	High Speed Sensing of Dual Port Static RAM Cell
09/415,396	10/08/99	6,738,796	05/18/04	Optimization of Memory Requirements for Multi-Threaded Operating Systems
09/265,486	03/09/99	6,490,250	12/03/02	Elementary Stream Multiplexer
09/439,920	11/12/99	6,898,243	05/24/05	Apparatus and Method for Down-Conversion Video De-Interlacing
09/507,305	02/18/00	6,782,135	08/24/04	Apparatus and Method for Adaptive Digital Video Quantization

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09/792,152	02/22/01	6,990,529	01/24/06	Unified Algorithm For Frame Scheduling And Buffer Management In Differentiated Services Networks
09/794,184	02/26/01	6,954,424	10/11/05	Credit-Based Pacing Scheme For Heterogeneous Speed Frame Forwarding
10/830,570	04/23/04			Signaling Extended Functionality And Management Information In A Network
10/830,575	04/23/04			Managing Coexistence Of Separate Protocols Sharing The Same Communications Channel
10/861,064	06/04/04			Managing An Access Point In The Presence Of Separate Protocols That Share The Same Communications Channel
10/861,065	06/04/04			Intelligent Downstream Traffic Delivery To Multi-Protocol Stations
10/886,025	07/08/04			Adaptive Frequency Equalizer
10/922,985	08/23/04			Power-Based Hardware Diversity
11/203,617	08/12/05			Systems And Methods For Decreasing Latency In A Digital Transmission System
11/314,149	12/21/05			Systems And Methods For Device Discovery
11/433,599	05/12/06			Coding Systems And Methods

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09/255,235	02/22/1999	6,345,072	2/05/02	Universal DSL Link Interface Between A DSL Digital Controller And A DSL Codec
09/263,160	03/05/1999	6570912	05/27/2003	Hybrid Software/Hardware Discrete Multi-Tone Transceiver
09/36,0252	07/23/1999	6243414	06/05/2001	Method And Apparatus For Data Transmission
09/701,810	12/01/2000	6771697	08/03/2004	Spread Spectrum Handshake For Digital Subscriber Line Telecommunications Systems
09/893,383	06/27/2001	6567465	05/20/2003	DSL Modem Utilizing Low Density Parity Check Codes
10/054,294	11/13/2001	6804292	10/12/2004	Broadband I/O Circuits, Interface And Bus
10/054,327	11/13/2001	6904083	06/07/2005	DSL Link With Embedded Control And Multi-Channel Capability
10/054,410	11/13/2001	6836510	12/28/2004	DSL Link With Scaleable Performance
10/996,054	11/24/2004			Method and system for enhancing bit rate in DMT quad spectrum systems
11/035,065	01/14/2005			Power management for wireless direct link
11/239,657				
11/513,089				
11/513,096				
11/556,916				
11/557,516				

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09/496,793	02/02/2000	6,985,548	01/10/2006	System And Method For Timing Recovery In A Discrete Multi-Tone System
09/643,567	08/22/2000	6,697,873	02/24/2004	High Speed Mac Address Search Engine
09/756,570	01/08/2001	6,868,095	03/15/2005	Control Channel Implementation In A Packet Switched Communications Network
09/899,426	07/05/2001	6,775,722	08/10/2004	Efficient Data Retrieval From Input Coupling Queues
09/935,533	08/23/2001	6,999,416	02/14/2006	Buffer Management For Support Of Quality-Of-Service Guarantees And Data Flow Control In Data Switching
09/966,691	09/28/2001	7,082,138	07/25/2006	Internal Communication Protocol For Data Switching Equipment

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Application Number	Filed Date	Title
11/239,657	28-Sep-2005	Non-interfering Signaling and Reception of Overlapping Single Carrier Transmissions Over Delay Spread Channels
11/513,089	31-Aug-2006	Minimum Power Leakage Windowing for VDSL Using Least Square Technique
11/513,096	31-Aug-2006	Techniques to Resolve SNR-Margin Difference between Fast and Interleave Channels under Colored Noise Condition for DMT-Based DSL System
11/556,916	06-Nov-2006	VOIP-Aware PS-POLL
11/557,516	08-Nov-2006	Collision Avoidance Systems and Methods

Application Number	Filed Date	Patent Number	Issued Date	Application Title
11/083,080	03/18/05			Multichannel MAC data stream for wireless communication