

PATENT ASSIGNMENT

Electronic Version v1.1

Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
Industrial Technology Research Institute	06/10/2006
RECEIVING PARTY DATA	
Name:	Transpacific IP Ltd.
Street Address:	10th Fl.-1A, No. 207 Dun Hua N. Road
City:	Taipei City 105
State/Country:	TAIWAN
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	11598154
CORRESPONDENCE DATA	
Fax Number:	(503)439-6558
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	503-439-6500
Email:	jflynn@bltg-ip.com
Correspondent Name:	Berkeley Law & Technology Group LLP
Address Line 1:	1700 NW 167th Place, Suite 240
Address Line 2:	Attn: Julianne Flynn
Address Line 4:	Beaverton, OREGON 97006
ATTORNEY DOCKET NUMBER:	112.P91073RE
NAME OF SUBMITTER:	Julianne Flynn
Total Attachments: 3 source=JJF_112.P91073#page1.tif source=JJF_112.P91073#page2.tif source=JJF_112.P91073#page3.tif	

CH \$40.00 11598154

500247485

PATENT
REEL: 019073 FRAME: 0121

ASSIGNMENT OF PATENT

Atty Dkt No.:

BHT/3111-779

WHEREAS, **Industrial Technology Research Institute**, of Hsinchu, Taiwan, whose address is No. 195, Sec. 4, Chung Hsing Rd., Chutung, Hsinchu, Taiwan, 310, R.O.C., is the owner of the entire right, title and interest of the following U.S. Patent(s):

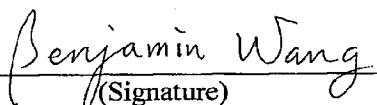
Patent No. Title

SEE ATTACHED APPENDIX A
(2 pages indicating 29 separate U.S. Patents)

WHEREAS, **TransPacific IP Ltd.**, of Taipei, Taiwan, whose address is 10th Fl.-1A, No.207, Dunhua N. Road, Taipei City 105, Taiwan, R.O.C., hereinafter referred to as "assignee", is desirous of acquiring the entire right, title and interest in the same;

NOW, THEREFORE, for good and valuable consideration, the receipt whereof is acknowledged, we, the patent owners, by these presents do sell, assign and transfer unto said assignee the entire right, title and interest in and to the aforementioned Patents; the same to be held and enjoyed by the said assignee for his own use and behoof, and for his legal representatives and assigns, to the full end of the term for which said Patents is granted, as fully and entirely as the same would have been held by me had this assignment and sale not been made.

Executed this 10th day of June, 2006, at Hsinchu


(Signature)
Benjamin Wang

Depuly General Director
(Title)

PATENT
REEL: 018498 FRAME: 0273

PATENT
REEL: 019073 FRAME: 0122

ASSIGNMENT OF PATENT APPENDIX A		Atty Dkt No.: BHT/3111-779
PATENT NOS.	TITLES	
5,754,380	CMOS OUTPUT BUFFER WITH ENHANCED HIGH ESD PROTECTION CAPABILITY	
5,637,900	LATCHUP-FREE FULLY-PROTECTED CMOS ON-CHIP ESD PROTECTION CIRCUIT	
5,572,394	CMOS ON-CHIP FOUR-LVTSCR ESD PROTECTION SCHEME	
5,781,026	CMOS LEVEL SHIFTER WITH STEADY-STATE AND TRANSIENT DRIVERS	
5,808,492	CMOS BIDIRECTIONAL BUFFER WITHOUT ENABLE CONTROL SIGNAL	
5,698,993	CMOS LEVEL SHIFTING CIRCUIT	
5,708,386	CMOS OUTPUT BUFFER WITH REDUCED L-DI/DT NOISE	
6,008,684	CMOS OUTPUT BUFFER WITH CMOS-CONTROLLED LATERAL SCR DEVICES	
5,854,560	CMOS OUTPUT BUFFER HAVING A HIGH CURRENT DRIVING CAPABILITY WITH LOW NOISE	
5,757,242	LOW POWER CONSUMPTION OSCILLATORS WITH OUTPUT LEVEL SHIFTERS	
5,852,315	N-SIDED POLYGONAL CELL LAYOUT FOR MULTIPLE CELL TRANSISTOR	
5,901,022	CHARGED DEVICE MODE ESD PROTECTION CIRCUIT	
5,850,159	HIGH AND LOW SPEED OUTPUT BUFFER WITH CONTROLLED SLEW RATE	
6,094,086	HIGH DRIVE CMOS OUTPUT BUFFER WITH FAST AND SLOW SPEED CONTROLS	
5,917,348	CMOS BIDIRECTIONAL BUFFER FOR MIXED VOLTAGE APPLICATIONS	
6,060,922	DUTY CYCLE CONTROL BUFFER CIRCUIT WITH SELECTIVE FREQUENCY DIVIDING FUNCTION	
6,002,599	VOLTAGE REGULATION CIRCUIT WITH ADAPTIVE SWING CLOCK SCHEME	
6,060,906	BIDIRECTIONAL BUFFER WITH ACTIVE PULL-UP/LATCH CIRCUIT FOR MIXED-VOLTAGE APPLICATIONS	
5,999,392	RESET CIRCUIT WITH TRANSIENT DETECTION FUNCTION	
6,444,295	METHOD FOR IMPROVING INTEGRATED CIRCUITS BONDING FIRMNESS	

6,658,597	METHOD AND APPARATUS FOR AUTOMATIC RECOVERY OF MICROPROCESSORS/MICROCONTROLLERS DURING ELECTROMAGNETIC COMPATIBILITY (EMC) TESTING
6,465,283	STRUCTURE AND FABRICATION METHOD USING LATCH-UP IMPLANTATION FOR IMPROVING LATCH-UP IMMUNITY IN CMOS FABRICATION PROCESS
6,815,775	ESD PROTECTION DESIGN WITH TURN-ON RESTRAINING METHOD AND STRUCTURES
6,750,515	SCR DEVICES IN SILICON-ON-INSULATOR CMOS PROCESS FOR ON-CHIP ESD PROTECTION
6,576,974	BIPOLAR JUNCTION TRANSISTORS FOR ON-CHIP ELECTROSTATIC DISCHARGE PROTECTION AND METHODS THEREOF
6,838,707	BI-DIRECTIONAL SILICON CONTROLLED RECTIFIER FOR ELECTROSTATIC DISCHARGE PROTECTION
6,599,578	METHOD FOR IMPROVING INTEGRATED CIRCUITS BONDING FIRMNESS
6,882,009	ELECTROSTATIC DISCHARGE PROTECTION DEVICE AND METHOD OF MANUFACTURING THE SAME
6,964,883	BI-DIRECTIONAL SILICON CONTROLLED RECTIFIER FOR ELECTROSTATIC DISCHARGE PROTECTION

RECORDED: 11/03/2006

PATENT
REEL: 018498 FRAME: 0275

RECORDED: 03/27/2007

PATENT
REEL: 019073 FRAME: 0124