

**PATENT ASSIGNMENT**

Electronic Version v1.1  
 Stylesheet Version v1.1

<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	First Amendment to Patent Security Agreement

**CONVEYING PARTY DATA**

Name	Execution Date
Newport Fab, LLC	02/28/2007

**RECEIVING PARTY DATA**

<b>Name:</b>	Wachovia Capital Finance Corporation (Western)
<b>Street Address:</b>	251 S. Lake Ave.
<b>Internal Address:</b>	Suite 900
<b>City:</b>	Pasadena
<b>State/Country:</b>	CALIFORNIA
<b>Postal Code:</b>	91101

**PROPERTY NUMBERS Total: 63**

Property Type	Number
Patent Number:	7173318
Patent Number:	6965132
Patent Number:	7183627
Patent Number:	7132700
Patent Number:	7064073
Patent Number:	7078744
Patent Number:	6979626
Patent Number:	7064415
Patent Number:	7015115
Patent Number:	7033898
Patent Number:	6995449
Patent Number:	7078310
Patent Number:	7041569
Patent Number:	4497685

**CH \$2520.00 7173318**

Patent Number:	5031014
Patent Number:	5097316
Patent Number:	4444617
Patent Number:	4593453
Patent Number:	7154161
Patent Number:	7063988
Patent Number:	7078786
Patent Number:	6992338
Patent Number:	7064361
Patent Number:	6972442
Patent Number:	7041564
Patent Number:	4506437
Patent Number:	4477962
Patent Number:	4459937
Patent Number:	4396479
Patent Number:	4507852
Patent Number:	4639142
Patent Number:	7056822
Patent Number:	6984577
Patent Number:	6995068
Patent Number:	7049246
Patent Number:	7109125
Patent Number:	6586307
Patent Number:	6838352
Patent Number:	7060557
Application Number:	09833953
Application Number:	11175720
Application Number:	10892015
Application Number:	11112194
Application Number:	11198425
Application Number:	10952256
Application Number:	11084391
Application Number:	10970645
Application Number:	11018164
Application Number:	11086168

Application Number:	10997638
Application Number:	10997534
Application Number:	11525457
Application Number:	11121360
Application Number:	11146537
Application Number:	60848973
Application Number:	11641500
Application Number:	11542088
Application Number:	11641296
Application Number:	11641504
Application Number:	11641376
Application Number:	11641925
Application Number:	60276277
Application Number:	11003572

**CORRESPONDENCE DATA**

Fax Number: (866)459-2899  
*Correspondence will be sent via US Mail when the fax attempt is unsuccessful.*  
Phone: 202-783-2700  
Email: oleh.hereliuk@federalresearch.com  
Correspondent Name: CBCInnovis dba Federal Research  
Address Line 1: 1023 Fifteenth Street, NW, Ste 401  
Address Line 2: attn: Oleh Hereliuk  
Address Line 4: Washington, DISTRICT OF COLUMBIA 20005

ATTORNEY DOCKET NUMBER:	380889
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NAME OF SUBMITTER:	LaKeeshia Saunders
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Total Attachments: 9  
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## RECORDATION FORM COVER SHEET PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

**1. Name of conveying party(ies)**

JAZZ SEMICONDUCTOR, INC.

Additional name(s) of conveying party(ies) attached?  Yes  No

**2. Name and address of receiving party(ies)**

Name: Wachovia Capital Finance Corporation (Western)

Internal Address: \_\_\_\_\_

Street Address: 251 S. Lake Ave., Suite 900

City: Pasadena

State: California

Country: USA Zip: 91101

Additional name(s) & address(es) attached?  Yes  No

**3. Nature of conveyance/Execution Date(s):**

Execution Date(s) February 28, 2007

- |   |   |
|---|---|
| <input type="checkbox"/> Assignment   | <input type="checkbox"/> Merger         |
| <input type="checkbox"/> Security Agreement                                       | <input type="checkbox"/> Change of Name |
| <input type="checkbox"/> Joint Research Agreement                                 |   |
| <input type="checkbox"/> Government Interest Assignment                           |   |
| <input type="checkbox"/> Executive Order 9424, Confirmatory License               |   |
| <input checked="" type="checkbox"/> Other <u>Assignment of Security Agreement</u> |   |

**4. Application or patent number(s):**

This document is being filed together with a new application.

A. Patent Application No.(s)

B. Patent No.(s)

09/754,806 (See Exhibit A)

Additional numbers attached?  Yes  No

**5. Name and address to whom correspondence concerning document should be mailed:**

Name: Federal Research Co. LLC

Internal Address: Attention: Oleh Hereliuk

Street Address: 1023 15th Street, NW

Suite 401

City: Washington

State: D.C. Zip: 20005

Phone Number: (800) 846-3190

Fax Number: \_\_\_\_\_

Email Address: \_\_\_\_\_

**6. Total number of applications and patents involved:** 63**7. Total fee (37 CFR 1.21(h) & 3.41)** \$ 1,590.00

- Authorized to be charged by credit card  
 Authorized to be charged to deposit account  
 Enclosed  
 None required (government interest not affecting title)

**8. Payment Information**

a. Credit Card Last 4 Numbers \_\_\_\_\_  
Expiration Date \_\_\_\_\_

b. Deposit Account Number \_\_\_\_\_  
Authorized User Name \_\_\_\_\_

**9. Signature:**

  
Signature

March 19, 2007

Date

Christopher Exberger, Esq.  
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents:

9

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:  
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

## FIRST AMENDMENT TO PATENT SECURITY AGREEMENT

THIS FIRST AMENDMENT TO PATENT SECURITY AGREEMENT (this "**Amendment**"), dated as of February 28, 2007, is entered into between NEWPORT FAB, LLC, a Delaware limited liability company, with its chief executive office located at 4321 Jamboree Road, Newport Beach, California 92660 ("**Pledgor**"), and WACHOVIA CAPITAL FINANCE CORPORATION (WESTERN) ("**Wachovia**"), a California corporation, with an office at 251 South Lake Avenue, Suite 900, Pasadena, California 91101, in its capacity as administrative agent for the Lenders (as defined below) (in such capacity, "**Pledgee**").

### RECITALS

A. Pledgor and Wachovia are parties to that certain Patent Security Agreement, dated as of January 6, 2006, and recorded with the United States Patent and Trademark Office on January 20, 2006 at Reel 017223, Frame 0083 (as the same may be amended, modified, supplemented or restated from time to time, the "**Patent Security Agreement**") that was entered into and delivered in connection with that certain Loan and Security Agreement, dated as of January 6, 2006, among Wachovia, as Lender, and Pledgor, and Jazz Semiconductor, Inc., a Delaware corporation, as co-borrowers (each a "**Borrower**" and collectively "**Borrowers**") (as amended, the "**Original Loan Agreement**" and together will all agreements entered into in connection therewith, the "**Original Financing Agreements**").

B. The Borrowers have entered into that certain Amended and Restated Loan and Security Agreement, dated as of the date hereof (as the same may be amended, modified, supplemented or restated from time to time, the "**Loan Agreement**"), with the financial institutions from time to time party thereto as lenders (the "**Lenders**") and Wachovia as administrative agent for the Lenders (in such capacity, the "**Agent**"), pursuant to which the Original Loan Agreement has been amended and restated in its entirety to set forth, among other things, (a) the multi-lender structure of the loan facility, (b) the appointment by the Lenders of Wachovia as Agent for the benefit of the Lenders and (c) the extension of further loans and financial accommodations to the Borrowers.

C. Since the date of the Patent Security Agreement, Pledgor has acquired or made Pledgee aware of the existence of the patents and related registrations and applications set forth on Exhibit A hereto (the "**New Patents**")

D. As an inducement for and in consideration of the Lenders making loans and advances and providing other financial accommodations to Borrowers pursuant to the Loan Agreement and the Financing Agreements (as defined in the Loan Agreement), Pledgor hereby agrees in favor of Pledgee, for the benefit of the Lenders, to amend the Patent Security Agreement in order to, among other things, (a) continue the security interest created under the Patent Security Agreement with respect to all of Pledgor's right, title and interest in the Collateral (as defined in the Patent Security Agreement), (b) reflect that Wachovia in its capacity as the Agent for the benefit of the Lenders, rather than Wachovia in its capacity as the sole Lender, is the Pledgee, (c) cover the New Patents.

## AGREEMENT

NOW, THEREFORE, in consideration of the foregoing and the mutual covenants herein contained, and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties hereto hereby agree as follows:

### 1. Amendment and Reaffirmation.

(a) Each reference in the Patent Security Agreement to Pledgee and each reference thereto in all other documents or agreements related thereto, shall mean and be a reference to Wachovia in its capacity as Agent for the benefit of the Lenders rather than Wachovia in its capacity as the sole Lender.

(b) Each reference in the Patent Security Agreement to “the Financing Agreements”, “thereof”, “therein” or words of like import referring to the Original Loan Agreement or the Original Financing Agreements, and each reference thereto in all other documents or agreements related thereto, shall mean and be a reference to the Loan Agreement (as defined herein) and the Financing Agreements (as defined in the Loan Agreement).

(c) The Patent Security Agreement is hereby amended to add the New Patents to Exhibit A of the Patent Security Agreement, and the term “Patents” as defined and used in the Patent Security Agreement shall include the New Patents.

(d) This Amendment shall be deemed to be an amendment to the Patent Security Agreement and the Patent Security Agreement, as amended hereby, is hereby reaffirmed, ratified, approved and confirmed in each and every respect. Without limiting the foregoing, Pledgor reaffirms, ratifies, approves, confirms and re-grants the security interest granted to Pledgee as provided in the Patent Security Agreement as amended hereby.

2. Defined Terms. Unless otherwise defined herein, terms used in this Amendment that are defined in the Loan Agreement shall have the same meanings herein as in the Loan Agreement.

3. Reference to and Effect on the Patent Security Agreement, Loan Agreement and Financing Agreements.

(a) Upon and after the effectiveness of this Amendment: (i) each reference in the Patent Security Agreement to “this Security Agreement”, “hereunder”, “hereof”, “herein” or words of like import referring to the Patent Security Agreement, and each reference in all other documents or agreements related thereto, including, without limitation, the Loan Agreement and the Financing Agreements, referring to the Patent Security Agreement, shall mean and be a reference to the Patent Security Agreement as modified and amended hereby; and (ii) each reference in the Patent Security Agreement to “the Financing Agreements”, “a Financing Agreement”, “thereunder”, “thereof”, “therein” or words of like import referring to the Financing Agreements or any Financing Agreement, as applicable, shall include the Patent Security Agreement as modified and amended hereby as a Financing Agreement or such Financing Agreement, as applicable.

(b) To the extent that any terms and conditions in any of the Loan Agreement, the Financing Agreements or any documents or agreements related thereto shall contradict or be in conflict with any terms or conditions of the Patent Security Agreement, after giving effect to this Amendment, such terms and conditions are hereby deemed modified or amended accordingly to reflect the terms and conditions of the Patent Security Agreement as modified or amended hereby.

4. Successors and Assigns. This Amendment shall be binding upon and inure to the benefit of Pledgor, Pledgee, each Lender, all future holders of the Obligations and their respective successors and assigns, except that Pledgor may not assign or transfer any of its rights or obligations under this Amendment or the Patent Security Agreement without the prior written consent of Pledgee.

5. Severability. If any part of this Amendment is contrary to, prohibited by, or deemed invalid under applicable laws or regulations, such provision shall be inapplicable and deemed omitted to the extent so contrary, prohibited or invalid, but the remainder hereof shall not be invalidated thereby and shall be given effect so far as possible.

6. Counterparts, etc. This Amendment may be executed in any number of counterparts, each of which shall be an original, but all of which taken together shall constitute one and the same agreement. Delivery of an executed counterpart of this Amendment by telefacsimile shall have the same force and effect as the delivery of an original executed counterpart of this Amendment. Any party delivering an executed counterpart of this Amendment by telefacsimile shall also deliver an original executed counterpart, but the failure to do so shall not affect the validity, enforceability or binding effect of this Amendment.

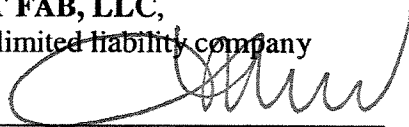
7. No Other Changes. Except as explicitly amended by this Amendment, all of the terms and conditions of the Patent Security Agreement shall remain in full force and effect.

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IN WITNESS WHEREOF, the parties hereto have caused this Amendment to be duly executed and delivered by its officers thereunto duly authorized as of the date first above written.

**PLEDGOR**

**NEWPORT FAB, LLC,**  
a Delaware limited liability company

By:   
Name: Sha Li  
Title: PRESIDENT & CEO

[Signature page First Amendment to Patent Security Agreement]



**PLEDGEE**

**WACHOVIA CAPITAL FINANCE  
CORPORATION (WESTERN),**  
a California corporation

By: Kate W. Cook  
Name: Kate W. Cook  
Title: Managing Director

[Signature page to First Amendment to Patent Security Agreement]

## EXHIBIT A

### List of Patents

<b>Title</b>	<b>Patent No.</b>	<b>Filing Date</b>	<b>Issue Date</b>
On-Chip Inductors	09/754,806 7,173,318		2/6/2007
Polycrystalline Silicon Emitter Having an Accurately Controlled Critical Dimension	10/321,877 6,965,132		11/15/2005
Independent Control of Polycrystalline Silicon-Germanium in an HBT and Related Structure	10/054,438 7,183,627		2/27/2007
Low Cost Fabrication Of High Resistivity Resistors	09/833,953	4/11/2001	Pending
SIGE Layer Having Small Poly Grains	10/915,797 7,132,700		11/7/2006
Technique for Reducing Contaminants in Fabrication of Semiconductor Wafers	10/434,961 7,064,073		6/20/2006
Transistor Emitter Having Alternating Undoped and Doped Layers	10/888,406 7,078,744		7/18/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Having Increased Manufacturability and Related Structure	10/442,449 6,979,626		12/27/2005
Fabricating a Self-Aligned Bipolar Transistor Having Increased Manufacturability	11/175,720	7/6/2005	Pending
Self-Aligned Bipolar Transistor Having Increased Manufacturability	10/995,769 7,064,415		6/20/2006
Method for Forming Deep Trench Isolation and Related Structure	10/371,307 7,015,115		3/21/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Having Recessed Spacers	10/865,153 7,033,898		4/25/2006
Bipolar Transistor Fabricated in a BiCMOS Process	10/892,015	7/14/2004	Pending
Densely Packed Metal Segments Patterned in a Semiconductor Die	11/112,194	4/22/2005	Pending
Deep N Wells in Triple Well Structures	11/198,425	8/5/2005	Pending
Deep Trench Isolation Region with Reduced-Size Cavities in Overlying Field Oxide	10/842,943 6,995,449		2/7/2006
High Density Composite MIM Capacitor with Flexible Routing in Semiconductor Dies	10/850,187 7,078,310		7/18/2006
Method for Fabricating a High Density Composite MIM Capacitor with Reduced Voltage Dependence in Semiconductor Dies	10/712,067 7,041,569		5/9/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Without Spacers	10/952,256	9/28/2004	Pending
Small Area High Value Resistor with Greatly Reduced Parasitic Capacitance	06/544,914 4,497,685		2/5/1985
Lateral Transistor Separated from Substrate by Intersecting Slots Filled with Substrate Oxide for Minimal Interference Therefrom	07/062,007 5,031,014		7/9/1991
Complementary NPN and PNP Lateral Transistors Separated from Substrate by Intersecting Slots Filled with Substrate Oxide for Minimal Interference Therefrom	07/068,383 5,097,316		3/17/1992
Reactive Ion Etching of Molybdenum Silicide and N+ Polysilicon	06/456,183 4,444,617		4/24/1984
Two-Level Transistor Structures and Method Utilizing Minimal Area Therefor	06/621,773 4,593,453		6/10/1986
Composite Ground Shield for Passive Components in a Semiconductor Die	10/826,507 7,154,161		12/26/2006

<b>Title</b>	<b>Patent No.</b>	<b>Filing Date</b>	<b>Issue Date</b>
Circuit for Detecting Arcing in an Etch Tool During Wafer Processing	10/758,494 7,063,988		6/20/2006
Integration of SIGE NPN and Vertical PNP Devices on a Substrate	11/084,391	3/17/2005	Pending
Method for Opto-Electronic Integration on a SOI Substrate and Related Structure	10/970,645	10/20/2004	Pending
SOI Substrate for Integration of Opto-Electronics with SiGe BiCMOS	11/018,164	12/20/2004	Pending
Method for Effective BiCMOS Process Integration	11/086,168	3/21/2005	Pending
Method for Fabricating a MIM Capacitor Having Increased Capacitance Density and Related Structure	10/997,638	11/23/2005	Pending
Method and Structure for Integration of Phosphorus Emitter in an NPN Device in a BiCMOS Process	10/997,534	11/23/2004	Pending
Integration of Phosphorus Emitter in an NPN Device in a BiCMOS Process	11/525,457	9/21/2006	Pending
Method for Fabricating a MIM Capacitor High-K Dielectric for Increased Capacitance Density and Related Structure	11/121,360	5/3/2005	Pending
Selective and Non-Selective Epitaxy for Base Integration in a BiCMOS process and related structure	11/146,537	6/6/2005	Pending
Method For Fabricating A Backside Through-Wafer Via In A Processed Wafer And Related Structure	60/848,973	10/2/2006	Pending
Method For Fabricating A Frontside Through-Wafer Via In A Processed Wafer And Related Structure	11/641,500	12/18/2006	Pending
Structure and Method for Encapsulating Microelectronic Devices	11/542,088	10/2/2006	Pending
Method For Fabricating A Substrate-Insulated Frontside Through-Wafer Via In A Processed Wafer And Related Structures	11/641,296	12/18/2006	Pending
Frontside Through-Wafer Vias For Semiconductor Device Region Isolation	11/641,504	12/18/2006	Pending
Method For Preventing Backside Metallization Separation In A Semiconductor Die And Related Structure	11/641,376	12/18/2006	Pending
Method For Fabricating A Top Conductive Layer In A Semiconductor Die And Related Structure	11/641,925	12/18/2006	Pending
Metal Resistor	60/276,277	3/15/2001	Pending
Composite Series Resistor Having Reduced Temperature Sensitivity in an IC Chip	10/843,190 7,078,786		7/18/2006
CMOS Transistor Spacers Formed in a BiCMOS Process	10/936,927 6,992,338		1/31/2006
NPN Transistor Having Reduced Extrinsic Base Resistance and Improved Manufacturability	10/865,634 7,064,361		6/20/2006
An Efficiently Fabricated Bipolar Transistor	10/313,583 6,972,442		12/6/2005
Method for Fabricating a Self-Aligned Bipolar Transistor	10/870,900 7,041,564		5/9/2006
Process for and structure of high density VLSI circuits, having self-aligned gates and contacts for FET devices and conducting lines	06/397,052 4,506,437		3/26/1985
Process for and structure of high density VLSI circuits, having self-aligned gates and contacts for FET devices and conducting lines	06/397,050 4,477,962		7/17/1984

<b>Title</b>	<b>Patent No.</b>	<b>Filing Date</b>	<b>Issue Date</b>
High rate resist polymerization apparatus	06/397,646 4,459,937		7/17/1984
Ion etching process with minimized redeposition	06/355,445 4,396,479		8/2/1983
Method for making a reliable ohmic contact between two layers of integrated circuit metallizations	06/531,529 4,507,852		4/2/1985
Dimension monitoring technique for semiconductor fabrication	484,666 4,639,142		1/27/1987
Method of Fabricating an Interconnect Structure Employing Air Gaps Between Metal Lines and Between Metal Layers	09/686,323 7,056,822		6/6/2006
Damascene Interconnect Structure and Fabrication Method Having Air Gaps Between Metal Lines and Metal Layers	09/665,422 6,984,577		1/10/2006
Double Implant High Performance Varactor and Method for Manufacturing Same	09/590,462 6,995,068		2/7/2006
NPN Transistor Having Reduced Extrinsic Base Resistance and Improved Manufacturability	11/003,572	12/2/2004	Pending
Method for Selective Fabrication of High Capacitance Density Areas in a Low Dielectric Constant Material and related Structure	09/575,055 7,049,246		5/23/2006
Selective Fabrication of High Capacitance Density Areas in a Low Dielectric Constant Material	10/995,762 7,109,125		9/19/2006
Method for Controlling an Emitter Window Opening in an HBT and Related Structure	6,586,307		7/1/2003
Damascene Trench Capacitor for Mixed-Signal/RF IC Applications	6,838,352		1/4/2005
Fabrication of High-Density Capacitors for Mixed Signal/RF Circuits	10/190,297 7,060,557		6/13/2006