PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	OPTION

CONVEYING PARTY DATA

Name	Execution Date
Alliance Semiconductor Corporation	04/30/2007

RECEIVING PARTY DATA

Name:	Acacia Patent Acquisition Corporation
Street Address:	500 Newport Center Dr., 7th Floor
City:	Newport Beach
State/Country:	CALIFORNIA
Postal Code:	92660

PROPERTY NUMBERS Total: 36

Property Type	Number
Patent Number:	5416738
Patent Number:	5518942
Patent Number:	5557122
Patent Number:	5598095
Patent Number:	5598526
Patent Number:	5617555
Patent Number:	5633832
Patent Number:	5638090
Patent Number:	5671188
Patent Number:	5672535
Patent Number:	5712664
Patent Number:	5777631
Patent Number:	5781497
Patent Number:	5825681
Patent Number:	5856944

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Patent Number:	5860076
Patent Number:	5892516
Patent Number:	5929872
Patent Number:	5940067
Patent Number:	6016270
Patent Number:	6020237
Patent Number:	6043804
Patent Number:	6081279
Patent Number:	6166409
Patent Number:	6175520
Patent Number:	6236608
Patent Number:	6258714
Patent Number:	6301629
Patent Number:	6303959
Patent Number:	6317135
Patent Number:	6392267
Patent Number:	6429076
Patent Number:	6456537
Patent Number:	6476666
Patent Number:	6903434
Patent Number:	6921688

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	AL (070430)
NAME OF SUBMITTER:	Marc J. Frechette

Total Attachments: 7

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Agreement executed April 30, 2007

between

Assignor and APAC

AGREEMENT

This agreement ("Agreement") is entered into by and between ALLIANCE SEMICONDUCTOR CORPORATION ("Assignor"), a Delaware corporation having its principal place of business at 2900 Lakeside Dr., Suite #229, Santa Clara, CA 95054, and ACACIA PATENT ACQUISITION CORPORATION ("APAC"), a Delaware corporation having a principal place of business at 500 Newport Center Drive, Suite 700, Newport Beach, CA 92660 (collectively referred to herein as the "Parties"). The effective date of this Agreement shall be the date on which the last Party executes this Agreement below (the "Effective Date").

BACKGROUND

Whereas, Assignor is the sole and exclusive owner of the patents and patent applications set forth on Schedule 1 attached hereto and, except for the excluded patent set forth on Schedule 3 (the "Excluded Patent"), all corresponding foreign patents and foreign patent applications, and all continuations, continuations in part, divisions, extensions, renewals, reissues and re-examinations of the patent and patent applications set forth on Schedule 1, which are collectively referred to as the "Assigned Patents" (the "Assigned Patents");

Whereas, Assignor desires to sell to APAC all of Assignor's right, title and interest in and to the Assigned Patents and APAC in turn, desires to acquire all of the rights, titles and interests in and to the Assigned Patents,

NOW, THEREFORE, in consideration of the promises and mutual covenants contained herein and for other good and valuable consideration, Assignor and APAC agree as follows:

1. ASSIGNMENT

1.1. Effective upon the date of Satisfactory Completion as set forth in Section 2.2 below, (i) Assignor assigns, conveys, transfers and sells to APAC the entire right, title, and interest in and to the Assigned Patents, including without limitation, all rights of Assignor to sue for past, present and future infringement of the Assigned Patents, including the right to collect and receive any damages, royalties, or settlements for such infringements, all rights to sue for injunctive or other equitable relief, and any and all causes of action relating to any of the inventions or discoveries claimed in the Patents; and (ii) Assignor assigns to APAC, subject to consent by Duke University, all of its rights under the License Agreement dated October 30, 1997 by and between Duke University and Assignor (the "Duke License"), pursuant to which Assignor received an exclusive license to the patent identified on Schedule 3 (the "Licensed Patent"). The Assigned Patents and the Licensed Patent are referred to collectively as the "Patents". Assignor shall execute and deliver to APAC a separate Assignment, which is attached hereto as Exhibit A, and such other documents as APAC shall reasonably require to effectuate the transactions contemplated by this Agreement.

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the Agreement between Assignor and APAC

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construed as if such invalid, illegal or unenforceable provision had never been contained therein.

7.7 This Agreement was negotiated between the Parties, and neither Party "prepared" this Agreement for purposes of California Civil Code §1654. Any ambiguity will not be construed against the drafter, but rather the terms and provisions of this Agreement will be given a reasonable interpretation.

7.8. This Agreement may be executed in several counterparts, each of which shall constitute an original, but all of which together shall constitute one and the same instrument. A faxed copy of a signature page shall be considered an original for purposes of this Agreement.

7.9 The headings contained in this Agreement have been inserted for convenient reference only and shall not modify, define, expand or limit any of the provisions of this Agreement.

IN WITNESS WHEREOF, the Parties have executed this Agreement on the Effective Date.

ALLIANCE SEMICONDUCTOR CORPORATION	ACACIA PATENT ACQUISITION CORPORATION
By: [signature]	By:
Print Name: Kenneth Wheeler Jr.	Print Name:
Title: Interim Chief Financial Officer	Title:
Date: 4/30/07	Date:

Schedule 1

Assigned Patents

Docket	Patent No.	Issue Date	Title	Product Group
6014	5,416,738	05/16/95	SINGLE TRANSISTOR FLASH EPROM CELL AND METHOD OF OPERATION	memory/flash
500	5,518,942	05/21/96	METHOD OF MAKING FLASH EPROM CELL HAVING IMPROVED ERASE CHALSCACTERISTICS BY USING A TILT ANGLE IMPLANT	memory/flash
800	5,557,122	09/17/96	SEMICONDUCTOR ELECTRODE HAVING IMPROVED GRAIN STRUCTURE AND OXIDE GROWTH PROPERTIES	memory/flash
200	5,598,095	01/28/97	SWITCHABLE CURRENT SOURCE FOR DIGITAL TO ANALOG CONVERTER (DAC)	graphics
6010	5,598,526	01/28/97	METHOD AND SYSTEM FOR DISPLAYING IMAGES USING A DYNAMICALLY RECONFIGURABLE DISPLAY MEMORY ARCHITECTURE	graphics
1500	5,617,555	04/01/97	BURST RANDOM ACCESS MEMORY EMPLOYING SEQUENCED BANKS OF LOCAL TRI-STATE DRIVERS	memory/DRAM
2300	5,623,832	05/27/97	REDUCED AREA WORD LINE DRIVING CIRCUIT FOR RANDOM ACCESS MEMORY	memory/DRAM
6002	5,638,096	06/10/97	WINDOW DEPENDENT BRIGHTNESS CONTROL FOR VIDEO DACs	graphics
6000	5,671,188	09/23/97	RANDOM ACCESS MEMORY HAVING SELECTIVE INTRA-BANK FAST ACTIVATION OF SENSE AMPLIFIERS	memory/DRAM
6004	5,672,535	09/30/97	METHOD OF FABRICATING DRAM CELL WITH SELF ALIGNED CONTACT	memory/DRAM
6401	5,712,664	01/27/98	SHARED MEMORY GRAPHICS ACCELERATOR SYSTEM	graphics
2210	5,777,631	07/07/98	METHOD AND APPARATUS FOR DISPLAYING A VIDEO WINDOW IN A COMPUTER GRAPHICS DISPLAY	graphics
6500	5,781,497	07/14/98	RANDOM ACCESS MEMORY WORD LINE SELECT CIRCUIT HAVING RAPID DYNAMIC DESELECT	memory/DRAM
3100	5,825,681	10/20/98	DIVIDER MULTIPLIER CIRCUIT HAVING HIGH PRECISION MODE	graphics
3600	5,856,944	01/05/99	SELF-CONVERGING OVER-ERASE REPAIR METHOD FOR FLASH EPROM	memory/flash
3900	5,870,076	01/12/99	48-BIT WIDE MEMORY ARCHITECTURE ADDRESSING SCHEME RECONFIGURABLE FOR 8-BIT, 16-BIT AND 32 BIT DATA ACCESSES	graphics
3500	5,892,516	04/06/99	PERSPECTIVE TEXTURE MAPPING CIRCUIT HAVING PIXEL COLOR INTERPOLATION MODE AND METHOD THEREOF	graphics
3700	5,929,872	07/27/99	METHOD AND APPARATUS FOR MULTIPLE COMPOSITING OF SOURCE DATA IN A GRAPHICS DISPLAY PROCESSOR	graphics
3600	5,949,867	08/17/99	REDUCED MEMORY COMPUTER GRAPHICS SYSTEM FOR RENDERED IMAGES	graphics

Docket	Patent No.	Issue Date	Title	Product Group
6908	6,016,270	01/18/00	FLASH MEMORY ARCHITECTURE THAT UTILIZES A TIME-SHARED ADDRESS BUS SCHEME AND SEPARATE MEMORY CELL ACCESS PATHS FOR SIMULTANEOUS READ/WRITE OPERATIONS	memory/flash
5400	6,026,237	02/01/00	METHOD OF REDUCING DIELECTRIC DAMAGE DUE TO CHARGING IN THE FABRICATION OF STACKED GATE STRUCTURES	memory/flash
3669	6,041,201	03/28/00	COLOR PIXEL FORMAT CONVERSION INCORPORATING COLOR LOOK-UP TABLE & POST LOOK-UP ARITHMETIC	graphics
6670	6,081,279	06/27/00	SHARED MEMORY GRAPHICS ACCELERATOR SYSTEM	graphics
4658	6,166,909	12/26/00	FLASH EPROM MEMORY CELL HAVING INCREASED CAPACITIVE COUPLING AND METHOD OF MANUFACTURE THEREOF	memory/flash
5303	6,175,510	01/16/01	NONVOLATILE MEMORY ARRAY HAVING LOCAL PROGRAM LOAD LINE REPEATERS	memory/flash
6074	6,236,608	05/22/01	TECHNIQUE TO IMPROVE THE SOURCE LEAKAGE OF FLASH EPROM CELLS DURING SOURCE ERASE	memory/flash
6072	6,258,714	07/10/01	MAKING SELF-ALIGNED CONTACT FOR SALICIDED MOS DEVICES	memory/flash
6034	6,301,629	10/09/01	HIGH SPEED/LOW SPEED INTERFACE WITH PREDICTION CACHE	graphics
6073	6,303,959	10/16/01	PROCESS TECHNIQUE TO IMPROVE THE SOURCE LEAKAGE OF FLASH EPROM CELLS DURING SOURCE ERASE	memory/flash
6078D2	6,317,136	11/13/01	DISTRIBUTED MEMORY GRAPHICS ACCELERATOR SYSTEM	graphics
5506	6,392,267	05/21/02	FLASH EPROM ARRAY WITH SELF-ALIGNED SOURCE CONTACTS AND PROGRAMMABLE SECTOR ERASE ARCHITECTURE	memory/flash
4660D	6,429,570	08/06/02	FLASH EPROM MEMORY CELL HAVING INCREASED CAPACITIVE COUPLING AND METHOD OF MANUFACTURE THEREOF	memory/flash
6075	6,456,537	09/24/02	NEW EPROM CELL STRUCTURE WITH DRAIN SIDE PROGRAMMING AND ERASE	memory/flash
6087	6,476,686	11/05/02	BOOTSTRAPPED CHARGE PUMP	memory/DRAM
6070	6,903,434	06/07/05	A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE	memory/flash
6070D1	6,921,688	07/26/05	A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE	memory/flash

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