PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Integrated Device Technology Inc.	09/20/1999

RECEIVING PARTY DATA

Name:	IP-First, LLC
Street Address:	1045 Mission Court
City:	Fremont
State/Country:	CALIFORNIA
Postal Code:	94539

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	5619667

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CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Taysie J. Locke

Total Attachments: 5
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INTELLECTUAL PROPERTY ASSIGNMENT

WHEREAS, Integrated Device Technology, Inc., a Delaware corporation, having a principal place of business at 2975 Stender Way, Santa Clara, California 95054 (hereinafter referred to as "Assignor") owns the patents, listed on Exhibit A hereto (the "Patents"),and the patent applications, listed on Exhibit B hereto (the "Patent Applications") (collectively referred to as "Intellectual Property");

WHEREAS, IP-First, LLC, a Delaware limited liability company (hereinafter referred to as Assignee) desires to acquire all right, title and interest in and to the Intellectual Property;

WHEREAS, Assignor, assigns the Intellectual Property (and all applications for registration thereof) to Assignee ~~subject to a license back to Assignor~~. BCB

NOW, THEREFORE, Assignor does hereby assign to Assignee, all right, title and interest in and to the Intellectual Property together with any foreign equivalents that exist, and Letters Patent to be obtained for the Patent Applications of Exhibit B or any continuation, division, renewal, or substitute thereof, and as to Patents any reissue or re-examination thereof in exchange for good and valuable consideration.

Executed at Santa Clara, California, this 20th day of September, 1999.

INTEGRATED DEVICE TECHNOLOGY, INC. (Assignor)

By: B C Bousseire
Name: B. C. Bousseire
Title: Vice President & Treasurer

IP-FIRST, LLC (Assignee)
By: Integrated Device Tech., Inc. as Managing Member
Name: B. C. Bousseire ; B C Bousseire
Title: Vice President & Treasurer, IDT

Exhibit A: Patents

Title	Patent Number	Patent Issue Date
Test Ring Oscillator	5911083	9/22/98
Apparatus and Method for Exception Handling During Microcode String Instructions	5784607	7/21/98
Cache Array Select Logic Allowing Cache Array Size To Differ From Physical Page Size	5809562	9/15/98
Configurable Drive Clock	5802356	9/1/98
Method and Apparatus for Locating Exception Correction Routines	5787241	7/28/98
Apparatus for Fast Forwarding of TI Bit During Descriptor Load	5864877	1/26/99
Method and Apparatus for Selector Storing and Restoration	5787495	7/28/98
Method and Apparatus for On the Fly Descriptor Validation	5815729	9/28/98
Method for Fast Validation Checking for Code and Data Segment Descriptor Loads	5822607	10/13/98
Method and Apparatus for Repetitive Execution of String Instructions Without Branch or Loop Microinstructions	5752015	5/12/98
Method and Apparatus for Sub Cache Line Access and Storage	5781926	7/14/98
Method And Apparatus For Sub Cache Line Access And Storage...	5835929	11/10/98
Apparatus And Method For Direct Loading Of Offset Register During Pointer Load Operation	5951676	9/14/99
Method and Apparatus for Register Address Fill-In of Register Generic Microcode Instructions	5717910	2/10/98
Method and Apparatus for Fast Fill of Translator Instruction Queue	5819057	4/8/97
Apparatus and Method for Register Address Indirection in the Instruction Queue	5864690	1/26/99
Apparatus And Method For Managing Interrupt Delay Associated With Mask Flag Transition	5864701	1/26/99
Apparatus and Method for Managing Interrupt Delay on Floating Point Error	5887175	3/23/99
Apparatus and Method for Tracking of Register Changes During Execution of a Micro Instruction Sequence	5812813	9/22/98
Apparatus and Method for Processing Exceptions During Execution of String Instructions	5774711	6/30/98
Fuse Array Control for Smart Function Enable	5889679	3/30/99
Method and Apparatus For Shared Cache Lines in Split Data/Code Caches	5930821	7/27/99
Method And Apparatus For Optimizing Dependent Operand Flow Within A Multiplier Using Recoding Logic	5892699	4/6/99
Method And Apparatus For Wafer Test Of Redundant Circuitry	5835431	11/10/98

Exhibit B: Patent Applications

Title	Serial	Filing Date
Method For Improving Updating Of Descriptor Access Bit	08/748575	11/13/96
Combining ALU And Memory Storage Micro Instructions By Using An Address Latch To Maintain An Address	08/820576	3/19/97
Apparatus For Fast Fill Of Translator Instruction Queue	08/826729	4/7/97
Method And Apparatus For Improved Exchange Instruction	08/854614	5/12/97
Method And Apparatus For Smart Bus Lock Utilizing An On-Chip Cache For Performing A Locked Read-Modify-	08/855801	5/12/97
Apparatus And Method For Tracking Changes In Stack Address Size During Stack Segment Register Load To	08/871040	6/9/97
Selectively Enabled/Disabled On-Chip Pull-up Circuit	08/931860	9/16/97
Method And Apparatus For Returning An Alternate Vendor ID From A Microprocessor	08/958641	10/14/97
Method And Apparatus For Branch Address Calculation During Decode	08/962344	10/31/97
Equal Propagation Logic Gates	08/967696	11/12/97
Instruction Set For BiDirectional Conversion And Transfer Of Integer And Floating Point Data	08/980481	11/29/97
Method And Apparatus For Emulation Of Microprocessor ROM	08/980480	11/29/97
Method And Apparatus For Improved Accessing Of Aggregate Data	08/008927	1/20/98
Apparatus And Method For Recording A Floating Point Error Pointer In Zero Cycles	09/019452	2/5/98
Method And Apparatus For Improved Aligned/Misaligned Data Load From Cache	09/020269	2/6/98
Method And Apparatus For Improved Exchange Instruction For Register Operand Swaps	09/019833	2/6/98
Method And Apparatus For Floating Point Tag Register Save	09/030680	2/25/98
Apparatus And Method For Single Instruction Record Floating Point	09/033399	3/2/98
Method For Transferring Burst Data In A Microprocessor	09/034556	3/3/98
Mechanism For Floating Point To Integer Conversion With RGB BIAS Multiply	09/048712	3/26/98
Method And Apparatus For Improved Floating Point Exchange	09/048524	3/26/98
Apparatus For Improved Cache Hit Determination	09/049679	3/27/98

Apparatus And Method For Branch Target Address Calculation During Instruction Decode	09/052624	3/31/98
Method And Apparatus For Absolute Floating Point Register Addressing	09/063282	4/20/98
Method For Improved Bit Scan	09/092386	6/5/98
Apparatus And Method For Integer Divide	09/108,845	7/1/98
Method And Apparatus For Single Precision Multiply	09/116189	7/15/98
Method And Apparatus For Fast Square Root Calculation Within A Microprocessor	09/118518	7/17/98
Method And Apparatus For Double Operand Load	09/130910	8/7/98
Slew-Controlled Split Voltage Output Driver	09/150316	9/9/98
Apparatus And Method For Double Push/Pop Operation	09/151006	9/10/98
Method And Apparatus For Passing Jump Addresses	09/167426	10/6/98
Double Pushall And Popall Apparatus Within A Single Pipeline Microprocessor	09/193278	11/17/98
Method And Apparatus For Providing Software Readable CPU Identification	09/193286	11/17/98
Microprocessor Having Fuse Control And Selection Of Clock Multiplier	09/193303	11/17/98
Method And Apparatus For Performing Branch Prediction Combining Static And Dynamic Branch	09/203884	12/2/98
Static Branch Prediction Mechanism Utilizing Opcode and Displacement	09/203900	12/2/98
Method And Apparatus For Speculatively Updating Global Branch History	09/203844	12/2/98
Apparatus And Method For Fast Forward Branch	09/272226	3/18/99
Method and Apparatus For Correcting An Internal Call/Return Stack In A Microprocessor That	09/271591	3/18/99
Static Branch Prediction Mechanism For Conditional Branch Instructions	09/272225	3/18/99
Combining ALU And Memory Storage Micro Instructions By Using An Address Latch To Maintain An Address	08/820576	4/21/99
Tester Management Of Microcode BIST Memory Test	09/299673	4/26/99
Result Forwarding Cache	09/314176	5/18/99
Pairing Of Load-ALU-Store With Conditional Branch	09/313908	5/18/99
Pairing of Micro Instructions in the Instruction Queue	09/313907	5/18/99

Status Register Associated With MMX Register File For Tracking Writes	09/344439	6/25/99
Method And Apparatus For Tracking Coherency Of Dual Floating Point And MMX Register Files	09/349441	7/9/99
Multiplier For Fast Multiply Accumulate Instruction	09/349440	7/9/99
Fuse Array For Serializing A Microprocessor Die	09/349445	7/9/99
Method And Apparatus For Selective Writing Of Incoherent Registers In Dual FP/MMX Register Files	09/357419	7/20/99
Exception Handler Method And Apparatus For Paired MMX Instructions	09/357703	7/20/99