PATENT ASSIGNMENT

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NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
HG INVESTMENT MANAGERS LIMITED	12/26/2006

RECEIVING PARTY DATA

Name:	PATENTICA IP LTD
Street Address:	111 Piccadilly, Suite 315
City:	Manchester
State/Country:	UNITED KINGDOM
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PROPERTY NUMBERS Total: 2

Property Type	Number
Application Number:	10814576
Application Number:	10090815

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Total Attachments: 15
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ASSIGNMENT

DATED 26 December 2006

BETWEEN

(1) **HG INVESTMENT MANAGERS LIMITED**, a Company organized and existing under the laws of *the United Kingdom, of Minerva House, Third Floor, 3-5 Montague Close, London SE1 9BB, UK* (the "**Assignor**");

(2) **PATENTICA IP LTD**, a Company organized and existing under the laws of *the United Kingdom, of 111 Piccadilly, Suite 315, Manchester, M1 2HX, UK* (the "**Assignee**")

WHEREAS

(1) The Assignor is the Registered Proprietor and beneficial owner of a series of Patent, Utility Model, Design and Trade Mark Applications, Patents and Trade Mark registrations listed hereinafter as set out in the accompanying Schedule of Intellectual Property (the "IP");

(2) The Assignor has agreed to **ASSIGN** to the Assignee for the consideration and upon the terms hereinafter mentioned all its right, title and interest in the said Intellectual Property ("IP").

NOW THIS DEED WITNESSETH as follows:

IN PURSUANCE of this Agreement and in consideration of the sum of £1 (One Pound) now paid by the Assignee to the Assignor (the receipt whereof the Assignor hereby acknowledges):

(1) The Assignor hereby **ASSIGNS** to the Assignee all its right title and interest in the said IP and all the rights powers and liberties and immunities conferred on the proprietor by the grant thereof including the right to sue for damages and other remedies in respect of any infringements of such rights or other acts within the scope of claims of any published specification of the IP or accompanying any applications therefore prior to the date hereof **TO HOLD** the same unto Assignee absolutely. No warranties are given or intended by the Assignor in respect of the IP.

(2) The Assignor hereby agrees that he will at the expense of the Assignee execute and sign all such documents or do any such acts as may be reasonable necessary to record the transfer of ownership of the IP hereunder.

(3) This Assignment shall be governed and construed in accordance with the law of Guernsey.

IN WITNESS WHEREOF the parties have executed this Assignment the day and year first mentioned.

EXECUTED for an on behalf of the Assignor)
)
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By: M.C.J. HUMPHRIES
Position DIRECTOR

EXECUTED for an on behalf of the Assignee in accordance with its Constitutions)
)
)

By: R.M.C.M. MARY
Position DIRECTOR

Schedule of Intellectual Property

Our Ref.	Application Number	Title	Abstract	Filing Date (Priority date)	Status	Applicant and Inventor(s)
1	UK 9623215.2	Solid State Memory Test System with Defect Compression	A high speed data transfer system by compressing test results while providing for subsequent regeneration. The system comprises: a) address receiving means for receiving addresses corresponding to the locations of said defective memory cells, b) a compression means coupled to the address receiving means, whereby after receipt of the addresses the compression means creates a representation of the received data, the representation being a compressed form of the original data allowing the lossless reconstruction of the original data or a restoration of the original data with losses in the form of additional defects which may be created during the restoration process.	07.11.96	Priority claimed	Process Insight Ltd. A. DEAS
100	PCT/GB97 /03007 WO98/20497 Publ.14.05.98			07.11.97 (07.11.96)	National Entries	Process Insight Ltd Inv.: A.Deas
102	US 09/101332 US PATENT 6,269,455	System and Method For Processing Information About Locations of Defective Memory Cells and Memory Test Apparatus		Nat. Entry 07.07.98 (07.11.96)	GRANTED 31.07.2001 4th year paid Renewal by 31 Jul 2008	ACUID CORP.Ltd; Inv.: A. Deas
103	Canada CA2,270,917	Solid State Memory Test System with Defect Compression		Nat. Entry 05.05.99 (07.11.96)	Exam requested 07.11.2002	Process Insight Inv.: A. Deas
104	Japan 10-521136 (translated)			Nat. Entry 07.05.99 (07.11.96)	Exam requested 07.11.2004	Process Insight Inv.: A.Deas
101	EP 1012848 Publ 28.06.00 97911326.3 (UK, DE) DE69713911 GB1012848			Nat. Entry 07.06.99 (07.11.96)	GRANTED, IN FORCE Renewal by 30.11.06	ACUID CORP (Guernsey) ltd Inv.: A.Deas
3.	UK 9714130.3	In situ Memory Characterisation Tool	A characterisation means coupled between a computer system under test and a memory that constitutes the device under test. By generating trigger signals for use by a measurement system, e.g. a logic analyser or an ATE, events around the data strobe time of the computer system can be characterised, for example, the address access time or output enable access time can be measured. In a preferred embodiment a read access control signal is detected by the characterisation means, and the data output of the device under test is compared with the data output of a reference memory after a variable delayed period of time, whereupon a trigger signal is generated when the data does not match.	05.07.97	Priority claimed	Appl/Inv.: Dr. Alex DEAS
301	PCT/GB98/01981 WO98/01871 Publ. 06.07.1998	Memory Characterisation Means and Method		06.07.98 (05.07.97)	Nat. Entries	The Acumen Trust Inv.: Dr. DEAS
302	US 09/477726			05.01.00 (05.07.97)	ABANDONED	Process Intelligence Ltd, (Assignment registered 13.03.2000) Inv. Deas
4.	UK 9716812.4	Memory Test Equipment with Optimisation Function	Automatic test equipment for memory devices with means to optimise features of the test according to the test results generated by the equipment at an individual defect level. The memory test system comprises: a means for executing each test in a sequence of test patterns, a means for obtaining fault bit maps for each test, a means for accumulating the bitmap fail data during the test; a means for correlating each bit map using analysis hardware or software to determine the performance data and a means for automatically modifying the test sequence in response to the performance data to maximise the performance of the test.	09.08.97	Priority claimed	Process Int. Ltd Inv.: Dr. Alex DEAS
400	PCT/RU98/00261 WO 99/08116 Publ. 18.02.1999			10.08.98 (09.08.97)	Nat. Entries	Appl./Inv.: MUSTAFINA, Inv. A DEAS
401	EP 98950530.0 (amended) publ. EP(GB) 1040358 DE19986025078	Test Sequence Optimisation Means and Method		Nat. Entry 09.03.00 (10.08.97)	Granted 10 August 2005 8th year renewal WAS NOT PAID	ACUID CORP. (Guernsey) Limited Inv.: DEAS MUSTAFINA

402	US 09/369,859 (amended)			09.08.99	Abandoned	Process Intell.Ltd Inv.: DEAS MUSTAFINA
404	JP2000-506533 (translated, amended)			10.08.97 (Nat. Entry 09.02.00)	Abandoned	Process Intell. Ltd Inv.: DEAS MUSTAFINA
5.	GB 9724529.4	Memory Redundancy Allocation System and Method of Redundancy Allocation	A means for providing a minimum repair solution in a memory redundancy allocation system by finding an optimal solution assuming the availability of unlimited spare resources and then, under the same conditions, adapting the optimal solution obtained to an existing ratio of spare resources. The system reduces the required amount of redundancy and number of waste repairs and enhances device reliability, thus improving overall yield and the profitability of a memory manufacturer.	21.11.97	Priority claimed	Process Intell.Ltd Inv.: ELKHIMOVA Alex DEAS
500	PCT/RU98/ 00392 WO 99/27431 publ. 03.06.99			PCT filing 23.11.98 (21.11.97)	IPER done National Entries by 23.05.2000	Appl/Inv.: Elkhimova Inventor: DEAS Process Intell. Ltd.
501	EP 98962798 EP(GB)1032870 DE69822658			EP Entry date 21.06.000	Granted IN FORCE Renewal by 23.11.06	ACUID CORP. (Guernsey) Limited Appl.Deas Inv.Deas, Elkhimova
502	US 09/453,843			US filed 02.12.99	Abandoned	Appl/Inv: Deas, Elkhimova Pr. Int. Ltd
503	CA 2,310,771			23.05.00	Abandoned	Elkhimova Deas
504	JP 2000-522506			22.05.00 (21.11.98)	Abandoned	Process Int.
6.	GB 9725066.6	Address Transformation Means	A transformation means for transforming memory cell addresses between different memory device topologies, wherein the transformation means is capable of a configurable mapping represented as an affine transformation in Pn space, where n denotes the total number of bits in an address, and P is the modulo 2 field. The transformation means provides the minimum memory space and time required for storage and computing defect data and also the flexibility of approach which allows the use of a wide spectrum of mapping classes and simplifies the transformation procedure.	PCT filed 30.11.98 (28.11.97)	National Entries by 28.05.2000	Process Intell. Ltd Inv.: VILKOV A DEAS
14. 1400	PCT/RU98/00403 WO 99/37083 Publ. 22.07.1999	Affine Transformation Means and Method of Affine Transformation	Means to create affine transformations and very fast method of implementation: orders of magnitude faster than any other mapping means known currently. Other advantages are that the proposed transformation procedure does not require checking for being non-contradictory, and also it is much more simple due to decreasing the number of operations used for transformation. To further speed up the procedure, pre-calculated partial results may be stored and used.	PCT filing Date 30.11.98 (28.11.97)	PCT filing	Appl/Inv.: VILKOV Inventors: Deas, Pliss Abrosimo
1401	EP 98967039.3 06.09.00 EP(GB)1033029 DE6980650			Filed by 28.06.00	GRANTED 10.07.02 IN FORCE Renewal by 30.11.06	ACUID UK Ltd. Inv.: Deas Vilkov Pliss Abrosimo
1402	US 09/450,693			US filed 30.11.99	Abandoned	Process Int. Ltd
1403	CA 2,312,126			Filed 28.05.00	Examination requested by 30.11.2003	Process Int.
1404	JP 11-341420 Publ. on			30.11.98 (Nat. Ent.	Examination to be requested by 30.11.2005	Process Int. Ltd

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	22.08.00 P2000- 231511A					
7	UK 9800957.4	Test Probe Interface Unit and Method of Manufacturing	Very high speed test probe interface, capable of speeds of hundreds of GHz. Consists of a wafer with probe points formed on the wafer. Microphotographs and other details from actual construction of the probe interface included.	17.01.98		Process Intell.Ltd Inv.: Davydov; A. DEAS
701	PCT/RU99/00014 WO 99/36790 Publ. 22.07.1999			PCT filing 18.01.99 (17.01.98)	National Entries	Process Intell.Ltd Inv.: V. Davidov A. Deas
702	US 6,566,245 10/090,828 Publ. 2002-0102746			06.03 2002 claiming priority of 11.01.00	GRANTED IN FORCE US 6,566,245 20.05.2003 Renewal 20.11.06	ACUID CORP (GUERNSEY) Ltd App/Inv.: Deas Davydov
707	RU2000122456			17.08.00	Examination requested 18.01.2002	Davidov
8	UK 9805054.5	Memory Test System with Buffer Memory	Data communications channel for semiconductor device testing providing continuous high-speed testing by intelligent pausing a timing means when a buffer memory is full or nearly full. When paused, the timing means is capable of maintaining properly refresh and clock functions for semiconductor devices. The memory test system comprises a central control unit, a timing means, a fault logic means for detecting failures in the memory elements, and a fault capture memory for storing fault information obtained at testing comprising a high speed buffer memory and a low speed main memory.	11.03.98	Priority claimed	Process Intell.Ltd Inv.:Dr. Alex DEAS
801	PCT/RU99/00068 WO 99/46778 Publ. 16.09.1999	High Speed Memory Test System with Intermediate Storage Buffer and Method of Testing		PCT filing 11.03.99 (11.03.98	National Entries by 11.09.2000	Vadim Demidov Inv.:Dr. Alex Deas; Demidov
802	US 6,460,152 (appl. Ser. 09/659,659)			Issue date 01.10.02	GRANTED Abandoned for non payment of renewal fee Renewal By 01.10.06	Acuid Corp. (Guernsey) Ltd Inv.: Deas, Demidov,
803	CA 2,347,549				Filed 11.09.2000	Demidov, Deas
804	JP 2000-536078 JP12-536078				Filed 08.09.2000	Demidov, Deas Assignee: Acuid
805	EP 1,080,471 Appl. No. 99926999.6 DE69903155				GRANTED 12.02.02 Abandoned for non payment of renewal fee 11.09.2006 8th renewal + extra	ACUID CORP. (Guernsey) Limited Inv. Alex Deas,
9. 901	PCT/RU98/00139 WO 99/57661 Publ.11.11.99	A System for Modelling Memory Business Parameters	A system for modelling memory business parameters provides the key competitive advantages for companies in the memory industry by optimising each step in the product flow to achieve the maximum number of products shipped at the lowest cost and with the optimum level of application compatibility. The system creates a model using various business parameters, such as memory design, processing costs, production capacity and characteristics, technology limits, user demand, and end application	PCT filing 06.05.98	National Entries	Appl./Inv.: KURSOV Inventor: Alex DEAS
902	US 09/304,823			US filed 05.05.99	Pending	Kursov, Deas Assignee: Proces Intell.
903	CA			Filed 06.11.00	Examination requested	Kursov, Deas

			compatibility. Using this model, the system then estimates the profitability		06.05.2003	
900	UK 0029708.5 GB2000 0029708		of a memory industry plant in terms of finished good devices as a function of the cost of sales, based on possible variations of business parameters and predicts the savings that may be obtained if business parameters are optimised.	Filed 05.12.00	GRANTED 14.05.2003 Abandoned for non payment of renewal fee	Acuid Corp (Guernsey Ltd Inv. Deas, Kursov)
10.	PCT/RU98/00204 WO00/00836 Publ. 06.01.2000	Skew Calibration Means and Method	A means for providing a high accuracy of transferring and receiving signals by intelligent skew calibration of a timing system.	PCT Filing 29.06.98	National Entries 29.12.2000	Appl/Inv. Klotchkov
1001	PCT/RU99/00194 WO00/00837 Publ. 06.01.2000		The means for automatic skew calibration of a transceiver comprises a plurality of input registers for transmitting signals; a plurality of output registers for receiving signals; a main clock driver for generating a main	PCT filing 10.06.99 (29.06.98)	Entry in EPO 29.01. 2000	Klotchkov
1002	US 09/342,227 US 6,298,465		clock signal; a reference clock driver for generating reference signals for calibrating the registers; the said reference clock driver being associated with the said main clock driver; and a plurality of phase shift means comprising at least one set of phase shift means associated with each said plurality of registers, for the relative alignment of the register's timing within each plurality.	29.06.99 (29.06.98)	Granted 30.01.2001 Abandoned, can be restored by 2 October 2007 450$ (renewal) + 1640$ restoration)	Acuid Corp. Guernsey. Ltd Klotchkov
1006	Taiwan 88110660 GRANTED TW1139357		The calibration is performed using a common time base which is distributed by means of a transmission line having predetermined wave characteristics.	24.06.99	GRANTED Renewal fees By 31.08.04	Acuid Corp. Guernsey) LTD. /Klotchkov
1003	Canada 2,346,883			29.12.00 (29.06.98)	Filed 04.11.2000	Klotchkov
1004	JP 2000-557157 JP12-557157				Request for Exam filed 12.06.06 but not paid yet	ACUID Corp., Klotchkov
1001 EP	EP 99933307.3 EP(GB)1131645 DE69905750				GRANTED IN FORCE Renewal by 10.06.2007	Acuid Corp. Guernsey Ltd. Inv. Klotchkov
1008	Singapore 200105639-9			Filed 29.07.01 (late entry)	GRANTED Grant fee paid 16.03.03	Acuid Corp. (Guernsey)
1002-2	US 09/967,535 US 6,820,234			Filed on 01.10.01	Granted 16.11.04 Renewal 02.10.07	ACUID Corp Limited UK
11. 1101	PCT/RU98/00275 WO 00/11554 Publ. 02.03.2000	A System for Identification of Transformation of Memory Device Addresses	A system for defining transforms of cell addresses between different device topologies providing the use of minimum memory space and time required for storage and computing defect data and also the flexibility of approach offering a user friendly interface and simplification of the	PCT filing 19.08.98	National Entries due by 19.02.2001	Appl/Inv.: VILKOV Inv.: DEAS To be assigned to Process Int Ltd.
1102	US 09/377,172 US 6,366,995		transformation procedure. The system comprises: a receiving means for receiving a representative plurality of pairs of addresses, each pair consisting of one memory cell address in the first address space and one address in the second address space, a storage means for storing said pairs of addresses, and	US filed 19.08.99 (19.08.98)	GRANTED 16 July 2001 Abandoned 2 October 2007 450$ (renewal) + 1640$ restoration)	Appl/Inv.: Vilkov, Deas Assigned to ACUID Guernsey
1103	Canada 2,341,014		a computing means for computing transformation formulas.	19.08.98 CA Entry	Request for Examination filed	Appl/Inv. Deas, Vilkov

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				19.02.01	19.08.2003	
12. 1201	PCT/RU98/00377 WO 00/29958 Publ. 25.05.00	System and Method of Transformation of Memory Device Addresses	A system for transformation of device addresses between different device topologies, each topology having its address space, providing the use of minimum memory space and time required for storage and computing defect data and also the flexibility of approach which allows mapping of memory device divided into an arbitrary number of tiles, each tile having different mapping scheme from a wide spectrum of mapping classes.	PCT filing 12.11.98	National Entries due by 12.05.2001	Appl/Inv: Vilkov, Inventor: DEAS Assigned to Process Intel. Ltd.
1202	US 09/423,804 US 6,393,543			12.11.99 (12.11.98)	GRANTED 14 Dec 2001 Renewal by 21 may 2009	ACUID Corp.Guer Vilkov, Deas
1203	Canada 2,346,831			Filed 08.04.2001	Exam to be requested by 12.11.2003	Vilkov, Deas
13. 1301	PCT/RU98/00414 WO 00/34797 Publ. 15.06.2000	linterface system for current drive mode memory devices	An interface system comprising a driver and a receiver for providing a low cost high speed signal transfer to and from a high speed current drive mode device, such as a Rambus device.	PCT filing 10.12.98		Process Int. (Stepanov, DEAS)
1305	EP 98966990.8 EP(GB) 1,137,953 DE69806275			Filed by 10.07.2001	GRANTED 26.06.02 Abandoned Renewal not paid	ACUID (Guernsey) Inv. Deas, Stepanov
1302	US 09/457,479	A Tester Interface System for Current Drive Mode Memory device		US filed 09.12.99	ABANDONED	Process Int. Deas; Stepanov
1308	Singapore 200103396-8			Filed 8.06.2001	Pending	Acuid Corp. (Deas, Stepanov)
1304	Japan 2000-587200			Filed 10.06.01	Pending	Acuid Corp. (Stepanov, Deas)
15		Semiconductor Device Processing and Sorting Apparatus and Method of Handling	A semiconductor device processing and sorting apparatus comprising inclined guideways for guiding the semiconductor devices. The inclined guideways include an input guideway; testing guideways spaced in the direction transverse to their sliding surface; and Sorting guideways.		Demand filed in EPO on 13.05.2001 National Entry by 13.04.02	Appl/Inv. Davidov Assigned to Process Int. Ltd.
1502				04.04.02	Abandoned	Appl/Inv. Davidov Assigned to Acuid Corp. Ltd.
16	PCT/RU00/00136	Apparatus for processing and Sorting Semiconductor Devices received in trays	A semiconductor device test handler which is adaptable to receive various customer tray configurations, e.g. JEDEC trays, and automatically test the ICs within.	PCT filing 06.03.00	Demand due By 06.10.2001	Appl/Inv. Davidov Assigned to Process Int. Ltd
1602	US 09/986,523			US filing 02.11.01 (prior 06.03.00)	Pending Abandoned	Appl/Inv. Davidov Assigned to Acuid Corp. Ltd
1607	RU 2001130173			Filed 06.12.01 (06.03.00)		Davidov
17	PCT/RU00/00149	Pressure Actuated Zero Insertion Force Socket	A connector for wide modules or devices that maintains excellent impedance control over a long life. Enables very high frequency devices to be tested or used in sockets.	20.04.00	National entries by 20.12.01	Davidov
1702	US 09/582,733 US 6,712,630			27.06.2000	Granted 30.03.04 Renewal by 30.03.07	ACUID CORP. (Guernsey) Limited Davidov
1707	RU 2001136102			21.01.00	Request for	Davidov

				(prior. 20.04.00)	exam 20.04.03	
18	PCT/RU00/00188 EP 00957155.5	Timing Control Means for Automatic Compensation of Timing Uncertainties	A means to achieve interfaces with low skew across data channels. Relates to automatic self-calibration of timing skew in receivers and transceivers using analog increments, wherein for each register a corresponding feedback loop is provided for the alignment of register's timing to generate a feedback signal. The invention is described with example embodiments that form a self calibrated receiver and a self calibrated transmitter.	22.05.00	Demand filed by 22.12.01 PCT appl. filed on 22.05.01	Appl. Abrosimov Inv.(s): Abrosimov, Deas
1902 prov	Provisional US 60/209,613	Test Systems for Protocol Memories	The invention relates generally to computer-controlled automatic test systems for testing integrated circuit and discrete devices, and more particularly to memory test systems with interchangeable heads which interface with high speed protocol memories such as DDR and RAMBUS devices, as well as synchronous DRAM.	06.06.00		Appl.: Deas Inv. Abrosimov, Deas
1901	PCT/RU01/00234	Data Processing System	A data processing system for high speed data communication and chip-to-chip data transfer. Input and output data are provided at high frequency, while data transferring sections are operable at low frequency, which is highly advantageous when interfacing with high speed protocol memories such as SDRAM, in particular DDR.	06.06.2001 (06.06.2000)	US filed by 06.02.02	AbrossimovKlotchkov,
1902	US 10/066,775	Data Processing System		06.06.2001 (06.06.2000 Entry under Chapter I 06.02.02	Abandoned	Abrossimov Klotchkov,
20	US 60/216,468	Subsystem with transmission data storage	A board provided with a means to compensate for uneven transmission line performance, e.g. caused by crosstalk or crosstalk artifacts using stored data on transmission characteristics.	06.07.00		Appl.: Abrossimov Inv. Deas; Abrosimov
2001	PCT/RU01/00289	Interface device with stored data on transmission line characteristics	An interface device provided with a means to compensate for uneven transmission line performance, e.g. caused by crosstalk or crosstalk artifacts using stored data on transmission line characteristics relating to a specific data pattern.	06.07.2001 (06.07.00)	US filing by 06.03.02	Appl./Inv. Abrossimov
2002	US 10/090,829			06.03.02 (06.07.00; 06.07.01)	Grant fee to be paid by 13.05.07	AbrossimovDeas
21	PCT/RU00/00339	A method and apparatus for controlling acceleration and velocity of a stepper motor	A method and apparatus for controlling acceleration and velocity of a stepper motor in which a phase offset is selected depending on motor velocity. The minimal phase offset indicates the position of the winding which generates the maximal driving moment. Increases speed by a factor of 10, max load by a factor of 3.	15.08.00	Demand was not filed by 15.03.02	Appl. Davidov Inv. Davidov
2102	US 10/367,017 US 2003-0137273 US 6,870,346			14.02.03 (15.08.00)	GRANT 22.03.05 IN FORCE Renewal by 22.03.08	Acuid Corp. (Guernsey)
22	PCT/RUO1/00202	Timing control means for automatic compensation of timing uncertainties	Automatic self-calibration of timing skew in transceivers, wherein a set of feedback loops is arranged for controlling even rising, even falling and odd rising edges.	22.05.2001 prior. 22.05.00 28.08.00		Appl./Inv: Abrossimov Inv.Deas
2202	US 09/898,250 Publ. US 2001-0056332 US 6,834,255			Filed on 03.07.01 (22.05.00; 28.08.00)	Grant 21.12.04 IN FORCE 21.12.07 4th year Renewal	Appl./Inv: AbrossimovDeas
2204	Japan 2001-587191 JP13-587191			Filed on 27.09.01	Pending Request for	Acuid UK Inv.: Abrosimov,

					exam by 22 May2008	Deas
2205	EP 01941340.0			22.12.02 (22.05.00 28.08.00)	Response filed 5th year renewal was not paid	Acuid Corp. (UK)
2200	Provisional application US 60/228,115			28.08.00		Appl./Inv: Abrossimov
23	Provisional application US 60/238,028	Timing delay generator and method using temperature stabilisation	A timing delay generator for supplying a signal delayed by a predetermined period. The generator comprises a vernier that provides variable delays for a main signal, the delays being sensitive to temperature variation, a sensor for sensing the vernier's temperature and a feedback loop to maintain the temperature of the silicon die at a constant level and thus, to provide the high long-term accuracy of the timing delay generator.	06.10.00	Regular application filed by 06.10.01	Abrosimov, Deas
2302	US 10/090,815			06.03.02	Restored Response filed on the 11 Oct 2006, ready for grant	Abrosimov Acuid Corp.
24	Provisional application US 60/244,178	Low Swing Communication System	Low Swing Transceiver, where feedback parameters influence the signal swing of the transmitter. The transceiver comprising a receiver for generating a signal indicative of parameters bearing information on the maximum and minimum levels, e.g. voltage, current or other levels, to cause a signal to be received as a logical one and as a logical zero. This parameter signal may be digital, but is preferably a differential analogue signal. The parameters influence the signal swing of the transmitter.	Filed on 31.10.2000		Alex Deas
2401	PCT/RU01/00485			Filed on 31.10.2001 (31.10.00)		Applicant: Atyunin Inv.: Deas, Atyunin
2405	EP 01 993 095.7 EP(GB)1,410,590 DE60110129			Nat. Entry 30.05.03	GRANT 13.04.05 In force Renewal by 31.10.07	ACUID CORP. (Guernsey) Limited
2402	US regular 09/985,725 US 2002-0052186			Filed on 06.10.2001 (31.10.00)	Abandoned for non response to OA 21.02.06	Atyunin Deas
25	Provisional application US 60/244,177	Transceiver with differential termination	Means to drive double power into a transmission line without affecting the impedance of the receiver. Transmitter comprises a series of drivers having terminating resistors joined at a common point. The drivers are controlled such they either all drive the same signal or one driver or group of drivers drives the inverse to the other signal. The transceiver has the improved high speed characteristics whilst simplified implementation.	Filed on 31.10.2000		Deas
2501	PCT/RU01/00484	Transmitter with active differential termination	Transmitter comprises a series of drivers having terminating resistors joined at the transmission line. The drivers can operate in two modes: either an input signal is transmitted in a communication line, or the drivers act as a parallel termination circuit, while no actual data is transmitted in this mode.	Filed on 31.10.2001 (31.10.00)		Appl/Inv. Atyunin Inv. Alex Deas
2502	US 10/425,638 US 6,788,102			Filed 30.04.03 (31.10.00)	GRANT 13.05.04 In force Renewal by 7 Sep 2007	ACUID Corp Guern Ltd
2505	EP 01 993 094.0 EP(GB)1,410,589			Filed 30.05.03 (31.10.00)	GRANT 25.10.04 In force	ACUID CORP. (Guernsey) Limited

	DE6011028				Renewal by 31.10.07	
26	Provisional application US 60/244,179	Pattern dependent driver	A means to compensate for the skew of a signal as a function of the data pattern being transmitted. The data pattern is compared directly or indirectly with stored values or parameters, the result of which is used to vary the skew of the signal, such as by changing the driver power or by adding or subtracting delay elements to the signal.	Filed on 31.10.00	See Appl. 34	Igor Abrossimov
28	GB 0026849.0	DDR SDRAM Memory Test System With Fault Strobe Synchronisation	A means to increase the timing window for DDR devices where the main apparatus uses a different strobe than that generated by the device. The test system comprises a synchronisation unit for triggering fault strobe generators with respect to DQS signals from the memory device under test.	Filed 03.11.00		Acuid Corporation (Gurensey)Ltd. Inv. Deas, Abrosimov
2801	PCT/RU01/00486 WO 02/039459	System for Communicating With Synchronous Device	A system for communicating with synchronous devices with a means to increase the timing window for DDR devices where the main apparatus uses a different strobe than that generated by the device. The test system comprises a synchronisation unit for triggering fault strobe generators with respect to DQS signals from the memory device under test.	Filed 05.11.01 (prior 03.11.00)	Nat Entry 03.05.03 Demand 03.06.02	Appl/Inv. Abrossimov
2802	US 10/ 425,629 US 2003-0191995			Filed 30.04.00 (03.05.00)	OA of 18 Jul 2006 Due date 18.10.06	Deas, Abrosimov
2809	DE 10196856.6 (Utility Model)			Filed 02.05.03 (03.05.00)	Abandoned renewal fee is not paid	ACUID Corp. Guernsey
2902	Prov. US 60/251,983	High Precision Receiver With Skew Compensation	A means to control the hysteresis of a receiver by shifting the reference voltage so as to compensate the hysteresis and reduce the skew caused by it. To avoid oscillation, the reference voltage can be switched over with a certain delay providing the voltage level has reached its stable state. The reference values and hysteresis values may be stored in a read-only memory.	11.12.00		Deas, AbrossimovAtuinin
2902	US 10/012,779 US 6,642,764	High Precision Receiver With Skew Compensation		10.12.01 (prior 11.12.00)	Grant 04.11.03 4.11.2006 4th year	Acuid Corp. Guernsey Deas, Abrossimov Atuinin
30	PCT/RU01/00128	Handler for Electronic Circuits	A testing and handling system for printed circuit boards, circuit modules, etc, wherein modules are handled in cassettes.	22.03.01	Published	Appl/inv.: Davidov. Inventors: Korolev, Evtukhov
					Abandoned	
31	Prov. US 60/293,053	Programmable Self-Calibrating Vernier and Method	The present invention is directed to the field of generation of precise electrical signals, in particular, to a technique for generating accurate delay of clock signals using a programmable delay line thus providing a self-calibrating vernier device.	Filed 21.05.01	Demand filed 18.12.02	Atuinin, Deas
3101	PCT/RU02/00241			Filed 21.05.02		Atyunin, Deas
3102	US 10/151,185 US 7,026,850			Filed 21.05.02	GRANT 11.04.06 11 April 2009 4th year	ACUID CORP. (Guernsey) Limited Atyunin, Deas
3105	EP 02736324.1 EP 1,410,504		A vernier for delaying an input main signal with an adjustable delay.	21.12.03 (21.05.02; 21.05.01)	Grant Decision Abandoned for non payment of 5th year	Acuid UK
32	Prov. US60/315,907	Noise reduction means	A means to reduce the noise in a signaling system to enable smaller noise	Filed 28.08.01		Deas,

			margins between logical levels. The invention also improves the tolerance of extremely high speed microcircuits to electrostatic discharges.			Atuinin, Abrosimov
3202	Regular US 10/229,082	Adaptive Equaliser for Reducing Distortion in a Communication Channel	An adaptive equaliser comprising a variable filter for modifying a signal to reduce the noise and enable smaller noise margins between logical levels. The equaliser comprises a means for measuring the received signal so as to determine the width of the eye opening in the eye diagram of the received signal; and a control means for adjusting a filter parameters based on the determined width of the eye opening. Preferably, the means for measuring the received signal constructs a digitised representation of the signal.	Filed 28.08.02	OA of 30.11.05 Not responded Deadline 30.05.06	Deas, Atuinin, Abrosimov
3201	PCT/IB02/03542			28.08.02 (28.08.01)		Abrosimov
3205	EP 02758748.4 EP(GB)1423923 DE60204156			28.03.04 (28.08.02; 28.08.01)	GRANT 12.11.04 Abandoned renewal 28.08.06 Not paid	ACUID CORP. (Guernsey) Limited
33	Prov US 60/293,052	Data Transmission Means And Method	Double ended active termination, where the termination is set by a self-calibration procedure to match the actual impedance of the line. This should include things like having the driver impedance controllable. This patent recognises that when a circuit board is made it has a design impedance and an actual impedance which may differ across the board. Here the drivers and receivers terminate the line to the actual impedance of the line, and drive using the actual impedance in order to reduce the size of the reflections that would appear.	Filed 21.05.01		Atuinin, Abrosimov
3301	PCT/RU02/00242			Filed 21.05.02		Atuinin, Abrosimov
3302	US 10/151,186 US 6,741,095			Filed 21.05.02	GRANT 25.05.07 renewal	ACUID CORP. (Guernsey) Limited Atuinin, Abrosimov
3301 EP	EP 1 405 154 EP 02736325.8			Nat. Entry 21.11.2003 (21.05.02)	Notification of Grant 12.07.05 Grant + claims to be paid by 30.11.06	ACUID UK
34	Prov US 60/310,299	Transmitter Circuit Comprising Timing Deskewing Means	Reduction of the data-dependent skew caused by line mismatch artefacts. A timing deskewing means adjusts the timing position of a signal transition between two logical levels by using information obtained as a result of history analysis.	Filed on 06.08.2001		Appl./Inv. Atunin, Deas
3401	PCT/RU01/00482			31.10.01 (31.10.00 06.08.01)		Appl./Inv. Atunin, Deas
3402	US 6,480,021 US 09/985,726			Filed 06.11.01	GRANT 12.11.02 Renewal 12.11.06	ACUID CORP. (Guernsey) Limited Appl./Inv. Atunin, Deas
3404	JP 2002-540310 JP14-540310			Filed 30.04.03 (31.01.00)	Pending OA responded	Acuid Corp. Guernsey
3405	EP 01993062.7 EP(GB)1,405,154 DE60111654			Filed 30.05.03 (31.01.00)	GRANT 12.05.05 In Force Renewal by 31 Oct 07	ACUID CORP. (Guernsey) Limited
35	PCT/RU01/00233	High Speed Protocol Memory Test Head For Memory Tester	This invention relates to a tester head which interfaces with high speed protocol memories such as RAMBUS devices. A memory test system head conditions the signals applied to the Device Under Test (DUT).	06.06.01 (06.06.00)	ABANDONED	AbrossimovAtunin

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36	UK 0111181.4	Channel Time Calibration Means	A high-speed communicational channel with a means for measuring time offsets between different signals that form the communication channel, at different frequencies and/or for different data patterns. transmitted through the channel, a storage means for storing the measured time offsets, and a timing correction means for applying the measured time offsets to compensate for said inter-signal skew.	28.03.2001		Abrosimov, Deas
3601	PCT/RU01/00365			06.09.2001 (31.10.00, 06.08.01)		AbrossimovAtyunin
3602	US 10/425,630 US 2003-0198309			Filed 30.04.03 (31.10.00)	Response to OA to be filed by 6 Jan 2007	Acuid Corp. Guernsey Ltd
3605	EP 01970401.4			Filed 30.05.03 (31.10.00)	OA 06.05.06 Abandoned for Non Renewal 30.09.06	Acuid Corp Ltd. UK
37	UK 0107692.6	Receiver With Optimised Bit Error Rate	A device and method employing the characteristic of metastability within the receiving registers to measure and control the characteristics of the channel and to compensate for production tolerances by altering the timing characteristics of the signal at the receiver.	27.03.2001	Regular appl. #39 filed 27.03.02	Abrosimov
3800	Provisional application US 60/314,496	Memory Test Apparatus and Method of Testing	A tester for testing memory devices, employing successive data processing algorithms with minimum feedback. Test instructions are generated in which fields are allocated for controlling respective functional parts of the tester. Control signals are stored together with data signals in an instruction memory that provides high speed test pattern generation. The width of instruction memory can vary.	24.08.01		AbrossimovAzarov, Kourbanov, Pankratov, Pyko, Khavin
3802	US 10/225,528 US 2003 –0099139 Publ.29.05.03			22.08.02	Notice of Allowance issue fee not paid; notice of abandonment 28.11.05	
3900	Provisional application US 60/317,216	Receiver With Automatic Skew Compensation	A self calibrated receiver for high speed transmission of data, wherein the data transmitted are oversampled and latched at the moment when the signal has a maximal stability. The self calibrating receiver comprises a plurality of samplers for latching data, coupled with a set of delay devices for providing a series of signal copies with each copy being shifted by a predetermined time interval, a comparator, a state machine for determining a number of copy with minimal BER, a multiplexer, and a pipeline of latency adjustment elements.	06.09.01		Abrossimov Deas
3901	PCT/RU02/00120			26.03.02 (27.03.01 06.09.01, 29.12.01)		Abrosimov,Deas
3909	UK 0131100.0			29.12.01	Abandoned as EP granted	Acuid Corporation Ltd.
3902	US 10/038,868 US 2003-0014683			08.01.02	Ready to grant Abandoned for failure to response to notice of non compliance of 11.10.05	AbrossimovDeas
3905	EP 02738994.9 EP(GB) 1,386,441 DE60201030		A self calibrating receiver with a plurality of samplers and a polyphase clock generator, for providing a series of signal copies, wherein the sampler produces a signal having the lowest Bit Error Rate by defining a sample copy closest to the minimum in BER distribution.	26.03.02 (prior of 27.03.01, 06.09.01, 29.12.01)	Granted 08.07.04 Abandoned Renewal + extra 26.09.06	Acuid Corp. (Guernsey) Ltd.
3904	JP 2002-576341 JP14-576341					
40	UK 0216453.1	High Speed Interface Device	The present invention is focused on interconnect within a single board, to provide either a synchronous conveyor or packet communications that deliver reliable interconnect at or close to theoretical limit, suiting both low latency and latency tolerant applications respectively.	16.07.02	Abandoned	Acuid Corporation Limited

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4200	UK 0202366.1	Means and method of data encoding and communication at rates above the channel bandwidth	A coding means reduces artifacts introduced by sending data at a higher rate than the bandwidth of the communication channel, such as the voltage and current offsets introduced in the data at the receiver as a function of the preceding data.	01.02.02		Acuid Corporation(Gurnsey)Limited
4202	US regular 10/079,260 US 7,092,439			21.02.02 (prior of 01.02.02)	GRANT Issue fee paid 30.06.06 Renewal by 17.08.09	ACUID CORP. (Guernsey) Limited Abrosimov Deas, Faulds
4201	PCT/IB03/00356 WO 03/065670		Coding means for coding 8 bit input symbols into 16 bit output codes for transmitting along a channel by signals having a limited minimum and maximum pulse width.	29.01.03 (21.02.02; 01.02.02)		Abrosimov Deas, Faulds
4221	US 10/656,143 US –2004-0047413 (CIP of PCT/IB03/00356) US 6,806,817		Coding means for encoding 8 bit input symbols into 12 bit output codes for transmitting along a channel by signals having a limited minimum and maximum pulse width. The coding means reduces artifacts introduced by sending data at a higher rate than the bandwidth of the communication channel.	08.09.03 (29.01.03; 01.02.02)	GRANT IN FORCE Renewal by 17 Oct 2006	ACUID CORP. (Guernsey) Limited Abrosimov
4231	US 60/556,971	Means and method of data encoding and communication at rates above the channel bandwidth	Coding means for encoding data represented by input symbols into codes, to have the minimum signal pulse width longer than one period of the receiver's sampling clock, the minimal pulse width being equal to 3 bit intervals. A preferred example is 8b/16b DC balanced code, which expands 8 bits of real data into 16 bits codes.	23.03.04		Abrosimov
4231	US 10/814,576 regular, CIP of US 10/656,143			01.04.04 (23.03.04; 08.09.03; 29.01.03 21.02.02; 01.02.02)	Notice of Abandonment 17.02.06	Abrosimov
4230	UK regular 0407693.1			05.04.04	Request for exam 05.04.05	Acuid Corp. (Guernsey) Ltd.
43	US Provisional 60/361,691	Line Termination Incorporating Compensation For Device And Package Parasitics	A terminator for terminating a transmission line linking a plurality of integrated circuits, wherein the termination is distributed between terminating components in the package to compensate for the characteristics of the ESD structure on the receiver.	06.03.02		AbrossimovDeas
4300	UK 0208014.1			05.04.02	Regular	Acuid Corporation Limited
4301	PCT/IB03/00991 WO03/075462			06.03.03 (06.03.02; 05.04.02)		Abrosimov Deas
4302	US 10/383,727 US-2003-0190949			10.03.03 (06.03.02; 05.04.02)	Abandoned for non-response to OA	Acuid Corp. (Guernsey) Limited Abrosimov Deas
4305	EP 1 488 521 EP 03743472.7				Renewal + extra 30.09.06	ACUID UK. (Guernsey) Limited
44	US Provisional 60/361,690	Line Driver With Reduced Power Consumption	A means for reducing the power consumption of the transmitter by storing the recent history of the transmitted data and controlling driving transistors as a function of comparison of that history with input data so that either the signal is driven into the transmission line at full strength or at a level near the minimum needed to retain the state in the receiver. The advantage is that the line capacitance decays through the terminating resistors or discharge transistors, such that when the next state change is needed, then line has less stored energy needing to be discharged.	06.03.02		AbrosimovDeas
4401	PCT/IB03/00888 WO 03/075464			06.03.03 (06.03.02)	National Entry by 06.09.04	Abrosimov
4402	US10/384,266			10.03.03 (06.03.02)	Response to OA is filed	ACUID CORP. (Guernsey) Limited
45	US Provisional 60/383,121	High Speed Amplifier Incorporating Pre-Emphasis	An amplifier in integrated circuits for the transmission of digital signals at high speed, which incorporates a pre-emphasis circuit operating at speeds higher than the cut-off frequency that would normally apply to a such amplifier and pre-emphasis circuits.	28.05.02		Abrosimov, Deas
4501	PCT/RU03/00254			28.05.03	National Entry	Abrosimov

	WO 2003/100965 Publ.04.12.03			(28.05.02)	by 28.11.04	
4502	US 10/997,591			24.11.04	Response to OA shall be filed by 24 may 2007	ACUID CORP. (Guernsey) Limited Abrosimov;Deas
46	US Provisional 60/383,120	Reference Voltage Generator Providing Stable Gate Propagation Time	Reference voltage generator creates a voltage reference that is a function of the gate propagation time, and applies this to create circuits where a constant time characteristic is beneficial.	28.05.02		Abrosimov;Deas
4601	PCT/RU03/00241 WO2003/100973			28.05.03 (28.05.02)	National Entry by 28.11.04	Abrosimov
4602	US 10/997,592			24.11.04	Response to OA is filed	ACUID CORP. (Guernsey) Limited Abrosimov;Deas
47	US Provisional 60/383,131	Pull Up For High Speed Structures	Pull-up structures with variable strength, which combines a resistor network with N MOS transistors, such as N-type MOSFET to allow the pull up to be varied to compensate for process and temperature variations around a predefined pull-up strength, at the same time providing low parasitic capacitance and a good dynamic response of the pull-up structure.	28.05.02	PCT filed 28.05.03	
4701	PCT/RU03/00242 WO 2003/100974 Publ. 04.12.03			28.05.03 (28.05.02)	National Entry 28.11.04	Abrosimov
4702	CIP US 10/853,123			26.05.04 (28.05.02, 28.05.03)	NOTICE OF ALLOWANC 14.02.06 ISSUE FEE NOT PAID	Abrosimov, Deas, Dedov
4702	PCT/RU05/000304			Filed 26.05.05	FEE NOT PAID	
48	US 60/431,226	Strip-Line Topology For A High Speed PCB With Low Dissipation High Speed Low Dissipation PCB Topologies	A multilayer pcb comprising a plurality of planar layers made of dielectric material and a plurality of conductor traces secured with their rough surfaces to these dielectric material layers, their smooth surfaces looking outwards or facing each other in superposed laminar relation to form a coplanar structure, so that the skin effect losses in the circuit structure are reduced. The traces can be driven in parallel to form a single conductor line.	06.12.02		Abrosimov
4801	PCT/RU03/000529			27.11.03 (06.12.02)	Demand filed 06.07.04	Abrosimov
4802	US 11/144,625			Nat. Entry 06.06.05	Abandoned for non-payment of filing fee	Abrosimov Deas
4805	EP 03781178.3			Nat. Entry 06.07.05		
4900	UK regular UK 0228629.2	Simultaneous bidirectional differential signalling interface	Bidirectional differential point to point simultaneous high speed signalling between integrated circuits with highly effective echo cancelling. To increase the quality of receiving an input signal, another signal adjusted in phase and amplitude is coupled at the output of the receive buffer, so that the echoing of the input signal is cancelled.	09.12.02		ACUID Corp. (Guernsey)
4902	US regular 10/387,443			14.03.03 (09.12.02)	OA 14.06.06 Response by 14.12.06	ACUID CORP. (Guernsey) Limited Abrosimov, Deas, Coyne
4901	PCT/RU03/000530		Bidirectional differential point to point simultaneous high speed signalling between integrated circuits with highly effective echo cancelling. To increase the quality of receiving an input signal, another signal adjusted in phase and amplitude is coupled at the output of the receive buffer, so that the echoing of the input signal is cancelled. Additionally, the rise time of the this signal is adjusted to match the rise time of the first signal.	27.11.03 (14.03.03; 09.12.02)	Demand filed 09.07.04	Abrosimov
4902_2	CIP US regular 10/730,055			09.12.03 (14.03.03; 09.12.02)	Ready for Examination	ACUID CORP. (Guernsey) Limited Abrosimov, Deas, Coyne
4902-2	PCT/RU2004/ /000490			06.12.04		Abrosimov, Deas, Coyne

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	EP 03781179.1			Nat. Entry 11.07.05	Nat. Entry of PCT/RU03/00530	
5000	US regular US 10/882,236 US2006-0001496	Array Oscillator Circuit and Polyphase Clock Oscillator	A ring oscillator circuit having the improved high speed characteristics. Overcomes Rambus patents on array oscillators with novel new design with higher speed, far greater stability, lower jitter and ease of layout. The array oscillator circuit includes a series of ring oscillators each having a plurality of buffer stages using N-type MOSFET transistors.	02.04.04	OA 06.01.06 (Correct drawings) ABANDONED PETITION TO REVIVE	Abrosimov, Deas, Dedov
5000	PCT/IB2004/002410			15.07.04		Abrosimov
5100	US provisional US 60/552,723	Eye Tracking and Expansion Using Oversampled Signals	Oversampling system with means to operate with negative eye openings, and means to overcome channel Cross Talk. The system extracts data from a stream of oversampled data employing eye expansion at the same time as eye tracking. Can operate with a smaller eye size than in the prior art methods by detecting a small sequence of bits such as three, as being a valid bit, and tracking the eye at the same time.	15.03.04	PCT filed 15.03.05	Abrosimov, Deas, Faulds, Klotchkov
5100	UK provisional UK 0406843.3			26.03.04		ACUID Corp. (Guernsey) Ltd.
5101	PCTRU05/000118			11.03.05		Abrosimov
5200	US provisional US 60/558,154	Clock Recovery in an Oversampled Serial Communication System	Clock recovery from parallel data bits in an over-sampling receiver. The receiver comprises a clock recovery phase detector, a phase and frequency detector and a lock detector, wherein the frequency lock detector determines when lock is achieved, and once achieved, switches the phase detector to the clock recovery phase detector which extracts the frequency of the data from the over-sampled data to generate signals to achieve the clock recovery	01.04.04	PCT filed 01.04.05	Abrosimov, Coyne, Deas,
5200	UK provisional 0407694.9			05.04.04		ACUID Corp. (Guernsey) Ltd.
52PCT	PCT/RU05/000167			01.04.05		Abrosimov
5300	US provisional US 60/568,237	Clock Frequency Reduction in Communications Receiver With Coding	A communications receiver using coding techniques to reduce the clock frequency, power dissipation and VCO tuning range or obtain improvements in BER, communication distance or increased data rate in a given communications medium	06.05.04	PCT filed 06.05.05	Abrosimov, Coyne, Deas,
5300	UK provisional UK 0406843.3			06.05.04		ACUID Corp. (Guernsey) Ltd.
	PCT/RU05/00250			03.05.05		Abrosimov
5400	US provisional US 60/600,397	Impedance Controlled Interconnect Substrate and Package for High Frequency Electronic Device	A ball grad array (BGA) semiconductor package for high frequency semiconductor device and its fabrication method. The BGA package comprises a multi-layer printed circuit board interconnect substrate with a plurality of solder bumps of predefined size for mounting a Ball Grid Array Packaging type semiconductor component and provides a controlled impedance environment for transmitting high frequency differential signals.	11.08.04	PCT filed 11.08.05	Deas, Zemlianov, Bogachev
5400	PCT/RU2005/000422			11.08.05		
5500	US provisional US 60/584,531	Circuit for Clock and Data Recovery	A receiver containing a clock and data recovery circuit operating at a quarter-rate clock frequency is provided for high-speed signalling between integrated circuits. Each integrated circuit comprises a receiver for receiving a first signal from the other integrated circuit. The receiver has a clock and data recovery phase locked loop	02.07.04		Abrosimov, Coyne, Deas,
5500	PCT/RU05/000371			PCT filed 04.07.05		ACUID Corp. (Guernsey) Ltd.
5600	US provisional US 60/588,993	Re-Timer Circuit for Data Recovery With Fast Recovery from a Low Power Mode	Sampling and re-timing of data in a high speed communications interface between integrated circuits, where the receiver circuit has a power down state and fast recovery from said low power state. The communications receiver with a plurality of receive channels and a phase locked loop, wherein each channel comprises clock and data	20.07.04		Abrosimov, Coyne, Deas
5600	PCT/RU2005/00385			PCT filed		ACUID Corp.

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			recovery circuit, and the phase locked loop generates an output clock distributed to all receive channels, so that each receive channel aligns the output clock from the phase locked loop to the receive data for the same receiver channel.	20.07.05		(Guernsey) Ltd.
5700	US provisional US 60/602,660	Read Latency Minimisation Using Frame Offset	A communications receiver with reduced latency comprising a plurality of transceiver cells for receiving/transmitting frames of serial data from/to a host controller. The transceiver cells deserialises the data into a parallel data word of width equal to the number of bits in a frame; a memory interface controller for decoding the parallel frame data from the transceiver cells and generating control signals and data signals to memory device, performing write operations and for formatting read data and status information from the memory device to the transceiver cells for onwards transmission across the serial interface.	19.08.04	PCT filed 19.08.05	Abrosimov, Coyne, Deas,
5700	PCT/RU05/000438			19.08.05		ACUID Corp. (Guernsey) Ltd.
5800	US provisional US 60/606,127	Digital Filter With High Speed Response	A distributed summation digital filter applicable for processing of signals with ISI reduction or multi-mode fibre distortion compensation in high speed communications.	01.09.04		Abrosimov, Coyne, Deas,
5800	PCT/RU05/000598			PCT filed 21.11.05		ACUID Corp. (Guernsey) Ltd.