10-18-07

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

10-22-2007

103454931

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

SHEET

To the Director of the U.S. Paten... ...ched documents or the new address(es) below.

**1. Name of conveying party(ies)**

General Electric Capital Corporation

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

**2. Name and address of receiving party(ies)**

Name: Morgan Stanley & Co., Incorporated

Internal Address: Floor 7

Street Address: One Pierrepont Plaza

City: Brooklyn

State: New York

Country: U.S.A. Zip: 11201

Additional name(s) & address(es) attached? ☐ Yes ☑ No

**3. Nature of conveyance/Execution Date(s):**

Execution Date(s) September 26, 2007

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☑ Other Assignment of Patent Security Interest

**4. Application or patent number(s):**

☐ This document is being filed together with a new application.

A. Patent Application No.(s)
09/192955

B. Patent No.(s)
4700996

Additional numbers attached? ☑ Yes ☐ No

RECEIVED OPR ASSIGNMENTS DIV 2007 OCT 18 PM 5:00

**5. Name and address to whom correspondence concerning document should be mailed:**

Name: Rita M. Carrier

Internal Address: Sullivan & Cromwell LLP, Suite 800

Street Address: 1701 Pennsylvania Avenue, N.W.

City: Washington

State: D.C. Zip: 20006

Phone Number: (202) 956-7685

Fax Number: (202) 293-6330

Email Address: CarrierR@sullcrom.com

**6. Total number of applications and patents involved:** 753

**7. Total fee** (37 CFR 1.21(h) & 3.41) $ 30,120.00

☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☑ Enclosed
☐ None required (government interest not affecting title)

**8. Payment Information**

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number

Authorized User Name

00000130 09192955 30120.00 OP

**9. Signature:** Rita M. Carrier Oct. 18, 2007

Signature Date

Rita M. Carrier

Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 66

10/19/2007 TDIAZ1 01 FC:8021

**Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:**
**Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450**

**Continuation of Item 4(A)**
**of Patent Recordation Form**

08/938707
09/315806
09/441774
09/549980
09/609046
09/614363
09/620373
09/621315
09/629458
09/644698
09/648150
09/648902
09/689784
09/689786
09/811158
09/888438
09/909700
09/909704
09/910587
09/934443
09/997404
10/020854
10/058050
10/109835
10/112345
10/112366
10/112392
10/112430
10/137026
10/145110
10/171095
10/174718
10/197845
10/205877
10/207940
10/208123
10/210257
10/235221
10/310237
10/310400
10/345357
10/345371
10/356236
10/365658
10/414236
10/414238
10/414239
10/414245

Continuation of Item 4(A)
of Patent Recordation Form

10/425735
10/426003
10/429257
10/434340
10/607163
10/620387
10/620797
10/620835
10/626576
10/631988
10/650030
10/674825
10/682841
10/687196
10/695779
10/696146
10/715882
10/785575
10/835855
10/836932
10/837057
10/868181
10/899316
10/912722
10/976531
10/982149
11/027752
11/043038
11/049111
11/079409
11/091237
11/113805
11/116734
11/121975
11/136260
11/182900
11/218868
11/224376
11/235493
11/255,920
11/261,045
11/268,493
11/295,676
11/324,684
11/334,526
11/340,486
11/340,579
11/343,968

11/365,280
11/368,451
11/368,452
11/368,625
11/405,387
11/464,148
11/490,505
60/735,962
11/426,469

4754398
4761733
4771440
4807121
4859188
4891751
4901230
4911645
4960384
4964081
4965863
4975074
4982153
4984993
5003508
5014419
5015800
5041903
5054192
5055707
5081573
5083194
5107418
5127570
5127986
5128810
5134247
5142100
5142638
5144691
5159678
5165038
5166775
5168547
5168570
5170370
5175496
5175856
5175862
5179667
5179702
5182420
5185502
5187789
5193187
5193192
5193193
5194710

5196377
5197130
5202970
5202975
5202988
5206952
5208914
5211567
5218689
5226163
5226171
5239629
5245319
5247637
5247696
5251097
5253359
5257372
5258576
5258660
5258944
5261074
5269698
5272664
5276955
5281026
5283791
5283948
5287504
5293626
5295260
5307478
5321697
5325263
5329188
5339415
5343359
5347637
5349677
5355397
5358826
5361354
5367690
5371879
5381536
5386562
5388217
5390041

5390300
5390329
5392292
5414381
5418481
5423008
5428803
5430884
5434970
5434995
5442475
5452452
5453934
5467040
5481746
5487074
5491823
5495596
5499356
5504874
5509125
5524250
5524255
5526478
5526487
5528735
5533198
5535365
5537498
5544331
5544337
5555354
5557761
5561784
5564804
5566321
5581705
5583990
5586325
5592487
5593221
5598547
5613120
5623650
5625831
5634110
5640524
5652874

5654873
5655102
5659706
5659796
5661638
5662163
5664151
5669008
5671235
5671381
5678015
5680576
5682479
5686730
5689646
5692196
5694028
5694532
5694578
5696529
5696922
5699079
5701416
5706490
5709263
5710733
5717695
5717881
5717895
5721819
5721921
5727037
5727150
5730605
5732138
5734908
5735340
5736843
5737628
5742277
5745721
5748900
5751280
5757658
5761043
5761534
5761706
5764965

5765181
5765198
5768104
5768445
5768529
5768596
5770822
5774704
5778212
5784567
5784569
5784706
5787476
5790124
5790373
5790447
5790612
5793259
5797035
5801700
5801924
5802284
5802341
5802375
5802482
5805418
5805788
5811997
5812147
5812754
5812855
5815686
5817997
5818250
5821925
5822381
5825238
5826922
5829512
5831697
5832306
5834705
5835092
5835717
5835729
5835925
5841973
5848275

5848286
5848906
5854631
5861815
5861885
5861891
5862313
5864738
5867419
5870325
5872963
5875468
5880730
5880930
5889529
5893110
5896119
5897180
5900023
5907962
5909594
5913069
5915104
5920714
5923882
5924780
5928322
5930803
5933155
5940625
5946496
5957556
5958017
5960081
5960434
5960435
5963428
5963913
5963981
5967825
5970232
5974456
5974536
5977965
5982382
5986737
5987626
5991824

5991895
5995655
5999437
6002738
6018459
6026241
6026399
6029212
6031847
6034697
6044424
6049476
6049866
6055157
6055579
6055618
6059839
6061104
6065084
6067411
6073090
6075543
6077311
6078515
6081882
6085303
6091155
6092226
6098162
6101181
6104415
6105113
6108722
6111578
6112285
6112286
6115278
6115790
6116915
6119198
6128639
6128731
6128775
6131189
6132019
6137499
6142789
6144360

6148379
6151706
6160589
6166748
6167437
6167947
6169659
6171120
6172874
6173322
6173428
6181231
6181336
6182058
6182089
6182195
6193532
6195676
6205119
6208361
6215686
6216174
6219057
6219457
6223270
6226330
6226790
6230252
6233647
6233704
6239810
6243068
6249802
6256196
6256655
6256677
6259451
6275239
6278464
6279028
6279073
6280257
6281108
6282195
6282583
6289424
6292200
6293813

6301579
6301704
6305463
6308250
6313836
6314546
6330486
6331856
6336177
6339812
6342892
6345515
6349398
6353844
6353917
6357003
6359389
6366270
6366461
6373483
6381139
6381681
6389581
6393533
6397274
6406257
6417713
6418460
6421712
6428352
6433627
6434007
6438309
6441666
6448955
6452805
6453408
6457146
6460049
6476813
6480194
6480548
6483024
6483699
6486723
6487082
6487685
6493603

6496048
6496385
6496909
6512676
6513099
6513770
6516372
6518812
6529570
6529928
6532501
6532575
6535190
6541853
6545685
6546451
6550048
6553446
6556197
6559826
6564277
6567976
6571387
6574121
6578115
6578197
6593929
6594787
6600487
6601120
6601183
6604161
6604185
6611249
6615204
6618049
6621300
6622182
6629855
6633958
6634011
6643764
6650327
6650337
6651157
6651197
6654029
6657607

6657624
6672878
6674720
6678798
6680636
6681293
6683607
6683876
6683979
6684373
6686765
6701496
6703908
6711636
6714464
6714960
6718442
6721739
6724669
6726505
6728206
6728895
6732065
6738885
6751636
6751698
6751705
6754863
6760876
6765795
6766358
6766515
6769122
6771517
6775339
6775742
6779072
6791551
6795900
6799238
6803872
6809733
6809739
6813151
6813599
6813739
6816145
6816947

6819333
6829666
6829683
6831642
6831648
6831834
6831924
6839820
6839820
6839856
6842176
6845410
6853387
6853387
6853969
6853969
6856950
6859863
6859863
6864706
6877029
6877030
6879948
6882531
6885376
6900818
6901500
6904501
6915387
6915388
6918010
6920526
6920526
6924805
6925547
6938128
6950833
6950833
6971086
6971086
6973559
6973559
6981101
6981101
6982682
6982682
6985149
6985149

6985484
6985484
6986001
6986001
6993523
6993523
7007097
7007097
7007205
7007205
7009616
7009616
7012614
7012614
7016998
7016998
7027072
7027072
7031420
7031420
7034837
7034837
7058218
7058218
7058896
7058896
7062527
7062527
7064755
7064755
7068263
7068263
7069306
7069306
7088581
7088581
7089398
7089398
7092983
7092983
7100018
7100018
7120906
D337323
D341574
D363703
D367269
D373760

**Continuation of Item 4(B)**
**of Patent Recordation Form**

D393249
D393449
D395286
D396698
D398009
D417203
D419141
D419465
D429248
D431242
D436950
D444461
D444471
D444474
D445112
D445425
D463796
D464054
D464056
D464973
D473561
RE38134

# ASSIGNMENT OF PATENT SECURITY INTEREST

This Assignment of Patent Security Interest (this "Assignment"), dated as of September 26, 2007, is made by General Electric Capital Corporation, a corporation formed under the laws of Delaware (the "Grantor") as former Collateral Agent, in favor of MORGAN STANLEY & CO., INCORPORATED a Delaware corporation, located at One Pierrepont Plaza, Floor 7, Brooklyn, NY 11201 (the "Grantee"), as current Collateral Agent for the benefit of the Secured Creditors under the Security Agreement among the Grantor, Silicon Graphics, Inc., Silicon Graphics Federal, Inc. and Silicon Graphics World Trade Corporation, the other Grantors from time to time party thereto and the Morgan Stanley Senior Funding, Inc., dated as of October 17, 2006, (as amended, modified, restated, and/or supplemented from time to time, the "Security Agreement").

WHEREAS, pursuant to that certain Side Letter, dated as of September 11, 2007 (the "Side Letter"), the Grantee has succeeded Grantor as Collateral Agent under the Security Agreement;

WHEREAS, pursuant to the Patent Security Agreement dated October 17, 2006, Silicon Graphics Inc., pledged and granted to Grantor as the then Collateral Agent, for the benefit of the Secured Creditors, a continuing security interest in all collateral set forth in Paragraph 1 of such Patent Security Agreement, including the Patents set forth on Schedule A attached hereto (all such collateral together, the "Patent Collateral"); and

WHEREAS, the Patent Security Agreement was recorded in the Patent Division of the United States Patent and Trademark Office on October 24, 2006 at Reel 018545 and Frame 0777;

WHEREAS, the Grantor now desires to assign the entirety of its security interest in, to and under the Patent Collateral to the Grantee, as current Collateral Agent for the benefit of the Secured Creditors.

NOW, THEREFORE, for good and valuable in consideration, the receipt and sufficiency of which are hereby acknowledged, the Grantor agrees as follows:

1. The Grantor hereby irrevocably assigns, transfers and conveys, without representation or warranty of any kind by such Grantor and without recourse to such Grantor, all of its right, title and interest in, to and under such Grantor's continuing security interest in the Patent Collateral to the Grantee, as Collateral Agent for the benefit of the Secured Creditors.

2. The Grantor authorizes and requests that the commissioner for Patents and any other applicable government officer record this Assignment.

3. This Assignment may be executed in any number of counterparts and by the different parties hereto on separate counterparts, each of which when so executed and delivered shall be an original, but all which together shall constitute one and the same instrument.

4. This Assignment has been granted in conjunction with the security interest granted to the Grantee under the Security Agreement and the Side Letter. The rights and remedies of the Grantee with respect to the security interest granted herein are more fully set forth in the Security Agreement and the Side Letter, all terms and provisions of which are incorporated herein by reference.

5. This Assignment shall be construed in accordance with and be governed by the Laws of the State of New York.

[Signatures Appear on the Following Page]

IN WITNESS WHEREOF, the undersigned have executed this Assignment as of the 26 day of September, 2007.

GENERAL ELECTRIC CAPITAL CORPORATION, as Grantor

By: Ali Mirza
Name: ALI MIRZA
Title: Duly Authorized Signatory

MORGAN STANLEY & CO., INCORPORATED, as Grantee

By:_____
Name:
Title:

[Assignment of Patent Security Agreement]

NY12529:415731

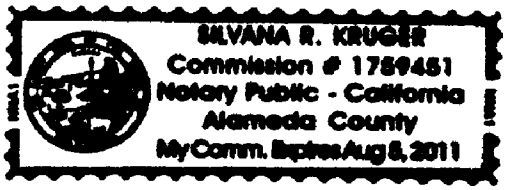
STATE OF CALIFORNIA)
) ss.:

COUNTY OF SAN FRANCISCO)

On this 26th day of September, 2007, before me, Silvana R. Kruger, the undersigned, a notary public in and for said state and county, personally appeared Ali Imran Mirza, proved to me on the basis of satisfactory evidence, to be the individual who executed the foregoing instrument on behalf of General Electric Capital Corporation, a Delaware corporation, as the duly authorized signatory of such corporation and acknowledged to me that the execution and delivery of said instrument was duly authorized by said corporation.

Notary Public

(Affix Seal Below)




NY12529:415731.1

IN WITNESS WHEREOF, the undersigned have executed this Assignment as of the __ day of September, 2007.

GENERAL ELECTRIC CAPITAL CORPORATION, as Grantor

By:_____
Name:
Title:

MORGAN STANLEY & CO., INCORPORATED, as Grantee

By:_____
Name: Gavin Baiera
Title: Authorized Signatory

[Assignment of Patent Security Agreement]

NY12529-415731

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| GB | MULTIDIMENSIONAL INTERCONNECTION AND ROUTING NETWORK FOR AN MPP COMPUTER | 07/06/2005 | 733237 |
| FR | MULTIDIMENSIONAL INTERCONNECTION AND ROUTING NETWORK FOR AN MPP COMPUTER | 07/06/2005 | 733237 |
| DE | MULTIDIMENSIONAL INTERCONNECTION AND ROUTING NETWORK FOR AN MPP COMPUTER | 07/06/2005 | 733237 |
| US | BUS CONTROL SYSTEM FOR ARBITRATING REQUESTS WITH PREDETERMINED ON/OFF TIME LIMITATIONS | 03/09/1993 | 5193193 |
| US | SYNCHRONIZED DRAM CONTROL APPARATUS USING TWO DIFFERENT CLOCK RATES | 01/12/1993 | 5179667 |
| US | RETAINING MEANS FOR REMOVABLE COMPUTER DRIVE AND RELEASE MEANS FOR THE SAME | 10/02/1990 | 4960384 |
| JP | COMPUTER THREE-WAY TRANSFER OPERATION | 10/20/2000 | 3120382 |
| US | COMPUTER THREE-WAY TRANSFER OPERATION | 11/09/1993 | 5261074 |
| FR | FILE CHARACTERIZATION FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 06/18/1997 | 511209 |
| GB | FILE CHARACTERIZATION FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 06/18/1997 | 511209 |
| JP | FILE CHARACTERIZATION FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 10/01/1999 | 2986209 |
| US | FILE CHARACTERIZATION FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 07/06/1993 | 5226163 |
| DE | FILE CHARACTERIZATION FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 06/18/1997 | 69030958.9 |
| US | RACK AND PINION RETAINING AND RELEASE DEVICE FOR REMOVABLE COMPUTER COMPONENTS | 06/28/1994 | 5325263 |
| US | COMPUTER-IMPLEMENTED METHOD AND AN APPARATUS FOR CONVERTING DATA ACCORDING TO A SELECTED DATA TRANSFORMATION | 12/02/1997 | 5694578 |
| US | COMPUTER-IMPLEMENTED METHOD AND AN APPARATUS FOR INPUTTING DATA STRUCTURE CHARACTERISTICS | 07/29/1997 | 5652874 |
| AU | COMPUTER MOUSE | 03/29/1993 | D116644 |
| US | COMPUTER MOUSE | 09/17/1996 | D373760 |
| BR | COMPUTER MOUSE | 03/26/1996 | MI5200051-6 |
| US | FILE ALTERATION MONITOR FOR COMPUTER OPERATING AND FILE MANAGEMENT SYSTEMS | 02/15/1994 | 5287504 |
| US | AN IMPROVED METHOD AND APPARATUS FOR CLOCKING IN A COMPUTER SYSTEM | 02/27/1996 | 5495596 |
| | | | |
| US | COMPUTER HOUSING | 11/23/1993 | D341574 |
| BR | COMPUTER HOUSING | 06/25/1996 | MI5200052-4 |
| AU | COMPUTER HOUSING | 07/06/1993 | 117575 |
| FR | COMPUTER HOUSING | 01/22/1992 | 920382 |
| GB | COMPUTER HOUSING | 10/14/1992 | 2020473 |
| US | THREE DIMENSIONAL NAVIGATION SYSTEM AND INTERFACE | 09/10/1996 | 5555354 |
| US | RETAINING AND RELEASE MECHANISM FOR COMPUTER STORAGE DEVICES INCLUDING A PAWL LATCH ASSEMBLY | 12/14/1993 | 5269698 |
| US | ELECTROMAGNETIC SHIELD FOR ATTACHMENT TO COMPUTERS | 07/13/1993 | D337323 |
| US | APPARATUS AND METHOD FOR DETECTING THE ACTIVITIES OF A PLURALITY PROCESSORS ON A SHARED BUS | 06/06/1995 | 5423008 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | A CENTRAL PROCESSING UNIT FOR PROCESSING A PLURALITY OF THREADS USING DEDICATED GENERAL PURPOSE REGISTERS AND MASQUE REGISTER FOR PROVIDING ACCESS TO THE REGISTERS | 06/04/1996 | 5524250 |
| US | CIRCULAR SCHEDULING METHOD AND APPARATUS FOR EXECUTING COMPUTER PROGRAMS BY MOVING INDEPENDENT INSTRUCTIONS OUT OF A LOOP | 01/31/1995 | 5386562 |
| US | A METHOD AND APPARATUS FOR DISPLAYING DATA WITHIN A THREE-DIMENSIONAL INFORMATIONAL LANDSCAPE | 06/18/1996 | 5528735 |
| US | A METHOD AND APPARATUS FOR INCLUDING SELECTED OBJECTS BY SPOTLIGHT | 09/23/1997 | 5671381 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VISUALIZING DATA USING PARTIAL HIERARCHIES | 10/24/2000 | 6137499 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR NAVIGATING THROUGH PARTIAL HIERARCHIES | 08/29/2000 | 6111578 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR MAPPING BETWEEN AN OVERVIEW AND A PARTIAL HIERARCHY | 07/10/2001 | 6259451 |
| US | METHOD AND APPARATUS FOR INDICATING SELECTED OBJECTS BY SPOTLIGHT | 01/19/1999 | 5861885 |
| US | HIGH MEMORY CAPACITY DRAM SIMM | 12/21/1993 | 5272664 |
| US | A SYSTEM AND METHOD FOR FAIR ARBITRATION ON A MULTI-DOMAIN MULTIPROCESSOR BUS | 04/16/1996 | 5509125 |
| US | A SYSTEM AND METHOD OF IMPLEMENTING READ RESOURCES TO MAINTAIN CACHE COHERENCY IN A MULTIPROCESSOR ENVIRONMENT PERMITTING SPLIT TRANSACTIONS | 04/02/1996 | 5504874 |
| US | SYSTEM AND METHOD OF IMPLEMENTING READ RESOURCES IN A MULTIPROCESSOR ENVIRONMENT | 09/02/1997 | 5664151 |
| US | SYSTEM AND METHOD FOR GENERATING A READ-MODIFY-WRITE OPERATION | 08/06/1996 | 5544331 |
| US | A SYSTEM AND METHOD FOR PIGGYBACKING OF READ RESPONSES ON A SHARED MEMORY MULTIPROCESSOR BUS | 08/05/1997 | 5655102 |
| US | THREE DIMENSIONAL MODEL WITH THREE DIMENSIONAL POINTERS AND MULTIMEDIA FUNCTIONS LINKED TO THE POINTERS | 06/11/1996 | 5526478 |
| US | THREE DIMENSIONAL MODEL WITH THREE DIMENSIONAL POINTERS AND MULTIMEDIA FUNCTIONS LINKED TO THE POINTERS | 11/06/2001 | 6313836 |
| US | TOP, SIDES AND FRONT PORTIONS OF A COMPUTER HOUSING | 10/31/1995 | D363703 |
| US | DISK DRIVE BRACKET | 10/15/1996 | 5564804 |
| US | TOP FRONT AND SIDE PORTIONS OF A COMBINED COMPUTER HOUSING AND SUPPORT STANDS | 02/20/1996 | D367269 |
| US | ARRANGEMENT FOR MODIFYING ELECTRICAL PRINTED CIRCUIT BOARDS | 11/10/1998 | 5834705 |
| US | A SYSTEM & METHOD OF PERFORMING TOMOGRAPHIC RECONSTRUCTION & VOLUME RENDERING USING TEXTURE MAPPING | 12/14/1999 | 6002738 |
| US | SYSTEM AND METHOD OF GENERATING OBJECT CODE USING AGGREGATE INSTRUCTION MOVEMENT | 09/17/1996 | 5557761 |
| US | LOOP SCHEDULER | 02/13/1996 | 5491823 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | SYSTEM AND METHOD FOR ENABLING, WITHOUT RECOMPILATION, MODIFICATION OF CLASS DEFINITIONS & IMPLEMENTATIONS IN AN OBJECT-ORIENTED COMPUTER PROGRAM | 03/18/1997 | 5613120 |
| GB | SYSTEM AND METHOD FOR CONDITIONALLY COMPILING A SOFTWARE COMPILATION UNIT | 10/14/1999 | 2307073 |
| US | SYSTEM AND METHOD FOR CONDITIONALLY COMPILING A SOFTWARE COMPILATION UNIT | 11/25/1997 | 5692196 |
| US | REMOTE CONTROL DESIGN | 09/08/1998 | D398009 |
| US | SYSTEM AND METHOD FOR OPTIMIZING A SOURCE CODE REPRESENTATION AS A FUNCTION OF RESOURCE UTILIZATION | 03/31/1998 | 5734908 |
| US | HIGH PERFORMANCE SINUSOIDAL HEAT SINK REMOVAL FROM ELECTRONIC EQUIPMENT | 01/20/1998 | 5709263 |
| US | CROSS-MODULE OPTIMIZATION FOR DYNAMICALLY-SHARED PROGRAMS AND LIBRARIES | 07/13/1999 | 5923882 |
| US | APPARATUS FOR GENERATING DIFFERENTIAL NOISE BETWEEN POWER AND GROUND PLANES | 08/11/1998 | 5793259 |
| US | SYSTEM AND METHOD FOR PROCESSING GRAPHIC LANGUAGE CHARACTERS | 09/01/1998 | 5802482 |
| US | EFFICIENT ULTRA LOW DROPOUT POWER REGULATOR | 04/07/1998 | 5736843 |
| US | FOUR-DIMENSIONAL GRAPHICAL USER INTERFACE | 10/14/1997 | 5678015 |
| US | HIERARCHICAL FAT HYPERCUBE ARCHITECTURE FOR PARALLEL PROCESSING SYSTEMS | 09/16/1997 | 5669008 |
| US | SYSTEM AND METHOD FOR NETWORK EXPLORATION AND ACCESS | 10/28/1997 | 5682479 |
| US | DIRECTORY-BASED COHERENCE PROTOCOL ALLOWING EFFICIENT DROPPING OF CLEAN-EXCLUSIVE DATA | 10/21/1997 | 5680576 |
| US | SYSTEM AND METHOD FOR MULTIPROCESSOR PARTITIONING TO SUPPORT HIGH AVAILABILITY | 11/23/1999 | 5991895 |
| US | FLAT PANEL MONITOR COMBINING DIRECT VIEW WITH OVERHEAD PROJECTION CAPABILITY | 12/09/1997 | 5696529 |
| US | MULTI-LAYER FLAT PANEL DISPLAY SCREEN APPARATUS | 11/16/1999 | 5986737 |
| US | FLAT PANEL DISPLAY SCREEN APPARATUS WITH OPTICAL JUNCTION AND REMOVABLE BACKLIGHTING ASSEMBLY | 11/03/1998 | 5831697 |
| US | REMOVABLE BACKLIGHTING ASSEMBLY FOR FLAT PANEL DISPLAY SUBSYSTEM | 04/20/1999 | 5896119 |
| US | REMOVABLE BACKLIGHTING ASSEMBLY FOR FLAT PANEL DISPLAY | 11/07/2000 | 6144360 |
| US | OVERHEAD PROJECTOR FOR FLAT PANEL DISPLAY CAPABILITY | 01/14/1997 | 5593221 |
| US | PROCESSOR-INCLUSIVE MEMORY MODULE | 01/20/1998 | 5710733 |
| US | PROCESSOR-INCLUSIVE MEMORY MODULE | 12/07/1999 | 5999437 |
| US | PROCESSOR-INCLUSIVE MEMORY MODULE | 02/02/1999 | 5867419 |
| US | DISTRIBUTED GLOBAL CLOCK SYSTEM | 10/13/1998 | 5822381 |
| US | PROGRAMMABLE, DISTRIBUTED NETWORK ROUTING | 02/24/1998 | 5721819 |
| US | APPARATUS AND METHOD FOR PAGE MIGRATION IN A NON-UNIFORM MEMORY ACCESS (NUMA) SYSTEM | 03/10/1998 | 5727150 |
| US | SYSTEM & METHOD FOR MAINTAINING COHERENCY OF VIRTUAL-TO-PHYSICAL MEMORY TRANSLATIONS IN A MULTIPROCESSOR COMPUTER | 07/28/1998 | 5787476 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | SYSTEM AND METHOD FOR MAINTAINING COHERENCY OF VIRTUAL-TO-PHYSICAL MEMORY TRANSLATIONS IN A MULTIPROCESSOR COMPUTER | 01/30/2001 | 6182195 |
| US | CACHE COHERENCY USING FLEXIBLE DIRECTORY BIT VECTORS | 05/27/1997 | 5634110 |
| EP | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 11/03/1999 | 826179 |
| FR | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 11/03/1999 | 826179 |
| GB | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 11/03/1999 | 826179 |
| US | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 06/16/1998 | 5768529 |
| DE | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 11/03/1999 | 69605037.4 |
| US | SYSTEM AND METHOD FOR INPUT/OUTPUT FLOW CONTROL IN A MULTIPROCESSOR COMPUTER SYSTEM | 10/26/1999 | 5974456 |
| TW | DUAL IN-LINE MEMORY MODULE (DIMM) | 09/01/1997 | 86284 |
| IN | DUAL IN-LINE MEMORY MODULE (DIMM) | 08/31/2002 | 188196 |
| KR | DUAL IN-LINE MEMORY MODULE (DIMM) | 05/21/1999 | 215267 |
| AU | DUAL IN-LINE MEMORY MODULE (DIMM) | 05/15/1996 | 707453 |
| GB | DUAL IN-LINE MEMORY MODULE (DIMM) | 05/14/1996 | 744748 |
| EP | DUAL IN-LINE MEMORY MODULE (DIMM) | 10/18/2000 | 744748 |
| FR | DUAL IN-LINE MEMORY MODULE (DIMM) | 10/18/2000 | 744748 |
| IT | DUAL IN-LINE MEMORY MODULE (DIMM) | 10/18/2000 | 744748 |
| EP | DUAL IN-LINE MEMORY MODULE (DIMM) | 04/10/2002 | 1020864 |
| FR | DUAL IN-LINE MEMORY MODULE (DIMM) | 04/10/2002 | 1020864 |
| GB | DUAL IN-LINE MEMORY MODULE (DIMM) | 04/10/2002 | 1020864 |
| DE | DUAL IN-LINE MEMORY MODULE (DIMM) | 10/18/2000 | 69610662 |
| DE | DUAL IN-LINE MEMORY MODULE (DIMM) | 04/10/2002 | 69620650.1 |
| US | HIGH MEMORY CAPACITY DIMM WITH DATA AND STATE MEMORY | 08/04/1998 | 5790447 |
| US | HIGH MEMORY CAPACITY DIMM WITH DATA AND STATE MEMORY | 04/11/2000 | 6049476 |
| US | SYSTEM & METHOD TO REDUCE PHASE OFFSET & PHASE JITTER IN PHASE-LOCKED & DELAY-LOCKED LOOPS USING SELF-BIASED CIRCUITS | 03/10/1998 | 5727037 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | RAID SYSTEM WITH FIBER CHANNEL ARBITRATED LOOP | 09/22/1998 | 5812754 |
| US | HEATSINK AND METHOD OF FORMING A HEATSINK | 11/03/1998 | 5829512 |
| US | SYSTEM AND METHOD FOR SAVING STATE INFORMATION IN AN INTERACTIVE TELEVISION SYSTEM | 11/10/1998 | 5835717 |
| US | SYSTEM AND METHOD FOR MEDIA STREAM SYNCHRONIZATION WITH A BASE ATOM INDEX FILE AND AN AUXILIARY ATOM INDEX FILE | 05/12/1998 | 5751280 |
| US | SYSTEM & METHOD USING COVER BUNDLES TO PROVIDE IMMEDIATE FEEDBACK TO A USER IN AN INTERACTIVE TELEVISION ENVIRONMENT | 09/01/1998 | 5802284 |
| US | SYSTEM AND METHOD FOR RESOURCE RECOVERY IN A DISTRIBUTED SYSTEM | 04/27/2004 | 6728895 |
| US | SYSTEM AND METHOD FOR COORDINATING COMMUNICATION BETWEEN LAYERS OF A LAYERED COMMUNICATION SYSTEM | 07/21/1998 | 5784567 |
| US | MULTI-CONFIGURABLE PUSH-PULL/OPEN-DRAIN DRIVER CIRCUIT | 09/22/1998 | 5811997 |
| US | SYSTEM AND METHOD TO REDUCE PHASE JITTER IN DELAY-LOCKED LOOPS | 08/04/1998 | 5790612 |
| US | ANTIALIASING OF SILHOUETTE EDGES | 04/21/1998 | 5742277 |
| US | OPERATING SYSTEM HAVING A MECHANISM FOR HANDLING A GROUP OF RELATED PROCESSES RESIDING ON SEPARATE MACHINES | 08/21/2001 | 6279028 |
| US | DIMM PAIR WITH DATA MEMORY AND STATE MEMORY | 11/11/1997 | 5686730 |
| US | ACKNOWLEDGE TRIGGERED FORWARDING OF EXTERNAL BLOCK DATA RESPONSES IN A MULTIPROCESSOR | 11/03/1998 | 5832306 |
| US | SYSTEM AND METHOD FOR UNCACHED STORE BUFFERING IN A MICROPROCESSOR | 10/05/1999 | 5963981 |
| US | SYSTEM AND METHOD FOR GENERATING AND DISPLAYING COMPLEX GRAPHIC IMAGES AT A CONSTANT FRAME RATE | 03/30/1999 | 5889529 |
| US | SYSTEM AND METHOD FOR ALLOWING A PERFORMER TO CONTROL AND INTERACT WITH AN ON-STAGE DISPLAY DEVICE | 08/04/1998 | 5790124 |
| US | PROCEDURE AND SYSTEM FOR PLACEMENT OPTIMIZATION OF CELLS WITHIN CIRCUIT BLOCKS BY OPTIMIZING PLACEMENT OF INPUT/OUTPUT PORTS WITHIN AN INTEGRATED CIRCUIT DESIGN | 05/26/1998 | 5757658 |
| US | OUTPUT PIN FOR SELECTIVELY OUTPUTTING ONE OF A PLURALITY OF SIGNALS INTERNAL TO A SEMICONDUCTOR CHIP ACCORDING TO A PROGRAMMABLE REGISTER FOR DIAGNOSTICS | 02/10/1998 | 5717695 |
| US | A METHOD TO PIPELINE WRITE MISSES IN SHARED CACHE MULTIPROCESSOR SYSTEMS | 02/23/1999 | 5875468 |
| US | READILY REMOVABLE HEAT SINK ASSEMBLY | 09/02/1997 | 5662163 |
| US | APPARATUS AND METHOD FOR DETERMINING THE SPEED OF A SEMICONDUCTOR CHIP | 10/06/1998 | 5818250 |
| US | SCAN CHAIN FOR SHIFTING THE STATE OF A PROCESSOR INTO MEMORY AT A SPECIFIED POINT DURING SYSTEM OPERATION FOR TESTING PURPOSES | 09/23/1997 | 5671235 |
| US | SYSTEM AND METHOD FOR AN ICONIC DRAG AND DROP INTERFACE FOR ELECTRONIC FILE TRANSFER | 09/01/1998 | 5801700 |
| US | SCA DRIVE SLED ASSEMBLY | 08/05/1997 | 5654873 |
| US | METHOD FOR SEEDING A PSEUDO-RANDOM NUMBER GENERATOR WITH A CRYPTOGRAPHIC HASH OF A DIGITIZATION OF A CHAOTIC SYSTEM | 03/24/1998 | 5732138 |
| US | HIGH PERFORMANCE SPIRAL HEAT SINK | 08/26/1997 | 5661638 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 12/18/2001 | 6331856 |
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 01/29/2002 | 6342892 |
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 07/15/2003 | 6593929 |
| US | RESTORATION FILTER FOR TRUNCATED PIXELS | 12/16/1997 | 5699079 |
| EP | SYSTEM AND METHOD FOR MERGING PIXEL FRAGMENTS BASED ON DEPTH RANGE VALUES | 03/31/2004 | EP 775982 |
| US | SYSTEM AND METHOD FOR MERGING PIXEL FRAGMENTS BASED ON DEPTH RANGE VALUES | 12/29/1998 | 5854631 |
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 12/26/2000 | 6166748 |
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 05/29/2001 | 6239810 |
| US | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 04/29/2003 | 6556197 |
| US | DATABASE-INDEPENDENT, SCALABLE, OBJECT-ORIENTED ARCHITECTURE AND API FOR MANAGING DIGITAL MULTIMEDIA ASSETS | 01/30/2001 | 6181336 |
| US | DATABASE-INDEPENDENT, SCALABLE, OBJECT-ORIENTED ARCHITECTURE AND API FOR MANAGING DIGITAL MULTIMEDIA ASSETS | 11/25/2003 | 6654029 |
| US | COLLABORATIVE WORK ENVIRONMENT SUPPORTING THREE-DIMENSIONAL OBJECTS AND MULTIPLE, REMOTE PARTICIPANTS | 10/13/1998 | 5821925 |
| US | COLLABORATIVE WORK ENVIRONMENT SUPPORTING THREE-DIMENSIONAL OBJECTS AND MULTIPLE, REMOTE PARTICIPANTS | 04/17/2001 | 6219057 |
| US | HEAT SINK WITH INTEGRAL ATTACHMENT MECHANISM | 04/07/1998 | 5735340 |
| US | SYSTEM AND METHOD TO EFFICIENTLY REPRESENT ALIASES AND INDIRECT MEMORY OPERATIONS IN STATIC SINGLE ASSIGNMENT FORM DURING COMPILATION | 06/16/1998 | 5768596 |
| US | SYSTEM AND METHOD TO EFFICIENTLY REPRESENT ALIASES AND INDIRECT MEMORY OPERATIONS IN STATIC SINGLE ASSIGNMENT FORM DURING COMPILATION | 10/10/2000 | 6131189 |
| US | A METHOD FOR SELECTING A THREE-DIMENSIONAL OBJECT FROM A GRAPHICAL USER INTERFACE | 12/02/1997 | 5694532 |
| US | APPARATUS AND METHOD FOR DYNAMIC CENTRAL PROCESSING UNIT CLOCK ADJUSTMENT | 06/30/1998 | 5774704 |
| US | SYSTEM AND METHOD FOR FINDING PREEMPTED THREADS IN A MULTI-THREADED APPLICATION | 07/09/2002 | 6418460 |
| US | BGA LAND PATTERN | 07/18/2000 | 6091155 |
| US | SYSTEM AND METHOD FOR BUFFERING MULTIPLE FRAMES WHILE CONTROLLING LATENCY | 08/03/1999 | 5933155 |
| US | SYSTEM AND METHOD FOR BUFFERING MULTIPLE FRAMES WHILE CONTROLLING LATENCY | 06/13/2000 | 6075543 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | BULK HEAD GASKET ASSEMBLY | 06/23/1998 | 5770822 |
| US | COMPUTER-RELATED METHOD, SYSTEM AND PROGRAM PRODUCT FOR CONTROLLING DATA VISUALIZATION IN EXTERNAL DIMENSIONS(S) | 11/12/2002 | 6480194 |
| US | COMPUTER-RELATED METHOD AND SYSTEM FOR CONTROLLING DATA VISUALIZATION IN EXTERNAL DIMENSION(S) | 01/11/2005 | 6842176 |
| US | MECHANISM FOR NON-LINEAR BROWSING OF DIVERSE INFORMATION SOURCES | 11/10/1998 | 5835092 |
| US | AN APPARATUS AND METHOD FOR COMPILER IDENTIFICATION OF ADDRESS DATA | 05/09/2000 | 6059839 |
| US | SYSTEM AND METHOD FOR CONSTANT PROPAGATION CLONING FOR UNKNOWN EDGES IN IPA | 09/22/1998 | 5812855 |
| US | INTER-PROCEDURAL ANALYSIS USER INTERFACE | 07/07/1998 | 5778212 |
| US | COMPILER HAVING AUTOMATIC COMMON BLOCKS OF MEMORY SPLITTING | 12/08/1998 | 5848275 |
| US | METHOD FOR SELECTING OPTIMAL PARAMETERS FOR COMPILING SOURCE CODE | 05/01/2001 | 6226790 |
| US | METHOD FOR UNROLLING TWO-DEEP LOOPS WITH CONVEX BOUNDS AND IMPERFECTLY NESTED CODE, AND FOR UNROLLING ARBITRARILY DEEP NESTS WITH CONSTANT BOUNDS AND IMPERFECTLY NESTED CODE | 05/20/2003 | 6567976 |
| US | METHOD AND APPARATUS FOR EXTRACTION OF PROGRAM REGION | 06/20/2000 | 6077311 |
| US | DISK DRIVE LOADING MECHANISM | 08/04/1998 | 5790373 |
| US | COMPACT COMPUTER HOUSING (AMENDED) | 06/16/1998 | D395286 |
| AU | COMPACT COMPUTER HOUSING (AMENDED) | 05/29/1998 | 746084(TM) |
| FR | COMPACT COMPUTER HOUSING (AMENDED) | 08/06/1997 | 974651 |
| GB | COMPACT COMPUTER HOUSING (AMENDED) | 09/07/1998 | 2068117 |
| DE | COMPACT COMPUTER HOUSING (AMENDED) | 11/07/1997 | 39753266 TM |
| US | PROGRAMMABLE PACKER AND UNPACKER WITH DITHERER | 05/16/2000 | 6065084 |
| US | BROWSER DRIVEN USER INTERFACE TO A MEDIA ASSET DATABASE | 04/06/1999 | 5893110 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM FOR VISUALLY APPROXIMATING SCATTERED DATA | 01/19/1999 | 5861891 |
| US | INTERPOLATION BETWEEN RELATIONAL TABLES FOR PURPOSES OF ANIMATING A DATA VISUALIZATION | 03/07/2000 | 6034697 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VISUALLY APPROXIMATING SCATTERED DATA USING COLOR TO REPRESENT VALUES OF A CATEGORICAL VARIABLE | 04/16/2002 | 6373483 |
| US | A TECHNIQUE FOR GUARANTEEING COMPLETION TIMES FOR BATCH JOBS WITHOUT STATIC PARTITIONING OF A MACHINE | 03/05/2002 | 6353844 |
| US | RESILIENT PANEL FOR HOUSING A MACHINE | 04/27/1999 | 5897180 |
| US | CABLE MANAGEMENT SYSTEM FOR A COMPUTER | 09/28/1999 | 5957556 |
| US | INSTRUCTION METHODS FOR PERFORMING DATA FORMATTING WHILE MOVING DATA BETWEEN MEMORY AND A VECTOR REGISTER FILE | 09/22/1998 | 5812147 |
| EP | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 04/02/2003 | 925687 |
| FR | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 04/02/2003 | 925687 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| GB | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 04/02/2003 | 925687 |
| US | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 06/16/1998 | 5768445 |
| DE | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 04/02/2003 | 69720477.4 |
| US | CIRCUIT TO SEPARATE AND COMBINE COLOR SPACE COMPONENT DATA OF A VIDEO IMAGE | 11/10/1998 | 5835729 |
| US | DIRECT MEMORY ACCESS APPARATUS FOR TRANSFERRING A BLOCK OF DATA HAVING DISCONTINUOUS ADDRESSES USING AN ADDRESS CALCULATING CIRCUIT | 08/22/2000 | 6108722 |
| US | A METHOD AND SYSTEM FOR AN EFFICIENT USER MODE CACHE MANIPULATION USING A SIMULATED INSTRUCTION | 04/11/2000 | 6049866 |
| US | METHOD AND APPARATUS FOR ADDRESS SPACE TRANSLATION USING A TLB | 09/29/1998 | 5815686 |
| US | PACKET SWITCHED ROUTER ARCHITECTURE FOR PROVIDING MULTIPLE SIMULTANEOUS COMMUNICATIONS | 01/27/2004 | 6683876 |
| US | GUARANTEED BANDWIDTH ALLOCATION METHOD IN A COMPUTER SYSTEM FOR INPUT/OUTPUT DATA TRANSFERS | 07/21/1998 | 5784569 |
| US | PACKETIZED DATA TRANSMISSIONS IN A SWITCHED ROUTER ARCHITECTURE | 08/28/2001 | 6282195 |
| US | PACKETIZED DATA TRANSMISSIONS IN A SWITCHED ROUTER ARCHITECTURE | 01/10/2006 | 6985484 |
| US | HIGH BANDWIDTH PCI TO PACKET SWITCHED ROUTER BRIDGE HAVING MINIMIZED MEMORY LATENCY | 06/22/1999 | 5915104 |
| US | SYNCHRONIZATION INFRASTRUCTURE FOR USE IN A COMPUTER SYSTEM | 06/09/1998 | 5764965 |
| US | COMPRESSION CONNECTOR | 03/24/1998 | 5730605 |
| US | LOADING AND PLACEMENT DEVICE FOR CONNECTING CIRCUIT BOARDS | 12/15/1998 | 5848906 |
| US | COMPACT COMPUTER HOUSING (DESIGN) | 08/04/1998 | D396698 |
| DE | COMPACT COMPUTER HOUSING (DESIGN) | 10/15/1997 | M9706956.6 |
| CN | COMPACT COMPUTER HOUSING (DESIGN) | 11/07/1998 | 104956 |
| AU | COMPACT COMPUTER HOUSING (DESIGN) | 09/21/1998 | 135088 |
| FR | COMPACT COMPUTER HOUSING (DESIGN) | 07/21/1997 | 974237 |
| GB | COMPACT COMPUTER HOUSING (DESIGN) | 01/14/1998 | 2067607 |
| US | METHOD AND SYSTEM FOR SIMULTANEOUS HIGH BANDWIDTH INPUT OUTPUT | 11/23/1999 | 5991824 |
| US | A METHOD AND APPARATUS FOR INTERACTIVELY SELECTING AMONG THREE-DIMENSIONAL ON-SCREEN OBJECTS | 11/09/1999 | 5982382 |
| US | METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR VISUALIZING AN EVIDENCE CLASSIFIER | 07/27/1999 | 5930803 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VISUALIZING AN EVIDENCE CLASSIFIER | 10/01/2002 | 6460049 |
| US | DISTRIBUTED SCHEDULING OF PARALLEL JOBS WITH NO KERNEL-TO-KERNEL COMMUNICATION | 07/20/2004 | 6766515 |
| US | EARNINGS-BASED TIME-SHARE SCHEDULING | 03/30/2004 | 6714960 |
| US | ADAPTIVE FREQUENCY SYNTHESIZER WITH SYNCHRONIZATION | 05/23/2000 | 6067411 |
| US | SYSTEM AND METHOD FOR INDEPENDENTLY CONFIGURING INTERNATIONAL LOCATION AND LANGUAGE | 06/06/2000 | 6073090 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | SYSTEM FOR COMMUNICATIONS WHERE FIRST PRIORITY DATA TRANSFER IS NOT DISTURBED BY SECOND PRIORITY DATA TRANSFER AND WHERE ALLOCATED BANDWIDTH IS REMOVED WHEN PROCESS TERMINATES ABNORMALLY | 06/01/1999 | 5909594 |
| US | SYSTEM FOR COMMUNICATIONS WHERE FIRST PRIORITY DATA TRANSFER IS NOT DISTURBED BY SECOND PRIORITY DATA TRANSFER AND WHERE ALLOCATED BANDWIDTH IS REMOVED WHEN PROCESS TERMINATES ABNORMALLY | 06/03/2003 | RE38134 |
| US | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 04/07/1998 | D393249 |
| DE | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 03/24/1997 | M9702994.7 |
| IT | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 02/13/2002 | 73445 |
| FR | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 08/08/1997 | 971719 |
| JP | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 01/25/2002 | 1136233 |
| GB | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 09/23/1996 | 2064454 |
| CN | HOUSING FOR DESKSIDE COMPUTER OR THE LIKE | 03/19/1998 | 97311011.2 |
| US | LOW-LATENCY REAL-TIME DISPATCHING IN GENERAL PURPOSE MULTIPROCESSOR SYSTEMS | 07/27/1999 | 5928322 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR DYNAMICALLY ALLOCATING LARGE MEMORY PAGES OF DIFFERENT SIZES | 01/30/2001 | 6182089 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VIRTUAL MEMORY SUPPORT FOR MANAGING TRANSLATION LOOK-ASIDE BUFFERS WITH MULTIPLE PAGE SIZE SUPPORT | 08/29/2000 | 6112285 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR MANAGING MEMORY IN A NON-UNIFORM MEMORY ACCESS SYSTEM | 09/11/2001 | 6289424 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR MANAGING MEMORY IN A NON-UNIFORM MEMORY ACCESS SYSTEM | 01/01/2002 | 6336177 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR PAGE SHARING BETWEEN FAULT-ISOLATED CELLS IN A DISTRIBUTED SHARED MEMORY SYSTEM | 11/14/2000 | 6148379 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR ORGANIZING PAGE CACHES | 09/05/2000 | 6115790 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR DYNAMICALLY SIZING HASH TABLES | 09/28/1999 | 5960434 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR ALLOCATING PHYSICAL MEMORY IN A DISTRIBUTED SHARED MEMORY NETWORK | 06/19/2001 | 6249802 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR PROFILING THREAD VIRTUAL MEMORY ACCESS | 10/26/1999 | 5974536 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VISUALIZING A DECISION-TREE CLASSIFIER | 08/21/2001 | 6278464 |
| US | REVERSE MAPPING PAGE FRAME DATA STRUCTURES TO PAGE TABLE ENTRIES | 08/29/2000 | 6112286 |
| US | POWER SWITCH PLUNGER MECHANISM | 10/06/1998 | 5817997 |
| US | ROTARY LATCH ASSEMBLY FOR A COMPUTER HOUSING | 10/27/1998 | 5826922 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR PARTIAL REDUNDANCY ELIMINATION BASED ON STATIC SINGLE ASSIGNMENT FORM DURING COMPILATION | 02/15/2000 | 6026241 |
| US | BAYES RULE BASED AND DECISION TREE HYBRID CLASSIFIER | 01/30/2001 | 6182058 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | SYSTEM AND METHOD FOR SELECTION OF IMPORTANT ATTRIBUTES | 02/15/2000 | 6026399 |
| US | HOUSING FOR A COMPUTER | 04/14/1998 | D393449 |
| DE | HOUSING FOR A COMPUTER | 03/27/1997 | M9703109.7 |
| IT | HOUSING FOR A COMPUTER | 02/13/2002 | 73450 |
| IN | HOUSING FOR A COMPUTER | 09/23/1997 | 173463 |
| FR | HOUSING FOR A COMPUTER | 08/22/1997 | 971844 |
| JP | HOUSING FOR A COMPUTER | 01/11/2002 | 1135316 |
| GB | HOUSING FOR A COMPUTER | 09/27/1996 | 2064556 |
| CN | HOUSING FOR A COMPUTER | 08/07/1999 | 97311141 |
| US | LIGHT BAR AND REFLECTOR ASSEMBLY | 01/19/1999 | 5861815 |
| US | SYSTEM AND METHOD FOR SCHEDULING AN EVENT SUBJECT TO THE AVAILABILITY OF REQUESTED PARTICIPANTS | 10/05/1999 | 5963913 |
| US | NETWORK REQUEST DISTRIBUTION BASED ON STATIC RULES AND DYNAMIC PERFORMANCE DATA | 01/09/2001 | 6173322 |
| US | ELECTROMAGNETIC INTERFERENCE SHIELDING ENCLOSURE AND HEAT SINK WITH COMPRESSION COUPLING MECHANISM | 03/09/1999 | 5880930 |
| US | SYSTEM AND METHOD FOR AUTOMATICALLY CREATING A DESKTOP ICON FOR ACCESS TO A REMOTE RESOURCE | 03/09/1999 | 5880730 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR PAGE REPLICATION IN A NON-UNIFORM MEMORY ACCESS SYSTEM | 12/26/2000 | 6167437 |
| US | CIRCUIT FOR FILTERING A POWER SUPPLY FOR NOISE SENSITIVE DEVICES | 10/20/1998 | 5825238 |
| US | METHOD AND SYSTEM FOR DECODING DATA ENCODED IN A VARIABLE LENGTH CODE WORD | 04/17/2001 | 6219457 |
| US | IMPROVED HOT-PLUG POWER SUPPLY FOR HIGH-AVAILABILITY COMPUTER SYSTEMS | 03/28/2000 | 6044424 |
| US | RESUMPTION OF A PREEMPTED NON-PRIVILEGED THREAD WITH NO KERNEL INTERVENTION | 02/16/1999 | 5872963 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR COMPUTING HISTOGRAM AGGREGATIONS | 09/28/1999 | 5960435 |
| US | CROSSBAR SWITCH WITH COMMUNICATION RING BUS | 04/27/2004 | 6728206 |
| US | SYSTEM AND METHOD FOR MAINTAINING TRANSLATION LOOK-ASIDE BUFFER (TLB) CONSISTENCY | 08/15/2000 | 6105113 |
| US | LATCHING ASSEMBLY FOR A COMPUTER | 06/01/1999 | 5907962 |
| US | SLIDING DOOR ASSEMBLY FOR A COMPUTER HOUSING | 07/20/1999 | 5924780 |
| US | METHOD AND SYSTEM FOR PERFORMING FLOATING POINT OPERATIONS IN UNNORMALIZED FORMAT USING A FLOATING POINT ACCUMULATOR | 07/03/2001 | 6256655 |
| US | MEDIA CO-PROCESSOR WITH GRAPHICS, VIDEO AND AUDIO TASKS PARTITIONED BY TIME DIVISION MULTIPLEXING | 08/14/2001 | 6275239 |
| US | METHOD AND SYSTEM FOR DESKEWING PARALLEL BUS CHANNELS | 02/29/2000 | 6031847 |
| US | ACOUSTIC PERSPECTIVE IN A VIRTUAL THREE-DIMENSIONAL ENVIRONMENT | 12/11/2001 | 6330486 |
| US | MODULAR CARD CAGE WITH CONNECTION MECHANISM | 01/09/2001 | 6171120 |
| US | SYSTEM AND METHOD FOR CODING COLORS AND STORING COMPENSATION FACTORS USED IN COLOR SPACE CONVERSION | 11/30/1999 | 5995655 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | DISTRIBUTED CONTROL AND SYNCHRONIZATION OF MULTIPLE DATA PROCESSORS USING FLEXIBLE COMMAND QUEUES | 04/25/2000 | 6055579 |
| US | METHOD AND SYSTEM FOR EFFICIENT CONTEXT SWITCHING IN A COMPUTER GRAPHICS SYSTEM | 03/27/2001 | 6208361 |
| US | A VIDEO FRAME DETECTOR READILY ADAPTABLE TO VIDEO SIGNAL FORMATS WITHOUT MANUAL PROGRAMMING AND METHOD FOR SAME | 12/12/2000 | 6160589 |
| DE | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 12/18/2002 | DE69904579 |
| EP | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 12/18/2002 | 1070301 |
| FR | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 12/18/2002 | 1070301 B1 |
| GB | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 12/18/2002 | 1070301 |
| US | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 06/10/2003 | 6578197 |
| US | HASHED DIRECT-MAPPED TEXTURE CACHE | 05/15/2001 | 6233647 |
| US | MULTIPLE LIGHT SOURCE COLOR BALANCING SYSTEM WITHIN A LIQUID CRYSTAL FLAT PANEL DISPLAY | 04/02/2002 | 6366270 |
| US | MULTIPLE LIGHT SOURCE COLOR BALANCING SYSTEM WITHIN A LIQUID CRYSTAL FLAT PANEL DISPLAY | 03/18/2003 | 6535190 |
| US | INTEGRAL ACTUATOR FOR A PRINTED CIRCUIT BOARD | 10/19/1999 | 5967825 |
| US | LIQUID CRYSTAL FLAT PANEL DISPLAY WITH ENHANCED BACKLIGHT BRIGHTNESS AND SPECIALLY SELECTED LIGHT SOURCES | 06/05/2001 | 6243068 |
| US | LIQUID CRYSTAL FLAT PANEL DISPLAY WITH ENHANCED BACKLIGHT BRIGHTNESS AND SPECIALLY SELECTED LIGHT SOURCES | 09/10/2002 | 6448955 |
| US | LIQUID CRYSTAL FLAT PANEL DISPLAY WITH ENHANCED BACKLIGHT BRIGHTNESS AND SPECIALLY SELECTED LIGHT SOURCES | 12/02/2003 | 6657607 |
| US | INTERCONNECT CAPACITIVE EFFECTS ESTIMATION | 11/06/2001 | 6314546 |
| US | EXCHANGING MESSAGES BETWEEN COMPUTER SYSTEMS COMMUNICATIVELY COUPLED IN A COMPUTER SYSTEM NETWORK | 07/20/2004 | 6766358 |
| US | METHOD AND SYSTEM FOR CLOCK CYCLE MEASUREMENT AND DELAY OFFSET | 01/20/2004 | 6680636 |
| US | AN INPUT/OUTPUT DEVICE MANAGED TIMER PROCESS | 07/15/2003 | 6594787 |
| US | DISPLAY SYSTEM HAVING FLOATING POINT RASTERIZATION AND FLOATING POINT FRAME BUFFERING | 11/18/2003 | 6650327 |
| US | APPARATUS AND METHOD FOR UTILIZING MULTIPLE RENDERING PIPES FOR A SINGLE 3-D DISPLAY | 09/18/2001 | 6292200 |
| DK | ROUTER TABLE LOOKUP MECHANISM | | 69804131.8 |
| US | ROUTER TABLE LOOKUP MECHANISM | 10/19/1999 | 5970232 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE | 10/14/2003 | 6633958 |
| US | SYSTEM AND METHOD FOR FAST BARRIER SYCHRONIZATION | 04/10/2001 | 6216174 |
| US | METHOD AND APPARATUS FOR PROCESSING A SET OF DATA VALUES WITH PULRAL PROCESSING UNITS USING MASK BITS GENERATED BY OTHER PROCESSING UNITS | 10/23/2001 | 6308250 |
| US | ELECTRICALLY CONDUCTIVE PATH THROUGH A DIELECTRIC MATERIAL | 04/01/2003 | 6541853 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR PERFORMING REGISTER PROMOTION VIA LOAD AND STORE PLACEMENT OPTIMIZATION WITHIN AN OPTIMIZING COMPILER | 10/03/2000 | 6128775 |
| US | QUANTUM ACCELERATION OF CONVENTIONAL NON-QUANTUM COMPUTERS | 06/27/2000 | 6081882 |
| US | METHOD SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VISUALIZING A DATA STRUCTURE | 10/09/2001 | 6301579 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR USING STATIC SINGLE ASSIGNMENT FORM AS A PROGRAM REPRESENTATION AND A MEDIUM FOR PERFORMING GLOBAL SCALAR OPTIMIZATION | 10/09/2001 | 6301704 |
| US | METHOD AND APPARATUS FOR COMPRESSING AND UNCOMPRESSING IMAGE DATA | 06/06/2006 | 7058218 |
| US | METHOD AND APPARATUS FOR BROADCASTING INVALIDATION MESSAGES IN A COMPUTER SYSTEM | 07/16/2002 | 6421712 |
| US | MEMORY SYSTEM WITH MULTIPLE ADDRESSING AND CONTROL BUSSES | 02/09/1999 | 5870325 |
| US | MEMORY SYSTEM WITH ADDRESSING AND CONTROL BUSSES | 06/20/2000 | 6078515 |
| US | SCAN INTERFACE CHIP (SIC) SYSTEM AND METHOD FOR SCAN TESTING ELECTRONIC SYSTEMS | 07/06/2004 | 6760876 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR EXTENDING SPARSE PARTIAL REDUNDANCY ELIMINATION TO SUPPORT SPECULATIVE CODE MOTION WITHIN AN OPTIMIZING COMPILER | 11/21/2000 | 6151706 |
| US | ENHANCED GRAPHICS CACHE MEMORY | 01/28/2003 | 6513099 |
| US | METHOD AND DEVICE FOR CONTROLLING ACCESS TO MEMORY | 05/21/2002 | 6393533 |
| US | LARGE AREA WIDE ASPECT RATIO FLAT PANEL MONITOR HAVING HIGH RESOLUTION FOR HIGH INFORMATION CONTENT DISPLAY | 11/09/2004 | 6816145 |
| US | METHOD AND SYSTEM FOR EFFICIENT EDGE BLENDING IN HIGH FIDELITY MULTICHANNEL COMPUTER GRAPHICS DISPLAYS | 04/08/2003 | 6545685 |
| US | DISPLAY ASSEMBLY OR SIMILAR ARTICLE (DESIGN) | 01/18/2000 | D419141 |
| JP | DISPLAY ASSEMBLY OR SIMILAR ARTICLE (DESIGN) | 10/27/2000 | 1095736 |
| US | FLAT PANEL DISPLAY AND STAND WITH VERTICAL ADJUSTMENT AND TILT ADJUSTMENT | 05/09/2000 | 6061104 |
| US | SYSTEM AND METHOD FOR PROVIDING A WIDE ASPECT RATIO FLAT PANEL DISPLAY MONITOR INDEPENDENT WHITE-BALANCE | 08/26/2003 | 6611249 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD AND APPARATUS FOR REPRESENTING, MANIPULATING AND RENDERING SOLID SHAPES USING VOLUMETRIC PRIMITIVES | 07/29/2003 | 6600487 |
| US | METHOD AND SYSTEM FOR HYBRID MAPPING OF OBJECTS INTO A RELATIONAL DATA BASE TO PROVIDE HIGH-SPEED PERFORMANCE AND UPDATE FLEXIBILITY | 09/02/2003 | 6615204 |
| US | COMPUTER HOUSING | 09/26/2000 | D431242 |
| FR | COMPUTER HOUSING | 09/01/2000 | 591467/475 |
| AU | COMPUTER HOUSING | 04/20/2000 | 140491 |
| GB | COMPUTER HOUSING | 08/18/1999 | 2083735 |
| DE | COMPUTER HOUSING | 06/02/1999 | 49905366.4 |
| US | COMPUTER HOUSING OR SIMILAR ARTICLE (DESIGN) | 11/30/1999 | D417203 |
| FR | COMPUTER HOUSING OR SIMILAR ARTICLE (DESIGN) | 09/17/1999 | 555348 |
| JP | COMPUTER HOUSING OR SIMILAR ARTICLE (DESIGN) | 06/30/2000 | 1084129 |
| GB | COMPUTER HOUSING OR SIMILAR ARTICLE (DESIGN) | 08/10/1999 | 2082932 |
| DE | COMPUTER HOUSING OR SIMILAR ARTICLE (DESIGN) | 09/21/1999 | 49904122.4 |
| US | METHOD FOR MODELING AND UPDATING A COLORIMETRIC REFERENCE PROFILE FOR A FLAT PANEL DISPLAY | 05/06/2003 | 6559826 |
| US | METHOD FOR EFFICIENT TRANSLATION OF MEMORY ADDRESSES IN COMPUTER SYSTEMS | 04/24/2001 | 6223270 |
| US | ADVANCED BOOT SEQUENCE FOR AN X86 COMPUTER SYSTEM THAT MAINTAINS EXPANSION CARD DEVICE COMPATIBILITY | 10/03/2000 | 6128731 |
| US | DESIGN FOR CIRCUIT BOARD ORTHOGONAL INSTALLATION AND REMOVAL | 07/03/2001 | 6256196 |
| US | ADVANCED FIRMWARE BOOT SEQUENCE X86 COMPUTER SYSTEM THAT MAINTAINS LEGACY HARDWARE AND SOFTWARE COMPATIBILIRTY | 03/12/2002 | 6357003 |
| US | MEMORY SYSTEM WITH SWITCHING FOR DATA ISOLATION | 09/05/2000 | 6115278 |
| US | MEMORY SYSTEM WITH SWITCHING FOR DATA ISOLATION | 04/10/2001 | 6215686 |
| US | DOOR ASSEMBLY FOR A COMPUTER | 10/17/2000 | 6132019 |
| US | COLOR CALIBRATION DEVICE FOR A DISPLAY (DESIGN) | 01/25/2000 | D419465 |
| FR | COLOR CALIBRATION DEVICE FOR A DISPLAY (DESIGN) | 08/25/1999 | 995251 |
| JP | COLOR CALIBRATION DEVICE FOR A DISPLAY (DESIGN) | 10/20/2000 | 1094490 |
| GB | COLOR CALIBRATION DEVICE FOR A DISPLAY (DESIGN) | 09/08/1999 | 2084674 |
| DE | COLOR CALIBRATION DEVICE FOR A DISPLAY (DESIGN) | 10/21/1999 | 49906462.3 |
| US | METHOD FOR MANAGING CONCURRENT ACCESS TO VIRTUAL MEMORY DATA STRUCTURES | 12/17/2002 | 6496909 |
| US | SYSTEM AND METHOD FOR COOLING ELECTRONIC COMPONENTS | 04/02/2002 | 6366461 |
| US | NOISE ESTIMATION FOR COUPLED RC INTERCONNECTS IN DEEP-SUBMICRON INTEGRATED CIRCUITS | 05/04/2004 | 6732065 |
| US | MEMORY SYSTEM INCLUDING GUIDES THAT RECEIVE MEMORY MODULES | 10/07/2003 | 6629855 |
| US | ABSTRACT VERIFICATION ENVIRONMENT | 02/15/2005 | 6856950 |
| US | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | 11/18/2003 | 6651157 |
| US | METERED FORCE SINGLE POINT HEATSINK ATTACH MECHANISM | 01/02/2001 | 6169659 |
| US | MULTITHREADED LAYERED-CODE PROCESSOR | 07/27/2004 | 6769122 |
| US | SYNCHRONIZATION OF HARDWARE SIMULATION PROCESSES | | 6879948 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | EFFICIENT MEMORY STRUCTURE SIMULATION FOR SEQUENTIAL CIRCUIT DESIGN VERIFICATION | 11/02/2004 | 6813599 |
| US | A CIRCUIT DESIGN FOR HIGH-SPEED DIGITAL COMMUNICATION | 08/10/2004 | 6775339 |
| US | CABLE DOCK FIXTURE WITH EMI SHIELDING | 08/28/2001 | 6280257 |
| US | SYSTEM AND METHOD TO PROVIDE POWER TO A SEA OF GATES STANDARD CELL BLOCK AN OVERHEAD BUMP GRID | 08/28/2001 | 6281108 |
| US | SCAN INTERFACE CHIP (SIC) SYSTEM AND METHOD FOR SCAN TESTING ELECTRONIC SYSTEMS | 06/22/2004 | 6754863 |
| US | SCAN INTERFACE CHIP (SIC) SYSTEM AND METHOD FOR SCAN TESTING ELECTRONIC SYSTEMS | 11/02/2004 | 6813739 |
| US | OPTIMIZING REPEATERS POSITIONING ALONG INTERCONNECTS | 05/14/2002 | 6389581 |
| US | A PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT | 07/09/2002 | 6417713 |
| US | A PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT | 10/12/2004 | 6803872 |
| US | A PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT | 11/26/2002 | 6486723 |
| US | METHOD AND COMPUTER PROGRAM PRODUCT FOR GLOBAL MINIMIZATION OF SIGN-EXTENSION AND ZERO-EXTENSION OPERATIONS | 05/27/2003 | 6571387 |
| US | MODELING AND FABRICATION OF OBJECTS REPRESENTED AS DEVELOPABLE SURFACES | 12/10/2002 | 6493603 |
| US | REMOTE ADDRESS TRANSLATION IN A MULTIPROCESSOR SYSTEM | 08/02/2005 | 6925547 |
| US | FLAT PANEL DISPLAY SCREEN WITH PROGRAMMABLE GAMMA FUNCTIONALITY | 03/19/2002 | 6359389 |
| US | SYSTEM AND METHOD FOR MAINTAINING AND RECOVERING DATA CONSISTENCY ACROSS MULTIPLE INSTANCES OF A DATABASE | 06/15/2004 | 6751636 |
| US | A SYSTEM AND METHOD FOR MAINTAINING AND RECOVERING DATA CONSISTENCY IN A DATA BASE PAGE | 01/31/2006 | 6993523 |
| US | SYSTEM AND METHOD FOR MAINTAINING AND RECOVERING DATA CONSISTENCY ACROSS MULTIPLE PAGES | 04/13/2004 | 6721739 |
| US | BEZEL FOR A COMPUTER | 08/08/2000 | D429248 |
| US | DETERMINING A WORST CASE SWITCHING FACTOR FOR INTEGRATED CIRCUIT DESIGN | 03/05/2002 | 6353917 |
| US | METHOD AND APPARATUS FOR PREPARING A PERSPECTIVE VIEW OF AN APPROXIMATELY SPHERICAL SURFACE PORTION | 11/05/2002 | 6476813 |
| US | METHOD AND APPARATUS FOR PREPARING A PERSPECTIVE VIEW OF AN APPROXIMATELY SPHERICAL SURFACE PORTION | 09/09/2003 | 6618049 |
| US | METHOD AND APPARATUS FOR ANALYZING BUFFER ALLOCATION TO A DEVICE ON A PERIPHERAL COMPONENT INTERCONNECT BUS | 05/28/2002 | 6397274 |
| US | MODULAR INPUT/OUTPUT CONTROLLER CAPABLE OF ROUTING PACKETS OVER BUSSES OPERATING AT DIFFERENT SPEEDS | 04/22/2003 | 6553446 |
| US | TRANSLATION OF PCI LEVEL INTERRUPTS INTO PACKET BASED MESSAGES FOR EDGE EVENT DRIVE MICROPROCESSORS | 08/05/2003 | 6604161 |
| US | TRANSFER ATTRIBUTE ENCODING WITHIN AN ADDRESS ON A BUS | 03/23/2004 | 6711636 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | UPSTREAM SITUATED APPARATUS AND METHOD FOR PROVIDING HIGH BANDWIDTH DATA FLOW CONTROL TO AN INPUT/OUTPUT UNIT | 09/16/2003 | 6622182 |
| US | SYSTEM AND METHOD FOR A HIERARCHICAL SYSTEM MANAGEMENT ARCHITECTURE OF A HIGHLY SCALABLE COMPUTING SYSTEM | 01/18/2005 | 6845410 |
| US | SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL | 04/18/2006 | 7031420 |
| US | DIAGNOSTIC SYSTEM AND METHOD FOR A HIGHLY SCALABLE COMPUTING SYSTEM | 07/29/2003 | 6601183 |
| US | COMPUTER MODULE MOUNTING SYSTEM AND METHOD | 09/17/2002 | 6452805 |
| US | METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM | 01/15/2002 | 6339812 |
| US | METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM | 06/10/2003 | 6578115 |
| US | MULTI-MODE DISPLAY | 03/07/2006 | 7009616 |
| US | METHOD AND APPARATUS FOR PREFETCHING INFORMATION AND STORING THE INFORMATION IN A STREAM BUFFER | 05/31/2005 | 6901500 |
| US | METHOD AND ASSEMBLY FOR INSTALLATION OR REMOVAL OF PRINTED CIRCUIT CARD | 12/17/2002 | 6496385 |
| US | FASTENERLESS CIRCUIT BOARD SUPPORT | 08/06/2002 | 6428352 |
| US | PANEL | 10/08/2002 | D464054 |
| US | PANEL | 10/29/2002 | D464973 |
| US | INDUSTRIAL RACK | 10/01/2002 | D463796 |
| US | PANEL GASKET | 11/19/2002 | 6483024 |
| US | PRINTED CIRCUIT BOARD CARRIER INSERTION/EXTRACTION ASSEMBLY | 02/27/2001 | 6193532 |
| US | MODULAR COMPUTING ARCHITECTURE HAVING COMMON COMMUNICATION INTERFACE | 12/07/2004 | 6829666 |
| US | PARTITIONING A DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER TO FACILITATE SELECTIVE HARDWARE MAINTENANCE | 02/04/2003 | 6516372 |
| EP | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 11/26/2003 | EP1222559 |
| DE | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 11/26/2003 | 1222559 |
| FR | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 11/26/2003 | 1222559 |
| GB | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 11/26/2003 | 1222559 |
| US | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 06/15/2004 | 6751698 |
| US | NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM | 12/06/2005 | 6973559 |
| US | MANAGEMENT AND SCHEDULING OF A DISTRIBUTED RENDERING METHOD AND SYSTEM | 06/13/2006 | 7062527 |
| US | MODULAR AIR MOVING SYSTEM AND METHOD | 06/18/2002 | 6406257 |
| US | SYSTEM AND METHOD FOR SHARED MEMORY PROTECTION IN A | 04/30/2002 | 6381681 |
| US | SYSTEM AND METHOD FOR MEMORY PAGE MIGRATION IN A MULTI-PROCESSOR COMPUTER | 09/17/2002 | 6453408 |
| US | SYSTEM AND METHOD FOR DISTRIBUTING OUTPUT QUEUE SPACE | 03/11/2003 | 6532501 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD AND APPARATUS FOR DECOUPLING PROCESSOR SPEED FROM MEMORY SUBSYSTEM SPEED IN A NODE CONTROLLER | 04/08/2003 | 6546451 |
| US | CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY | 08/21/2001 | 6279073 |
| EP | METHOD AND APPARATUS FOR PROCESSING ERRORS IN A COMPUTER SYSTEM | 07/10/2002 | 1221229 |
| US | METHOD AND APPARATUS FOR PROCESSING ERRORS IN A COMPUTER SYSTEM | 09/24/2002 | 6457146 |
| US | SYSTEM AND METHOD FOR MINIMIZING ERROR CORRECTION CODE BITS IN VARIABLE SIZED DATA FORMATS | 11/26/2002 | 6487685 |
| US | DATA SYNCHRONIZER FOR A MULTIPLE RATE CLOCK SOURCE AND METHOD THEREOF | 03/04/2003 | 6529570 |
| US | ELECTRICAL CONNECTOR WITH LATCHING BACKPLATE ASSEMBLY | 09/25/2001 | 6293813 |
| US | METHOD AND SYSTEM FOR HANDLING INTERRUPTS IN A NODE CONTROLLER WITHOUT ATTACHED PROCESSORS | 05/13/2003 | 6564277 |
| US | SYSTEM AND METHOD FOR DISPLAYING AN IMAGE USING DISPLAY DISTORTION CORRECTION | 11/16/2004 | 6819333 |
| US | ELECTRONIC DEVICE SUPPORT AND METHOD | 02/04/2003 | 6513770 |
| US | HOUSING GROUND BRACKET AND METHOD | 06/03/2003 | 6574121 |
| US | CABLE ORGANIZER AND METHOD | 08/20/2002 | 6438309 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING SCALABLE MULTI-READER/SINGLE-WRITER LOCKS | 07/29/2003 | 6601120 |
| US | IMAGE DATA COMPRESSION AND DECOMPRESSION | 01/27/2004 | 6683979 |
| US | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 06/27/2006 | 7068263 |
| US | METHOD AND SYSTEM FOR SECURE REMOTE DISTRIBUTED RENDERING | 08/15/2006 | 7092983 |
| US | CARRIER FOR COMPUTER PERIPHERAL DEVICE | 04/30/2002 | 6381139 |
| US | TRACE RECORDER ON-CHIP TRACE RECORDING | 02/28/2006 | 7007205 |
| US | DEVICE AND METHOD FOR STORING INFORMATION IN MEMORY | 05/18/2004 | 6738885 |
| US | CONDITIONING AND FILLING SYSTEM FOR A SPRAY EVAPORATIVE COOLING WORKING FLUID | 02/12/2002 | 6345515 |
| US | OPTIMIZE GLOBAL NET TIMING WITH REPEATER BUFFERS | 01/27/2004 | 6684373 |
| US | RADIAL COMPUTER SYSTEM | 01/30/2001 | D436950 |
| US | I/O IMPEDANCE CONTROLLER | 03/09/2004 | 6703908 |
| US | METHOD AND APPARATUS FOR RECORDING PROGRAM EXECUTION IN A MICROPROCESSOR BASED INTEGRATED CIRCUIT | 10/14/2003 | 6634011 |
| US | SERVER DOOR | 07/17/2001 | D445112 |
| US | DRIVE SLED DOOR | 07/24/2001 | D445425 |
| US | METHOD AND SYSTEM FOR CALCULATING INTERCONNECT MOMENTS AND DELAY | 03/11/2003 | 6532575 |
| US | COMMON USER INTERFACE DEVELOPMENT TOOLKIT | 11/29/2005 | 6971086 |
| US | CACHE LINE CONVERTER | 06/15/2004 | 6751705 |
| US | ****OWNED BY SGI JAPAN/TOSHIBA *** METHOD FOR DISPLAYING THREE-DIMENSIONAL OBJECTS AND A COMPUTER-READABLE STORAGE MEDIUM STORING A PROGRAM FOR ACHIEVING THE SAME | 01/27/2004 | 6683607 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD AND SYSTEM FOR ESTIMATING INTERCONNECT DELAY | 02/08/2005 | 6853969 |
| US | METHOD AND SYSTEM FOR ESTIMATING INTERCONNECT DELAY | 02/08/2005 | 6853969 |
| US | METHOD AND SYSTEM FOR DETERMINING REPEATER ALLOCATION REGIONS | 04/15/2003 | 6550048 |
| US | METHOD AND CACHE-COHERENCE SYSTEM ALLOWING PURGING OF MID-LEVEL CACHE ENTRIES WITHOUT PURGING LOWER-LEVEL CACHE ENTRIES | 01/20/2004 | 6681293 |
| US | GTL+ DRIVER | 03/08/2005 | 6864706 |
| US | GTL+ DRIVER | 02/03/2004 | 6686765 |
| US | GTL + ONE-ONE/ZERO-ZERO DETECTOR | 08/13/2002 | 6433627 |
| US | VARIABLE MODE BI-DIRECTIONAL AND UNI-DIRECTIONAL COMPUTER COMMUNICATION SYSTEM | 12/14/2004 | 6831924 |
| US | DUAL-BANK FIFO FOR SYNCHRONIZATION OF READ DATA IN DDR SDRAM | 07/19/2005 | 6920526 |
| US | DUAL- BANK FIFO FOR SYNCHRONIZATION OF READ DATA IN DDR SDRAM | 07/19/2005 | 6920526 |
| US | DISCRETE DELAY LINE SYSTEM AND METHOD | 02/11/2003 | 6518812 |
| US | SYNTHESIS WITH AUTOMATED PLACEMENT INFORMATION FEEDBACK | 03/02/2004 | 6701496 |
| US | MEMORY DEVICE STORING DATA AND DIRECTORY INFORMATION THEREON, AND METHOD FOR PROVIDING THE DIRECTORY INFORMATION AND THE DATA IN THE MEMORY DEVICE | 08/10/2004 | 6775742 |
| US | SYSTEM AND METHOD FOR MEMORY ARBITRATION | 11/09/2004 | 6816947 |
| US | METHOD AND APPARATUS FOR MANAGING NODE CONTROLLERS USING PARTITIONS IN A COMPUTER SYSTEM | 04/05/2005 | 6877029 |
| US | SYSTEM AND METHOD FOR REDUCING MEMORY LATENCY DURING READ REQUESTS | 01/13/2004 | 6678798 |
| US | METHOD AND SYSTEM FOR USING HIGH COUNT INVALIDATE ACKNOWLEDGEMENTS IN DISTRIBUTED SHARED MEMORY SYSTEMS | 04/06/2004 | 6718442 |
| US | SYSTEM AND METHOD FOR HANDLING UPDATES TO MEMORY IN A DISTRIBUTED SHARED MEMORY SYSTEMS | 07/05/2005 | 6915387 |
| US | METHOD AND SYSTEM FOR MANAGING DATA AT AN INPUT/OUTPUT INTERFACE FOR A MULTIPROCESSOR SYSTEM | 02/22/2005 | 6859863 |
| US | METHOD AND SYSTEM FOR MANAGING DATA AT AN INPUT/OUTPUT INTERFACE FOR A MULTIPROCESSOR SYSTEM | 02/22/2005 | 6859863 |
| US | METHOD AND SYSTEM FOR STORING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM | 09/21/2004 | 6795900 |
| US | METHOD AND SYSTEM FOR EFFICIENT USE OF A MULTI-DIMENSIONAL SHARING VECTOR IN A COMPUTER SYSTEM | 07/05/2005 | 6915388 |
| US | SYSTEM AND METHOD FOR TRANSFERRING OWNERSHIP OF DATA IN A DISTRIBUTED SHARED MEMORY SYSTEM | 12/07/2004 | 6829683 |
| US | MEMORY DAUGHTER CARD APPARATUS, CONFIGURATIONS, AND METHODS | 04/27/2004 | 6726505 |
| US | SYSTEM AND METHOD FOR ACCURATE ADJUSTMENT OF DISCRETE INTEGRATED CIRCUIT DELAY LINES | 12/17/2002 | 6496048 |
| US | PRINTED CIRCUIT BOARD STIFFENER | 01/28/2003 | 6512676 |
| US | PRINTED CIRCUIT BOARD STIFFENER | 08/03/2004 | 6771517 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD AND APPARATUS FOR ACCESSING MMR REGISTERS DISTRIBUTED ACROSS A LARGE ASIC | 08/17/2004 | 6779072 |
| US | METHOD AND SYSTEM FOR COVERING MULTIPLE RESOURCES WITH A SINGLE CREDIT IN A COMPUTER SYSTEM | 02/28/2006 | 7007097 |
| US | BAFFLE SYSTEM FOR AIR COOLED COMPUTER ASSEMBLY | 11/19/2002 | 6483699 |
| TW | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 02/16/2004 | 188942 |
| US | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 02/08/2005 | 6853387 |
| US | COMPACT FLAT PANEL COLOR CALIBRATIONS SYSTEM | 02/08/2005 | 6853387 |
| US | HEAT SINK ATTACHMENT CLIP | 08/13/2002 | 6434007 |
| US | ASSEMBLY PROCESS AND HEAT SINK DESIGN FOR HIGH POWERED PROCESSOR | 12/14/2004 | 6831834 |
| US | METHOD AND CIRCUIT FOR RELIABLE DATA CAPTURE IN THE PRESENCE OF BUS-MASTER CHANGEOVERS | 01/04/2005 | 6839856 |
| US | TRANSLATING WRITE COMMANDS TO INITIATE PURGE REQUESTS TO MULTIPLE PROCESSORS | 08/05/2003 | 6604185 |
| US | PROVIDING SHARED AND NON-SHARED ACCESS TO MEMORY IN A SYSTEM WITH PLURAL PROCESSOR COHERENCE DOMAINS | 06/27/2006 | 7069306 |
| US | DRIVE SLED HANDLE | 07/03/2001 | D444471 |
| US | DRIVE SLED COVER | 07/03/2001 | D444474 |
| US | SERVER COVER | 07/03/2001 | D444461 |
| US | METHOD AND SYSTEM FOR MAINTAINING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM | 12/27/2005 | 6981101 |
| US | METHOD AND SYSTEM FOR CONTROLLING DATA ACCESS BETWEEN AT LEAST TWO MEMORY ARRANGEMENTS | 01/04/2005 | 6839820 |
| US | METHOD AND SYSTEM FOR CONTROLLING DATA ACCESS BETWEEN AT LEAST TWO MEMORY ARRANGEMENTS | 01/04/2005 | 6839820 |
| US | SYSTEM AND METHOD FOR GENERATING CLOCK SIGNALS | 08/27/2002 | 6441666 |
| US | METHOD AND SYSTEM FOR SPATIALLY COMPOSITING DIGITAL VIDEO IMAGES WITH A TILE PATTERN LIBRARY | 04/11/2006 | 7027072 |
| US | MULTIPROCESSOR SYSTEM UTILIZING MULTIPLE LINKS TO IMPROVE POINT TO POINT BANDWIDTH | 11/04/2003 | 6643764 |
| US | METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR DETERMINING A STRUCTURE OF A GRAPHICS COMPOSITOR TREE | 04/25/2006 | 7034837 |
| US | PRINTED CIRCUIT BOARD COMPONENT PACKAGING | 11/26/2002 | 6487082 |
| US | SYSTEM AND METHOD FOR REPAIRING A MEMORY COLUMN | 04/20/2004 | 6724669 |
| US | SYSTEM AND METHOD FOR IMPROVING SPEED OF OPERATION OF INTEGRATED CIRCUITS | 09/16/2003 | 6621300 |
| US | METHOD AND SYSTEM FOR PREFETCHING DATA | 07/12/2005 | 6918010 |
| US | SYNCHRONIZATION OF VERTICAL RETRACE FOR MULTIPLE PARTICIPATING GRAPHICS COMPUTERS | 09/14/2004 | 6791551 |
| US | SWAP BUFFER SYNCHRONIZATION IN A DISTRIBUTED RENDERING SYSTEM | 10/26/2004 | 6809733 |
| US | SERVER PRODUCT FACEPLATE | 10/08/2002 | D464056 |
| US | MULTI-DEVICE FACEPLATES | 04/22/2003 | D473561 |
| TW | MULTI-DEVICE FACEPLATES | 02/04/2004 | 86962 |
| FR | MULTI-DEVICE FACEPLATES | 08/02/2002 | 671245-46 |
| JP | MULTI-DEVICE FACEPLATES | 04/02/2004 | 1205713 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| GB | MULTI-DEVICE FACEPLATES | 07/18/2002 | 3002487 |
| DE | MULTI-DEVICE FACEPLATES | 03/27/2002 | 402028961 |
| US | SYNCHRONIZED IMAGE DISPLAY AND BUFFER SWAPPING IN A MULTIPLE DISPLAY ENVIRONMENT | 12/14/2004 | 6831648 |
| US | SYSTEM AND METHOD FOR DECOUPLING THE USER INTERFACE AND APPLICATION WINDOW IN A GRAPHICS APPLICATION | 01/10/2006 | 6985149 |
| US | AUTOMATIC FRAME ACCUMULATOR | 11/02/1999 | 5977965 |
| US | INCREASING COLOR ACCURACY | 11/18/2003 | 6650337 |
| US | CLUSTER FILE SYSTEM | 09/27/2005 | 6950833 |
| US | SYSTEM AND METHOD FOR GENERATING SEQUENCES AND GLOBAL INTERRUPTS IN A CLUSTER OF NODES | 03/21/2006 | 7016998 |
| US | CACHE MEMORY FOR IDENTIFYING LOCKED AND LEAST RECENTLY USED STORAGE LOCATIONS | 06/07/2005 | 6904501 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR INTUITIVE INTERACTIVE NAVIGATION CONTROL IN VIRTUAL ENVIRONMENTS | 06/06/2006 | 7058896 |
| US | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REAL TIME SHADING OF COMPUTER GENERATED IMAGES | 12/02/2003 | 6657624 |
| US | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR BLENDING TEXTURES DURING RENDERING OF A COMPUTER GENERATED IMAGE USING A SINGLE TEXTURE AS A MASK *** provisional combined and filed with 1251.00*** non provisionals to be filed as two separate cases | 10/26/2004 | 6809739 |
| US | A METHOD OF ACCELERATING MINIFIED TEXTURED CACHE ACCESS | 08/15/2000 | 6104415 |
| US | BUS SPEED CONTROLLER USING SWITCHES | 09/28/2004 | 6799238 |
| US | SYSTEM AND METHOD FOR IMPLEMENTING SHADOWS USING PRE-COMPUTED TEXTURES | 06/20/2006 | 7064755 |
| US | SYSTEM AND METHOD FOR MANAGING GRAPHICS APPLICATIONS | 01/03/2006 | 6982682 |
| US | METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR | 04/05/2005 | 6877030 |
| US | ACTUATABLE CONNECTOR SYSTEM | 01/06/2004 | 6672878 |
| US | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | 03/30/2004 | 6714464 |
| US | EXTERNAL FAN AND METHOD FOR EXCHANGING AIR WITH MODULAR BRICKS IN A COMPUTER SYSTEM | 08/08/2006 | 7088581 |
| US | METHOD AND SYSTEM FOR EXCHANGING AIR WITH MODULAR BRICKS IN A COMPUTER SYSTEM | 04/19/2005 | 6882531 |
| US | MODULAR FAN BRICK AND METHOD FOR EXCHANGING AIR IN A BRICK-BASED COMPUTER SYSTEM | 07/20/2004 | 6765795 |
| US | SYSTEM AND METHOD FOR HIERARCHICAL APPROXIMATION OF LEAST RECENTLY USED REPLACEMENT ALGORITHMS | 01/10/2006 | 6986001 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR NEAR-REAL TIME LOAD BALANCING ACROSS MULTIPLE RENDERING PIPELINES | 04/26/2005 | 6885376 |
| US | METHOD AND SYSTEM FOR FORMING AN OBJECT PROXY | 12/14/2004 | 6831642 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | SYSTEM AND METHOD FOR IMAGE-BASED RENDERING WITH PROXY SURFACE ANIMATION | 08/02/2005 | 6924805 |
| US | COMPUTER ENCLOSURE AND METHOD FOR MANUFACTURE | 11/02/2004 | 6813151 |
| US | SYSTEM AND METHOD FOR ENCODING PAGE SIZE INFORMATION | 08/29/2006 | 7100018 |
| US | ADDRESS TRANSLATION USING A PAGE SIZE TAG | 08/08/2006 | 7089398 |
| US | TEXTURE ROAMING VIA DIMENSION ELEVATION | 03/14/2006 | 7012614 |
| US | PRIMITIVE CULLING APPARATUS AND METHOD | 05/31/2005 | 6900818 |
| US | CLUSTER FILESYSTEM | 08/27/2005 | 6950833 |
| | | | |
| US | SYSTEM AND METHOD FOR REDUCING MEMORY LATENCY DURING READ REQUESTS | 08/03/2005 | 6938128 |
| JP | FLEXIBLE CHAINING IN VECTOR PROCESSOR WITH SELECTIVE USE OF VECTOR REGISTERS AS OPERAND AND RESULT REGISTERS | 04/16/1996 | 2511397 |
| US | FLEXIBLE CHAINING IN VECTOR PROCESSOR WITH SELECTIVE USE OF VECTOR REGISTERS AS OPERAND AND RESULT REGISTERS | 02/13/1990 | 4901230 |
| CA | PERIPHERAL INTERFACE SYSTEM | 10/27/1987 | 1228677 |
| JP | PERIPHERAL INTERFACE SYSTEM | 06/21/1994 | 1850940 |
| US | PERIPHERAL INTERFACE SYSTEM | 02/21/1989 | 4807121 |
| US | SYSTEM FOR MULTIPROCESSOR COMMUNICATION USING LOCAL AND COMMON SEMAPHORE AND INFORMATION REGISTERS | 06/28/1988 | 4754398 |
| US | DATA MODULATION INTERFACE | 09/13/1988 | 4771440 |
| US | ZIF EDGE CONNECTOR | 10/20/1987 | 4700996 |
| US | WIRE/DISK BOARD-TO-BOARD INTERCONNECT DEVICE | 08/22/1989 | 4859188 |
| US | LEAD BONDING OF CHIPS TO CIRCUIT BOARDS AND CIRCUIT BOARDS TO CIRCUIT BOARDS | 10/08/1991 | 5054192 |
| US | SINGLE DISK EMULATION INTERFACE FOR AN ARRAY OF SYNCHRONOUS SPINDLE DISK DRIVES | 07/07/1992 | 5128810 |
| US | COMPUTER SIGNAL INTERCONNECT APPARATUS | 09/01/1992 | 5144691 |
| US | GALLIUM ARSENIDE LOGIC DESIGN SYSTEM | 10/23/1990 | 4965863 |
| US | OPTICAL CLOCK DISTRIBUTION METHOD AND APPARATUS | 08/15/1995 | 5442475 |
| EP | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 10/21/1992 | 419499 |
| FR | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 10/21/1992 | 419499 |
| GB | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 10/21/1992 | 419499 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| JP | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 08/04/2000 | 3095393 |
| US | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 09/20/1994 | 5349677 |
| DE | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 10/21/1992 | 68903280.3 |
| US | INTEGRATED CIRCUIT CHIP CARRIER LID | 11/02/1993 | 5258576 |
| US | TWO-PIECE EDGE ZIF CONNECTOR WITH SLIDING BLOCK | 01/15/1991 | 4984993 |
| US | PARALLEL BOARD ZIF MODULE CONNECTOR | 03/27/1990 | 4911645 |
| US | METHOD AND APPARATUS FOR COOLING AN INTEGRATED CIRCUIT CHIP DURING TESTING | 01/01/1991 | 4982153 |
| US | SKEW-COMPENSATED CLOCK DISTRIBUTION SYSTEM | 11/02/1993 | 5258660 |
| US | METHOD OF ADJUSTING FOR CLOCK SKEW | 05/09/1995 | 5414381 |
| US | METHOD FOR ADJUSTING CLOCK SKEW | 11/14/1995 | 5467040 |
| US | APPARATUS FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 08/25/1992 | 5142638 |
| US | METHOD FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 04/13/1993 | 5202970 |
| US | FLEXIBLE AUTOMATED BONDING METHOD AND APPARATUS | 07/07/1992 | 5127570 |
| EP | METHOD AND APPARATUS FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 06/08/1994 | 532542 |
| FR | METHOD AND APPARATUS FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 06/08/1994 | 532542 |
| US | METHOD AND APPARATUS FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 09/21/1993 | 5247637 |
| DE | METHOD AND APPARATUS FOR SHARING MEMORY IN A MULTIPROCESSOR SYSTEM | 06/08/1994 | 69102431.6 |
| US | READ-WHILE-WRITE RAM CELL | 10/16/1990 | 4964081 |
| EP | MODULAR INPUT/OUTPUT SYSTEM FOR SUPERCOMPUTERS | 06/28/1995 | 485507 |
| FR | MODULAR INPUT/OUTPUT SYSTEM FOR SUPERCOMPUTERS | 06/28/1995 | 485507 |
| GB | MODULAR INPUT/OUTPUT SYSTEM FOR SUPERCOMPUTERS | 06/28/1995 | 485507 |
| US | MODULAR INPUT/OUTPUT SYSTEM FOR SUPERCOMPUTERS | 09/13/1994 | 5347637 |
| DE | MODULAR INPUT/OUTPUT SYSTEM FOR SUPERCOMPUTERS | 06/28/1995 | 69020569.4 |
| US | DISTRIBUTING SYSTEM FOR MULTI-PROCESSOR INPUT AND OUTPUT USING CHANNEL ADAPTERS | 02/07/1995 | 5388217 |
| US | SINGLE DISK EMULATION INTERFACE FOR AN ARRAY OF ASYNCHRONOUSLY OPERATING DISK DRIVES | 06/08/1993 | 5218689 |
| US | REDUCED CAPACITANCE CHIP CARRIER | 07/28/1992 | 5134247 |
| US | SYSTEM FOR MULTIPROCESSOR COMMUNICATION | 06/11/1996 | 5526487 |
| US | HIGH POWER, HIGH DENSITY INTERCONNECT METHOD AND APPARATUS FOR INTEGRATED CIRCUITS | 07/07/1992 | 5127986 |
| US | HIGH POWER, HIGH DENSITY INTERCONNECT METHOD AND APPARATUS FOR INTEGRATED CIRCUITS | 02/09/1993 | 5185502 |
| US | TWISTED WIRE JUMPER ELECTRICAL INTERCONNECTOR AND METHOD OF MAKING | 05/14/1991 | 5014419 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | DUAL CONTACT BEAM ASSEMBLY FOR AN IC TEST FIXTURE | 12/29/1992 | 5175496 |
| EP | A SCALABLE PARALLEL VECTOR COMPUTER SYSTEM | 12/28/1994 | 553158 |
| FR | A SCALABLE PARALLEL VECTOR COMPUTER SYSTEM | 12/28/1994 | 553158 |
| GB | A SCALABLE PARALLEL VECTOR COMPUTER SYSTEM | 12/28/1994 | 553158 |
| DE | A SCALABLE PARALLEL VECTOR COMPUTER SYSTEM | 12/28/1994 | 69106384.2 |
| US | VECTOR BIT-MATRIX MULTIPLY FUNCTIONAL UNIT | 12/08/1992 | 5170370 |
| US | CAM ACTUATED ELECTRICAL CONNECTOR | 12/04/1990 | 4975074 |
| US | AIR JET IMPINGEMENT ON MINIATURE PIN-FIN HEAT SINKS FOR COOLING ELECTRONIC COMPONENTS | 01/21/1992 | 5083194 |
| US | AIR MANIFOLD FOR COOLING ELECTRONIC DEVICES | 11/24/1992 | 5166775 |
| US | FIBER OPTIC CHANNEL EXTENDER INTERFACE METHOD AND APPARATUS | 02/14/1995 | 5390041 |
| US | COMMUNICATION PROTOCOL FOR TRANSFERRING INFORMATION ACROSS A SERIAL COMMUNICATION LINK | 01/07/1997 | 5592487 |
| US | FAULT TOLERANT NETWORKING ARCHITECTURE | 04/27/1993 | 5206952 |
| US | METHOD OF FABRICATING METALLIZED CHIP CARRIERS FROM WAFER-SHAPED SUBSTRATES | 01/26/1993 | 5182420 |
| US | METHOD OF FABRICATING METALLIZED CHIP CARRIERS FROM WAFER-SHAPED SUBSTRATES | 10/25/1994 | 5358826 |
| US | ERROR RECOVERY METHOD AND APPARATUS FOR HIGH PERFORMANCE DISK DRIVES | 02/01/1994 | 5283791 |
| US | VECTOR SHIFT FUNCTIONAL UNIT FOR SUCCESSIVELY SHIFTING OPERANDS STORED IN A VECTOR REGISTER BY CORRESPONDING SHIFT COUNTS STORED IN ANOTHER VECTOR REGISTER | 01/02/1996 | 5481746 |
| US | VECTOR WORD SHIFT BY VO SHIFT COUNT IN VECTOR | 12/08/1998 | 5848286 |
| US | VECTOR SHIFT FUNCTIONAL UNIT FOR SUCCESSIVELY SHIFTING | 08/01/2000 | 6098162 |
| US | ASSOCIATIVE SCALAR DATA CACHE WITH WRITE-THROUGH | 02/10/1998 | 5717895 |
| US | METHOD OF MANUFACTURING INTERCONNECT BUMPS | 02/08/1994 | 5283948 |
| US | METHOD AND APPARATUS FOR LASER MASKING OF LEAD BONDING | 03/16/1993 | 5194710 |
| EP | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 07/30/1997 | 571395 |
| FR | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 07/30/1997 | 571395 |
| GB | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 07/30/1997 | 571395 |
| EP | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 05/10/2000 | 712076 |
| FR | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 05/10/2000 | 712076 |
| GB | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 05/10/2000 | 712076 |
| US | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 07/18/1995 | 5434970 |
| DE | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 07/30/1997 | 69127101.1 |
| DE | SYSTEM FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATION | 05/10/2000 | 69132195.7 |
| US | MULTIPROCESSING SYSTEM USING INDIRECT ADDRESSING TO ACCESS RESPECTIVE LOCAL SEMAPHORE REGISTERS BITS FOR SETTING THE BIT OR BRANCHING IF THE BIT IS SET | 11/22/1994 | 5367690 |
| US | SYSTEM AND METHOD FOR DISTRIBUTED MULTIPROCESSOR COMMUNICATIONS | 07/06/1999 | 5920714 |
| EP | APPARATUS AND METHOD FOR TESTING OF NEW OPERATING SYSTEMS THROUGH PRIVILEGED INSTRUCTION TRAPPING | 06/28/1995 | 578646 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| FR | APPARATUS AND METHOD FOR TESTING OF NEW OPERATING SYSTEMS THROUGH PRIVILEGED INSTRUCTION TRAPPING | 06/28/1995 | 578646 |
| GB | APPARATUS AND METHOD FOR TESTING OF NEW OPERATING SYSTEMS THROUGH PRIVILEGED INSTRUCTION TRAPPING | 06/28/1995 | 578646 |
| US | APPARATUS AND METHOD FOR TESTING OF NEW OPERATING SYSTEMS THROUGH PRIVILEGED INSTRUCTION TRAPPING | 12/06/1994 | 5371879 |
| DE | APPARATUS AND METHOD FOR TESTING OF NEW OPERATING SYSTEMS THROUGH PRIVILEGED INSTRUCTION TRAPPING | 06/28/1995 | 69110908.7 |
| EP | REAL TIME I/O OPERATION IN A VECTOR PROCESSING COMPUTER SYSTEM BY RUNNING DESIGNATED PROCESSORS IN PRIVILEGED MODE AND BYPASS THE OPERATING SYSTEM | 10/04/1995 | 577614 |
| FR | REAL TIME I/O OPERATION IN A VECTOR PROCESSING COMPUTER SYSTEM BY RUNNING DESIGNATED PROCESSORS IN PRIVILEGED MODE AND BYPASS THE OPERATING SYSTEM | 10/04/1995 | 577614 |
| GB | REAL TIME I/O OPERATION IN A VECTOR PROCESSING COMPUTER SYSTEM BY RUNNING DESIGNATED PROCESSORS IN PRIVILEGED MODE AND BYPASS THE OPERATING SYSTEM | 10/04/1995 | 577614 |
| US | REAL TIME I/O OPERATION IN A VECTOR PROCESSING COMPUTER SYSTEM BY RUNNING DESIGNATED PROCESSORS IN PRIVILEGED MODE AND BYPASS THE OPERATING SYSTEM | 02/14/1995 | 5390300 |
| DE | REAL TIME I/O OPERATION IN A VECTOR PROCESSING COMPUTER SYSTEM BY RUNNING DESIGNATED PROCESSORS IN PRIVILEGED MODE AND BYPASS THE OPERATING SYSTEM | 10/04/1995 | 69113639.4 |
| US | MEMORY RANGE MONITORING APPARATUS FOR A MULTIPROCESSOR COMPUTER SYSTEM | 03/15/1994 | 5295260 |
| US | METHOD OF FABRICATING SILICON-BASED CARRIERS | 03/23/1993 | 5196377 |
| US | PRINTED CIRCUIT BOARD WITH COOLING MONITORING SYSTEM | 01/25/1994 | 5281026 |
| EP | HIGH PERFORMANCE MANTISSA DIVIDER | 09/23/1998 | 658256 |
| FR | HIGH PERFORMANCE MANTISSA DIVIDER | 09/23/1998 | 658256 |
| GB | HIGH PERFORMANCE MANTISSA DIVIDER | 09/23/1998 | 658256 |
| US | HIGH PERFORMANCE MANTISSA DIVIDER | 11/02/1993 | 5258944 |
| DE | HIGH PERFORMANCE MANTISSA DIVIDER | 09/23/1998 | 69321241.1 |
| US | METALLIZED CONNECTOR BLOCK | 05/18/1993 | 5211567 |
| EP | SOLID STATE STORAGE DEVICE | 08/23/2000 | 642685 |
| FR | SOLID STATE STORAGE DEVICE | 08/23/2000 | 642685 |
| GB | SOLID STATE STORAGE DEVICE | 08/23/2000 | 642685 |
| US | SOLID STATE STORAGE DEVICE | 06/14/1994 | 5321697 |
| DE | SOLID STATE STORAGE DEVICE | 08/23/2000 | 69329282.2 |
| US | OPTICAL CLOCK DISTRIBUTION SYSTEM | 07/16/1996 | 5537498 |
| US | PARALLEL PROCESSING SYSTEM | 01/14/1992 | 5081573 |
| US | PARALLEL VECTOR PROCESSING SYSTEM FOR INDIVIDUAL AND BROADCAST DISTRIBUTION OF OPERANDS AND CONTROL INFORMATION | 07/06/1993 | 5226171 |
| US | DIRECT-EXECUTION MICROPROGRAMMABLE MICROPROCESSOR SYSTEM | 08/02/1988 | 4761733 |
| US | MASSIVELY PARALLEL VECTOR PROCESSING COMPUTER | 01/02/1990 | 4891751 |
| US | LINEAR NEAREST NEIGHBOR INTERCONNECT BUS SYSTEM | 03/26/1991 | 5003508 |
| DE | SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 08/06/2003 | 733236 |
| EP | SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 08/06/2003 | 733236 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| FR | SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 08/06/2003 | 733236 |
| GB | SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 08/06/2003 | 733236 |
| US | SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 06/09/1998 | 5765181 |
| US | DIRECTION ORDER PRIORITY ROUTING OF PACKETS BETWEEN NODES IN A NETWORKED SYSTEM | 07/02/1996 | 5533198 |
| US | CONFIGURING OF NETWORKED SYSTEM TO PERMIT REPLACEMENT OF FAILED MODES AND SELECTION OF ALTERNATE PATHS | 11/18/1997 | 5689646 |
| EP | BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/14/1999 | 733234 |
| FR | BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/14/1999 | 733234 |
| GB | BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/14/1999 | 733234 |
| US | BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/18/1995 | 5434995 |
| DE | BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/14/1999 | 69419524.3 |
| US | APPARATUS FOR COOLING DAUGHTER BOARDS | 08/30/1994 | 5343359 |
| US | BOUNDARY SCAN TESTING USING CLOCKED SIGNAL | 01/23/1996 | 5487074 |
| US | MATRIX PROCESSOR SYSTEM | 08/28/2001 | 6282583 |
| EP | MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM | 07/14/1999 | 734554 |
| FR | MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM | 07/14/1999 | 734554 |
| GB | MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM | 07/14/1999 | 734554 |
| US | MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM | 12/03/1996 | 5581705 |
| DE | MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM | 07/14/1999 | 69419525.1 |
| EP | CLUSTER ARCHITECTURE FOR A HIGHLY PARALLEL SCALAR/VECTOR MULTIPROCESSOR SYSTEM | 09/01/1999 | 512007 |
| FR | CLUSTER ARCHITECTURE FOR A HIGHLY PARALLEL SCALAR/VECTOR MULTIPROCESSOR SYSTEM | 09/01/1999 | 512007 |
| GB | CLUSTER ARCHITECTURE FOR A HIGHLY PARALLEL SCALAR/VECTOR MULTIPROCESSOR SYSTEM | 09/01/1999 | 512007 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | CLUSTER ARCHITECTURE FOR A HIGHLY PARALLEL SCALAR/VECTOR MULTIPROCESSOR SYSTEM | 03/23/1993 | 5197130 |
| DE | CLUSTER ARCHITECTURE FOR A HIGHLY PARALLEL SCALAR/VECTOR MULTIPROCESSOR SYSTEM | 09/01/1999 | 69033272.6 |
| US | INTERLEAVED MEMORY ACCESS SYSTEM HAVING VARIABLE-SIZED SEGMENTS LOGICAL ADDRESS SPACES AND MEANS FOR DIVIDING/MAPPING PHYSICAL ADDRESS INTO HIGHER AND LOWER ORDER ADDRESSES | 10/01/1996 | 5561784 |
| US | PACKAGING ARCHITECTURE FOR A HIGHLY PARALLEL MULTIPROCESSOR SYSTEM | 10/05/1993 | 5251097 |
| US | METHOD AND APPARATUS FOR MON-SEQUENTIAL RESOURCE ACCESS | 05/04/1993 | 5208914 |
| US | METHOD & APPARATUS FOR A SPECIAL PURPOSE BOOLEAN UNIT | 12/29/1992 | 5175862 |
| US | METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES | 01/12/1993 | 5179702 |
| US | METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES | 02/27/2001 | 6195676 |
| US | SCALAR/VECTOR PROCESSOR | 07/04/1995 | 5430884 |
| US | METHOD AND APPARATUS FOR CHAINING VECTOR INSTRUCTIONS | 06/17/1997 | 5640524 |
| US | PARTITIONED ADDRESSING APPARATUS FOR VECTOR/SCALAR REGISTERS | 04/28/1998 | 5745721 |
| US | VECTOR PROCESSOR HAVING REGISTERS FOR CONTROL BY VECTOR REGISTERS | 08/06/1996 | 5544337 |
| US | VECTOR PROCESSOR HAVING FUNCTIONAL UNIT PATHS OF DIFFERING PIPELINE LENGTHS | 01/28/1997 | 5598547 |
| US | METHOD OF PROCESSING A SEQUENCE OF CONDITIONAL VECTOR IF STATEMENTS | 04/22/1997 | 5623650 |
| US | METHOD OF PROCESSING CONDITIONAL BRANCH INSTRUCTIONS IN SCALAR/VECTOR PROCESSOR | 01/06/1998 | 5706490 |
| US | DATA PROCESSING SYSTEM FOR PROCESSING ONE AND TWO PARCEL INSTRUCTIONS | 02/10/1998 | 5717881 |
| US | VECTOR/SCALAR PROCESSOR WITH SIMULTANEOUS PROCESSING AND INSTRUCTION CACHE FILLING | 08/19/1997 | 5659706 |
| US | METHOD AND APPARATUS FOR A MULTIPROCESSOR RESOURCE LOCKOUT INSTRUCTION | 03/12/1996 | 5499356 |
| US | DISTRIBUTED ARCHITECTURE FOR INPUT/OUTPUT FOR A MULTI-PROCESSOR SYSTEM | 12/01/1992 | 5168547 |
| US | CONTROL AND MAINTENANCE SUBSYSTEM FOR USE WITH A MULTIPROCESSOR COMPUTER SYSTEM | 10/12/1993 | 5253359 |
| US | GLOBAL REGISTERS FOR A MULTIPROCESSOR SYSTEM | 11/17/1992 | 5165038 |
| US | METHOD AND APPARATUS FOR ACCESSSING GLOBAL REGISTERS IN A MULTIPROCESSOR SYSTEM | 06/04/1996 | 5524255 |
| US | METHOD AND APPARATUS FOR A MULTIPLE REQUEST TOGGLING PRIORITY SYSTEM | 12/01/1992 | 5168570 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | DEDICATED CENTRALIZED SIGNALING MECHANISM FOR SELECTIVELY SIGNALING DEVICES IN A MULTI-PROCESSOR SYSTEM | 08/24/1993 | 5239629 |
| US | FAST INTERRUPT MECHANISM FOR INTERRUPTING PROCESSORS IN PARALLEL IN A MULTIPROCESSOR SYSTEM WHEREIN PROCESSORS ARE ASSIGNED PROCESS ID NUMBERS | 03/09/1993 | 5193187 |
| US | METHOD AND APPARATUS FOR SINGLE STEP CLOCKING ON SIGNAL PATHS LONGER THAN A CLOCK CYCLE | 10/08/1991 | 5055707 |
| EP | COMPUTER WITH INTEGRATED HIERARCHICAL REPRESENTATION OF PROGRAM WHEREIN IHR FILE IS AVAILABLE FOR DEBUGGING AND OPTIMIZING DURING TARGET EXECUTION | 12/08/1999 | 537257 |
| FR | COMPUTER WITH INTEGRATED HIERARCHICAL REPRESENTATION OF PROGRAM WHEREIN IHR FILE IS AVAILABLE FOR DEBUGGING AND OPTIMIZING DURING TARGET EXECUTION | 12/08/1999 | 537257 |
| GB | COMPUTER WITH INTEGRATED HIERARCHICAL REPRESENTATION OF PROGRAM WHEREIN IHR FILE IS AVAILABLE FOR DEBUGGING AND OPTIMIZING DURING TARGET EXECUTION | 12/08/1999 | 537257 |
| US | COMPUTER WITH INTEGRATED HIERARCHICAL REPRESENTATION OF PROGRAM WHEREIN IHR FILE IS AVAILABLE FOR DEBUGGING AND OPTIMIZING DURING TARGET EXECUTION | 12/29/1992 | 5175856 |
| DE | COMPUTER WITH INTEGRATED HIERARCHICAL REPRESENTATION OF PROGRAM WHEREIN IHR FILE IS AVAILABLE FOR DEBUGGING AND OPTIMIZING DURING TARGET EXECUTION | 12/08/1999 | 69131832.8 |
| EP | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 12/08/1999 | 535107 |
| FR | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 12/08/1999 | 535107 |
| GB | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 12/08/1999 | 535107 |
| JP | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 06/04/2002 | 3288372 |
| US | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 04/13/1993 | 5202975 |
| DE | METHOD FOR OPTIMIZING INSTRUCTION SCHEDULING FOR A PROCESSOR HAVING MULTIPLE FUNCTIONAL RESOURCES | 06/21/2000 | 69131830.1 |
| US | METHOD FOR INSERTING A PATH INSTRUCTION DURING COMPILATION OF COMPUTER PROGRAMS FOR PROCESSORS HAVING MULTIPLE FUNCTIONAL UNITS | 04/26/1994 | 5307478 |
| EP | METHOD FOR REPRESENTING SCALAR DATA DEPENDENCIES FOR AN OPTIMIZING COMPILER | 03/11/1998 | 533813 |
| FR | METHOD FOR REPRESENTING SCALAR DATA DEPENDENCIES FOR AN OPTIMIZING COMPILER | 03/11/1998 | 533813 |
| GB | METHOD FOR REPRESENTING SCALAR DATA DEPENDENCIES FOR AN OPTIMIZING COMPILER | 03/11/1998 | 533813 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD FOR REPRESENTING SCALAR DATA DEPENDENCIES FOR AN OPTIMIZING COMPILER | 04/21/1992 | 5107418 |
| DE | METHOD FOR REPRESENTING SCALAR DATA DEPENDENCIES FOR AN OPTIMIZING COMPILER | 03/11/1998 | 69129067.9 |
| US | MINIATURE CONTROLLED-IMPEDANCE TRANSMISSION LINE CABLE AND METHOD OF MANUFACTURE | 05/14/1991 | 5015800 |
| EP | METHOD FOR EFFICIENT NON-VIRTUAL MAIN MEMORY MANAGEMENT | 04/26/2000 | 533805 |
| FR | METHOD FOR EFFICIENT NON-VIRTUAL MAIN MEMORY MANAGEMENT | 04/26/2000 | 533805 |
| GB | METHOD FOR EFFICIENT NON-VIRTUAL MAIN MEMORY MANAGEMENT | 04/26/2002 | 533805 |
| US | METHOD FOR EFFICIENT NON-VIRTUAL MAIN MEMORY MANAGEMENT | 10/27/1992 | 5159678 |
| US | MULTILAYER INTERCONNECT SYSTEM FOR AN AREA ARRAY INTERCONNECTION USING SOLID STATE DIFFUSION | 01/11/1994 | 5276955 |
| US | METHOD & APPARATUS FOR SEPARATE MARK AND WAIT INSTRUCTIONS FOR PROCESSORS HAVING MULTIPLE PORTS | 01/10/1995 | 5381536 |
| US | TRANSMISSION LINE WITH FLUID PERMEABLE JACKET | 08/25/1992 | 5142100 |
| US | METHOD AND APPARATUS FOR A UNIFIED PARALLEL PROCESSING ARCHITECTURE | 06/27/1995 | 5428803 |
| US | EXTENDIBLE CLOCK MECHANISM | 04/29/1997 | 5625831 |
| US | CLOCK DISTRIBUTION APPARATUS AND PROCESS PARTICULARLY USEFUL IN MULTIPROCESSOR SYSTEMS | 03/08/1994 | 5293626 |
| EP | DUAL LEVEL SCHEDULING OF PROCESS TO MULTIPLE PARALLEL REGIONS OF A MULTITHREADED PROGRAM ON A TIGHTLY COUPLED MULTIPROCESSOR COMPUTER SYSTEM | 05/12/1999 | 544822 |
| FR | DUAL LEVEL SCHEDULING OF PROCESS TO MULTIPLE PARALLEL REGIONS OF A MULTITHREADED PROGRAM ON A TIGHTLY COUPLED MULTIPROCESSOR COMPUTER SYSTEM | 05/12/1999 | 544822 |
| GB | DUAL LEVEL SCHEDULING OF PROCESS TO MULTIPLE PARALLEL REGIONS OF A MULTITHREADED PROGRAM ON A TIGHTLY COUPLED MULTIPROCESSOR COMPUTER SYSTEM | 05/12/1999 | 544822 |
| US | DUAL LEVEL SCHEDULING OF PROCESS TO MULTIPLE PARALLEL REGIONS OF A MULTITHREADED PROGRAM ON A TIGHTLY COUPLED MULTIPROCESSOR COMPUTER SYSTEM | 08/16/1994 | 5339415 |
| DE | DUAL LEVEL SCHEDULING OF PROCESS TO MULTIPLE PARALLEL REGIONS OF A MULTITHREADED PROGRAM ON A TIGHTLY COUPLED MULTIPROCESSOR COMPUTER SYSTEM | 05/12/1999 | 69131228.1 |
| US | SYSTEM HAVING INTEGRATED DISPATCHER FOR SELF-SCHEDULING PROCESSORS TO EXECUTE MULTIPLE TYPES OF PROCESSORS | 09/19/1995 | 5452452 |
| US | VECTORIZED LR PARSING OF COMPUTER PROGRAMS | 03/09/1993 | 5193192 |
| US | RESPONDING TO SERVICE REQUESTS USING MINIMAL SYSTEM-SIDE CONTEXT IN A MULTIPROCESSOR ENVIRONMENT | 02/14/1995 | 5390329 |
| US | SYSTEM FOR COMMUNICATING AMONG PROCESSORS HAVING DIFFERENT SPEEDS | 04/13/1993 | 5202988 |
| US | GRAPHICAL DISPLAY OF COMPILER-GENERATED INTERMEDIATE DATABASE REPRESENTATION | 02/16/1993 | 5187789 |
| US | CLOCK PULSE MEASURING AND DESKEWING SYSTEM AND PROCESS | 07/12/1994 | 5329188 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | CLOCK STARTUP STABILIZATION FOR COMPUTER SYSTEMS | 10/11/1994 | 5355397 |
| US | VERTICAL SEMICONDUCTOR INTERCONNECTION METHOD AND STRUCTURE | 08/20/1991 | 5041903 |
| US | REPETITIVE SIGNAL DETECTOR FOR PREVENTING THERMAL RUNAWAY | 05/23/1995 | 5418481 |
| EP | VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 02/14/2001 | 737338 |
| FR | VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 02/14/2001 | 737338 |
| GB | VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 02/14/2001 | 737338 |
| US | VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 07/21/1998 | 5784706 |
| DE | VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 02/14/2001 | 69426708.2 |
| US | SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL | 12/10/1996 | 5583990 |
| EP | MULTIDIMENSIONAL INTERCONNECTION AND ROUTING NETWORK FOR AN MPP COMPUTER | 07/06/2005 | 733237 |
| US | NETWORKED MULTIPROCESSOR SYSTEM WITH GLOBAL DISTRIBUTED MEMORY AND BLOCK TRANSFER ENGINE | 08/18/1998 | 5797035 |
| US | MULTIPROCESSOR COMPUTER SYSTEM WITH INTERLEAVED PROCESSING ELEMENT NODES | 04/07/1998 | 5737628 |
| EP | APPARATUS AND METHOD FOR TESTING USING A CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS | 04/12/2000 | 792486 |
| FR | APPARATUS AND METHOD FOR TESTING USING A CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS | 04/12/2000 | 792486 |
| GB | APPARATUS AND METHOD FOR TESTING USING A CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS | 04/12/2000 | 792486 |
| US | APPARATUS AND METHOD FOR TESTING USING A CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS | 01/09/2001 | 6173428 |
| DE | APPARATUS AND METHOD FOR TESTING USING A CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS | 04/12/2000 | 69516303.5 |
| US | CONFIGURABLE SPARE MEMORY CHIPS | 02/21/1995 | 5392292 |
| US | RECURSIVE ADDRESS CENTRIFUGE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 12/09/1997 | 5696922 |
| US | RECURSIVE ADDRESS CENTRIFUGE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS | 09/12/2000 | 6119198 |
| US | SYNCHRONIZED STEREOSCOPIC DISPLAY SYSTEM | 09/14/1993 | 5245319 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | METHOD FOR COMPILING LOOPS HAVING RECURSIVE EQUATIONS BY DETECTING AND CORRECTING RECURRING DATA POINTS BEFORE STORING THE RESULT TO MEMORY | 09/21/1993 | 5247696 |
| EP | METHODS FOR EFFICIENT DISTRIBUTION OF PARALLEL TASKS TO SLAVE PROCESSES IN A MULTIPROCESSING SYSTEM | 06/03/1998 | 491342 |
| FR | METHODS FOR EFFICIENT DISTRIBUTION OF PARALLEL TASKS TO SLAVE PROCESSES IN A MULTIPROCESSING SYSTEM | 06/03/1998 | 491342 |
| US | METHODS FOR EFFICIENT DISTRIBUTION OF PARALLEL TASKS TO SLAVE PROCESSES IN A MULTIPROCESSING SYSTEM | 10/26/1993 | 5257372 |
| DE | METHODS FOR EFFICIENT DISTRIBUTION OF PARALLEL TASKS TO SLAVE PROCESSES IN A MULTIPROCESSING SYSTEM | 06/03/1998 | 69129526.3 |
| US | OPTIMIZATION OF ALTERNATE LOOP EXITS | 11/01/1994 | 5361354 |
| US | METHOD FOR USE IN DESIGNING AN ARBITRARILY SHAPED OBJECT | 09/26/1995 | 5453934 |
| US | METHOD OF MANAGING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM | 10/15/1996 | 5566321 |
| US | METHOD AND APPARATUS FOR LOCKING SHARED MEMORY LOCATIONS IN MULTIPROCESSING SYSTEMS | 07/09/1996 | 5535365 |
| US | METHOD FOR THE DYNAMIC ALLOCATION OF PAGE SIZES IN VIRTUAL MEMORY | 09/01/1998 | 5802341 |
| US | METHOD FOR THE DYNAMIC ALLOCATION OF ARRAY SIZES IN A MULTIPROCESSOR SYSTEM | 12/17/1996 | 5586325 |
| US | OUTER LOOP VECTORIZATION | 09/01/1998 | 5802375 |
| US | ARRAY ADDRESS AND LOOP ALIGNMENT CALCULATIONS | 10/03/2000 | 6128639 |
| US | METHOD AND APPARATUS FOR REMOVING POWER-OF-TWO RESTRICTIONS ON DISTRIBUTED ADDRESSING | 05/04/1999 | 5900023 |
| EP | BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS | 02/20/2002 | 829047 |
| FR | BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS | 02/20/2002 | 829047 |
| GB | BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS | 02/20/2002 | 829047 |
| US | BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS | 02/24/1998 | 5721921 |
| DE | BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS | 02/20/2002 | 69619366.3 |
| US | USING EXTERNAL REGISTERS TO EXTEND MEMORY REFERENCE CAPABILITIES OF A MICROPROCESSOR | 11/10/1998 | 5835925 |
| US | METHOD OF HANDLING ARBITRARY SIZE MESSAGE QUEUES IN WHICH A MESSAGE IS WRITTEN INTO AN ALIGNED BLOCK OF EXTERNAL REGISTERS WITHIN A PLURALITY OF EXTERNAL REGISTERS | 02/22/2000 | 6029212 |
| US | STREAM BUFFERS FOR HIGH-PERFORMANCE COMPUTER MEMORY SYSTEMS | 06/02/1998 | 5761706 |
| EP | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 01/12/2000 | 821816 |
| FR | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 01/12/2000 | 821816 |
| GB | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 01/12/2000 | 821816 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| JP | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 03/12/2004 | 3532574 |
| US | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 12/23/1997 | 5701416 |
| DE | ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK | 01/12/2000 | 69514550.9 |
| US | SYSTEM FOR RANDOMLY MODIFYING VIRTUAL CHANNEL ALLOCATION AND ACCEPTING THE RANDOM MODIFICATION BASED ON THE COST FUNCTION | 08/19/1997 | 5659796 |
| US | TRANSPARENT RELOCATION OF REAL MEMORY ADDRESSES IN THE MAIN MEMORY OF A DATA PROCESSOR | 06/09/1998 | 5765198 |
| US | SYSTEM AND METHOD FOR DENSITY TIME VECTOR CONDITIONAL OPERATIONS | 08/17/1999 | 5940625 |
| US | SPATIAL DERIVATIVE BUS ENCODER AND DECODER | 11/12/2002 | 6480548 |
| US | DAUGHTER CARD ASSEMBLY | 06/02/1998 | 5761043 |
| US | MESSAGING IN DISTRIBUTED MEMORY MULTIPROCESSING SYSTEM HAVING SHELL CIRCUITRY FOR ATOMIC CONTROL OF MESSAGE STORAGE QUEUE'S TAIL POINTER STRUCTURE IN LOCAL MEMORY | 11/24/1998 | 5841973 |
| US | MASSIVELY PARALLEL PROCESSING SYSTEM USING TWO DATA PATHS: ONE CONNECTING ROUTER CIRCUIT TO THE INTERCONNECT NETWORK AND THE OTHER CONNECTING ROUTER CIRCUIT TO I/O CONTROLLER | 01/26/1999 | 5864738 |
| EP | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 11/24/1999 | 858633 |
| FR | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 11/24/1999 | 858633 |
| GB | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 11/24/1999 | 858633 |
| US | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 04/25/2000 | 6055618 |
| DE | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 11/24/1999 | 69605319.5 |
| US | SYSTEM FOR ARBITRATING PACKETIZED DATA FROM THE NETWORK TO THE PERIPHERAL RESOURCES AND PRIORITIZING THE DISPATCHING OF PACKETS ONTO THE NETWORK | 06/02/1998 | 5761534 |
| US | COOLING APPROACH FOR HIGH POWER INTEGRATED CIRCUITS MOUNTED ON PRINTED CIRCUIT BOARDS | 06/16/1998 | 5768104 |
| US | AIR OR LIQUID COOLED COMPUTER MODULE COLD PLATE | 10/23/2001 | 6305463 |
| US | COOLING CAP METHOD AND APPARATUS FOR TAB PACKAGED INTEGRATED CIRCUITS | 09/08/1998 | 5805418 |
| US | COOLING CAP METHOD AND APPARATUS FOR TAB PACKAGED INTEGRATED CIRCUITS | 10/05/1999 | 5963428 |
| US | METHOD AND APPARATUS FOR ADJUSTING THE POWER SUPPLY VOLTAGE PROVIDED TO MICROPROCESSORS | 12/02/1997 | 5694028 |
| US | RECONFIGURABLE RING-BASED NETWORK SYSTEM | 05/15/2001 | 6233704 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | ADAPTIVE CONGESTION CONTROL MECHANISM FOR MODULAR COMPUTER NETWORKS | 05/05/1998 | 5748900 |
| US | ADAPTIVE CONGESTION CONTROL MECHANISM FOR MODULAR COMPUTER NETWORKS | 09/28/1999 | 5958017 |
| US | METHOD AND APPARATUS FOR COOLING DAUGHTER CARD MODULES | 09/01/1998 | 5801924 |
| US | RAID SYSTEM USING I/O BUFFER SEGMENT TO TEMPORARY STORE STRIPED AND PARITY DATA AND CONNECTING ALL DISK DRIVES VIA A SINGLE TIME MULTIPLEXED NETWORK | 01/19/1999 | 5862313 |
| US | RAID-5 PARITY GENERATION AND DATA RECONSTRUCTION | 09/08/1998 | 5805788 |
| US | DEMOUNTEABLE, COMPLIANT AREA ARRAY INTERCONNECT | 11/07/2000 | 6142789 |
| US | DIAMOND-BASED TRANSFORMERS AND POWER CONVERTERS | 01/30/2001 | 6181231 |
| US | LARGE AREA, MULTI-DEVICE HEAT PIPE FOR STACKED MCM-BASED SYSTEMS | 04/25/2000 | 6055157 |
| US | ADAPTIVE BANDWIDTH SHARING | 03/20/2001 | 6205119 |
| US | SYSTEM AND METHOD FOR STACKING OF INTEGRATED CIRCUIT PACKAGES | 01/09/2001 | 6172874 |
| US | THE FABRICATION OF TEST LOGIC FOR LEVEL SENSITIVE SCAN ON A CIRCUIT | 07/18/2000 | 6092226 |
| US | EMBEDDING A DIGITAL SIGNATURE IN A VIDEO SEQUENCE | 09/28/1999 | 5960081 |
| US | POROUS METAL HEAT SINK | 01/25/2000 | 6018459 |
| US | SERIALIZED RACE-FREE VIRTUAL BARRIER NETWORK | 07/04/2000 | 6085303 |
| US | HYBRID HYPERCUBE/TORUS ARCHITECTURE | 05/08/2001 | 6230252 |
| EP | ROUTER TABLE LOOKUP MECHANISM | 03/06/2002 | 1032887 |
| FR | ROUTER TABLE LOOKUP MECHANISM | 03/06/2002 | 1032887 |
| GB | ROUTER TABLE LOOKUP MECHANISM | 03/06/2002 | 1032887 |
| US | DISTRIBUTED VECTOR ARCHITECTURE | 08/31/1999 | 5946496 |
| US | STOP ALIGN LATERAL MODULE TO MODULE INTERCONNECT | 09/12/2000 | 6116915 |
| US | FLOATING-POINT ADDER PERFORMING FLOATING-POINT AND INTEGER OPERATIONS | 03/04/2003 | 6529928 |
| US | INTERLEAVING MEMORY IN DISTRIBUTED VECTOR ARCHITECTURE MULTIPROCESSOR SYSTEM | 06/15/1999 | 5913069 |
| EP | MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK | 11/24/2004 | 1038375 |
| FR | MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK | 11/24/2004 | 1038375 |
| GB | MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK | 11/24/2004 | 1038375 |
| US | MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK | 07/03/2001 | 6256677 |
| DE | MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK | 11/24/2004 | 69827843.7 |
| US | METHOD AND APPARATUS FOR PARTIAL-SCAN BUILT-IN SELF-TEST LOGIC | 02/19/2002 | 6349398 |
| US | PRECISE DETECTION OF ERRORS USING HARDWARE WATCHPOINT MECHANISM | 11/16/1999 | 5987626 |
| US | METHOD FOR DETERMINING THE OPTIMUM LOCATIONS FOR SCAN LATCHES IN A PARTIAL-SCAN IC BUILT IN SELF TEST SYSTEM | 11/18/2003 | 6651197 |
| US | EIGEN-MODE ENCODING OF SIGNALS IN A DATA GROUP | 05/01/2001 | 6226330 |
| EP | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 07/24/2002 | 1031096 |
| FR | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 07/24/2002 | 1031096 |
| GB | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 07/24/2002 | 1031096 |
| WO | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 07/24/2002 | 1031096 |
| US | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 08/08/2000 | 6101181 |
| DE | VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS | 07/24/2002 | 69806798.3 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | AGE-BASED NETWORK ARBITRATION SYSTEM AND METHOD | 01/06/2004 | 6674720 |
| US | HIGH PERFORMANCE GAS COOLING SYSTEM AND METHOD | 01/02/2001 | 6167947 |
| US | PACKETIZED DATA TRANSMISSIONS IN A SWITCHED ROUTER ARCHITECTURE | 01/10/2006 | 6985484 |
| US | SYSTEM AND METHOD FOR MAINTAINING AND RECOVERING DATA CONSISTENCY IN A DATA BASE PAGE | 01/31/2006 | 6993523 |
| US | SCALABLE HYPERCUBE MULTIPROCESSOR NETWORK FOR MASSIVE PARALLEL PROCESSING | 12/06/2005 | 6973559 |
| US | COMMON USER INTERFACE DEVELOPMENT TOOLKIT | 11/29/2005 | 6971086 |
| US | METHOD AND SYSTEM FOR MAINTAINING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM | 12/27/2005 | 6981101 |
| US | SYSTEM AND METHOD FOR DECOUPLING THE USER INTERFACE AND APPLICATION WINDOW IN A GRAPHICS APPLICATION | 01/10/2006 | 6985149 |
| US | SYSTEM AND METHOD FOR MANAGING GRAPHICS APPLICATIONS | 01/03/2006 | 6982682 |
| US | SYSTEM AND METHOD FOR HIERARCHICAL APPROXIMATION OF LEAST RECENTLY USED REPLACEMENT ALGORITHMS WITHIN A CACHE ORGANIZED AS TWO OR MORE SUPER-WAYS OF MEMORY BLOCKS | 01/10/2006 | 6986001 |
| US | SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL DATA SIGNALS RELATIVE TO A CLOCK | 04/18/2006 | 7031420 |
| US | MULTI-MODE DISPLAY | 03/07/2006 | 7009616 |
| US | METHOD AND APPARATUS FOR RECORDING TRACE DATA IN A MICROPROCESSOR BASED INTEGRATED CIRCUIT | 02/28/2006 | 7007205 |
| US | METHOD AND SYSTEM FOR COVERING MULTIPLE RESOURCES WITH A SINGLE CREDIT IN A COMPUTER SYSTEM | 02/28/2006 | 7007097 |
| US | METHOD AND SYSTEM FOR SPATIALLY COMPOSITING DIGITAL VIDEO IMAGES WITH A TILE PATTERN LIBRARY | 04/11/2006 | 7027072 |
| US | METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR DETERMINING A STRUCTURE OF A GRAPHICS COMPOSITOR TREE | 04/25/2006 | 7034837 |
| US | SYSTEM AND METHOD FOR GENERATING SEQUENCES AND GLOBAL INTERRUPTS IN A CLUSTER OF NODES | 03/21/2006 | 7016998 |
| US | TEXTURE ROAMING VIA DIMENSION ELEVATION | 03/14/2006 | 7012614 |
| US | METHOD AND APPARATUS FOR COMPRESSING AND UNCOMPRESSING IMAGE DATA | 06/06/2006 | 7058218 |
| US | MANAGEMENT AND SCHEDULING OF A DISTRIBUTED RENDERING METHOD AND SYSTEM | 06/13/2006 | 7062527 |
| US | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 06/27/2006 | 7068263 |
| US | PROVIDING SHARED AND NON-SHARED ACCESS TO MEMORY IN A SYSTEM WITH PLURAL PROCESSOR COHERENCE DOMAINS | 06/27/2006 | 7069306 |
| US | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR INTUITIVE INTERACTIVE NAVIGATION CONTROL IN VIRTUAL ENVIRONMENTS | 06/06/2006 | 7058896 |
| US | SYSTEM AND METHOD FOR IMPLEMENTING SHADOWS USING PRE-COMPUTED TEXTURES | 06/20/2006 | 7064755 |
| US | METHOD AND SYSTEM FOR SECURE REMOTE DISTRIBUTED RENDERING | 08/15/2006 | 7092983 |

## Schedule A

| Country | Title | Issue Date | Patent |
|---|---|---|---|
| US | EXTERNAL FAN AND METHOD FOR EXCHANGING AIR WITH MODULAR BRICKS IN A COMPUTER SYSTEM | 08/08/2006 | 7088581 |
| US | SYSTEM AND METHOD FOR ENCODING PAGE SIZE INFORMATION | 08/29/2006 | 7100018 |
| US | ADDRESS TRANSLATION USING A PAGE SIZE TAG | 08/08/2006 | 7089398 |
| US | METHOD AND COMPUTER PROGRAM PRODUCT FOR PRECISE FEEDBACK DATA GENERATION AND UPDATING FOR COMPILE-TIME OPTIMIZATIONS | 10/10/2006 | 7120906 |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| FR | COMPUTER MOUSE | 920381 | 23-Jan-92 | Pending |
| JP | SYSTEM AND METHOD FOR CONDITIONALLY COMPILING A SOFTWARE COMPILATION UNIT | 508759/96 | 02-Aug-95 | Pending |
| DE | SYSTEM AND METHOD FOR CONDITIONALLY COMPILING A SOFTWARE COMPILATION UNIT | 19581754 | 02-Aug-95 | Pending |
| IN | EFFICIENT ULTRA LOW DROPOUT POWER REGULATOR | 891/DEL/96 | 25-Apr-96 | Pending |
| JP | PAGE MIGRATION IN A NON-UNIFORM MEMORY ACCESS (NUMA) SYSTEM | 533568/96 | 03-May-96 | Pending |
| JP | SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS | 533514/1996 | 26-Apr-96 | Pending |
| JP | DUAL IN-LINE MEMORY MODULE (DIMM) | 120502/96 | 15-Jul-96 | Pending |
| CA | DUAL IN-LINE MEMORY MODULE (DIMM) | 2176642 | 15-May-96 | Pending |
| JP | ANTIALIASING OF SILHOUETTE EDGES | 299231/96 | 04-Oct-96 | Pending |
| TW | ANTIALIASING OF SILHOUETTE EDGES | 85112159 | 04-Oct-96 | Pending |
| CN | ANTIALIASING OF SILHOUETTE EDGES | 96112418 | 07-Oct-96 | Pending |
| EP | ANTIALIASING OF SILHOUETTE EDGES | 96307309.3 | 07-Oct-96 | Pending |
| JP | SYSTEM AND METHOD FOR GENERATING AND DISPLAYING COMPLEX GRAPHIC IMAGES AT A CONSTANT FRAME RATE | 533497/97 | 21-Mar-97 | Pending |
| DE | SYSTEM AND METHOD FOR GENERATING AND DISPLAYING COMPLEX GRAPHIC IMAGES AT A CONSTANT FRAME RATE | 97916723.6 | 21-Mar-97 | Pending |
| EP | SYSTEM AND METHOD FOR GENERATING AND DISPLAYING COMPLEX GRAPHIC IMAGES AT A CONSTANT FRAME RATE | 97916723.6 | 21-Mar-97 | Pending |
| GB | SYSTEM AND METHOD FOR GENERATING AND DISPLAYING COMPLEX GRAPHIC IMAGES AT A CONSTANT FRAME RATE | 97916723.6 | 21-Mar-97 | Pending |
| JP | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 0446-96 | 22-Nov-96 | Pending |
| EP | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 561718 | 22-Nov-95 | Pending |
| TW | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 85114447 | 22-Nov-96 | Pending |
| CN | HIGH PERFORMANCE LOW COST VIDEO GAME SYSTEM WITH COPROCESSOR PROVIDING HIGH SPEED EFFICIENT 3D GRAPHICS AND DIGITAL AUDIO SIGNAL PROCESSING | 96121757.X | 22-Nov-96 | Pending |
| JP | RESTORATION FILTER FOR TRUNCATED PIXELS | 0446-JP | 21-Nov-96 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| EP | RESTORATION FILTER FOR TRUNCATED PIXELS | 96308414 | 21-Nov-96 | Pending |
| JP | SYSTEM AND METHOD FOR MERGING PIXEL FRAGMENTS BASED ON DEPTH RANGE VALUES | 96352108 | 21-Nov-96 | Pending |
| CA | COMPRESSION AND DECOMPRESSION SCHEME PERFORMED ON SHARED WORKSTATION MEMORY BY MEDIA COPROCESSOR | 2259513 | 03-Jul-97 | Pending |
| EP | PACKET SWITCHED ROUTER ARCHITECTURE FOR PROVIDING MULTIPLE SIMULTANEOUS COMMUNICATIONS | 97937252.1 | 14-Aug-97 | Pending |
| WO | SYNCHRONIZATION INFRASTRUCTURE FOR USE IN A COMPUTER SYSTEM | US97/14652 | 19-Aug-97 | Pending |
| JP | SYNCHRONIZATION INFRASTRUCTURE FOR USE IN A COMPUTER SYSTEM | 514672/1998 | 19-Aug-97 | Pending |
| EP | SYNCHRONIZATION INFRASTRUCTURE FOR USE IN A COMPUTER SYSTEM | 97938461.7 | 19-Aug-97 | Pending |
| US | SYSTEM PROVIDING EXTENSIBLE CONTENT PROCESSING AND INSTALLATION IN A DISTRIBUTED MULTIMEDIA ASSET MANAGEMENT SYSTEM | 938707 | 26-Sep-97 | Pending |
| JP | SYSTEM AND METHOD FOR HIGH-SPEED EXECUTION OF GRAPHICS APPLICATION PROGRAMS INCLUDING SHADING LANGUAGE INSTRUCTIONS | 100077481 | 08-Apr-99 | Pending |
| US | DISPLAY SYSTEM HAVING FLOATING POINT RASTERIZATION AND FLOATING POINT FRAME BUFFERING | 09/614363 | 12-Jul-00 | Pending |
| US | METHOD AND APPARATUS FOR COMPRESSING AND UNCOMPRESSING IMAGE DATA | 10/674825 | 01-Oct-03 | Pending |
| US | A METHOD TO ENABLE THE USE OF MORE DEVICES AND HIGHER BUS SPEEDS BY REDUCING DEVICE LOADING ON A PCI BUS | 09/315806 | 21-May-99 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING A WIDE ASPECT RATIO FLAT PANEL DISPLAY MONITOR INDEPENDENT WHITE-BALANCE ADJUSTMENT AND GAMMA CORRECTION CAPABILITIES | 10/650030 | 25-Aug-03 | Allowed |
| US | CAMABLE, BLIND MATE/DEMATE OPTICAL EDGE CONNECTOR | 09/549980 | 14-Apr-00 | Pending |
| DE | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | US00/25596 | 19-Sep-00 | Pending |
| FR | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | US00/25596 | 19-Sep-00 | Pending |
| GB | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | US00/25596 | 19-Sep-00 | Pending |
| JP | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | 2001-532400 | 19-Sep-00 | Pending |
| US | MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN | 10/696146 | 29-Oct-03 | Pending |
| US | NODE TRANSLATION AND PROTECTION IN A CLUSTERED MULTIPROCESSOR SYSTEM | 10/020854 | 14-Dec-01 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| US | DISPLAY CAPABLE OF DISPLAYING IMAGES IN RESPONSE TO SIGNALS OF A PLURALITY OF SIGNAL FORMATS | 10/626576 | 25-Jul-03 | Allowed |
| US | COMPENSATED CANCELLER AND EQUALIZER FOR SIMULTANEOUS BI-DIRECTIONAL COMMUNICATIONS IN A COMPUTING SYSTEM | 09/441774 | 17-Nov-99 | Pending |
| US | METHOD AND SYSTEM FOR RENAMING REGISTERS IN A MICROPROCESSOR | 10/210257 | 31-Jul-02 | Pending |
| US | METHOD AND SYSTEM FOR DISTRIBUTED RENDERING | 09/609046 | 30-Jun-00 | Pending |
| US | BACKSHELL ASSEMBLY | 10/205877 | 24-Jul-02 | Allowed |
| US | SYSTEM AND METHOD FOR A HIERARCHICAL SYSTEM MANAGEMENT ARCHITECTURE OF A HIGHLY SCALABLE COMPUTING SYSTEM | 09/644698 | 24-Aug-00 | Pending |
| WO | METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM | US00/25832 | 19-Sep-00 | Pending |
| JP | MODULAR COMPUTING ARCHITECTURE HAVING COMMON COMMUNICATION INTERFACE | 2001-526717 | 29-Sep-00 | Pending |
| EP | MODULAR COMPUTING ARCHITECTURE HAVING COMMON COMMUNICATION INTERFACE | 967100.9 | 29-Sep-00 | Pending |
| JP | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 2001-526730 | 29-Sep-00 | Pending |
| US | MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD | 10/868181 | 15-Jun-04 | Pending |
| WO | NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM | US00/27024 | 29-Sep-00 | Pending |
| JP | NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM | 2001-526728 | 29-Sep-00 | Pending |
| EP | NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM | 967199.1 | 29-Sep-00 | Pending |
| WO | CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY | 25296 | 14-Sep-00 | Pending |
| DE | CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY | 965033.4 | 14-Sep-00 | Pending |
| FR | CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY | 965033.4 | 14-Sep-00 | Pending |
| GB | CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY | 965033.4 | 14-Sep-00 | Pending |
| JP | METHOD AND APPARATUS FOR PROCESSING ERRORS IN A COMPUTER SYSTEM | 2001-526709 | 20-Sep-00 | Pending |
| US | METHOD AND SYSTEM FOR MINIMIZING AN AMOUNT OF DATA NEEDED TO TEST DATA AGAINST SUBAREA BOUNDARIES IN SPATIALLY COMPOSITED DIGITAL VIDEO | 10/058050 | 29-Jan-02 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| US | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING | 09/629458 | 31-Jul-00 | Pending |
| US | MAINTAINING MEMBERSHIP IN HIGH AVAILABILITY COMPUTING SYSTEMS | 09/811158 | 16-Mar-01 | Pending |
| US | COMMON USER INTERFACE DEVELOPMENT TOOLKIT FOR A SYSTEM ADMINISTRATION PROGRAM | 11/224376 | 12-Sept.-2005 | Pending |
| US | SYSTEM AND METHOD FOR RETROFITTING A PROCESSOR INTO A SYSTEM DESIGNED FOR ANOTHER PROCESSOR | 09/648150 | 25-Aug-00 | Pending |
| US | ADDRESS-SELECTED ATTRIBUTE ENCODING AND BYTE-SWAPPING | 09/648902 | 25-Aug-00 | Pending |
| US | AN INTERFACE FOR SYNCHRONOUS DATA TRANSFER BETWEEN DOMAINS CLOCKED AT DIFFERENT FREQUENCIES | 09/621315 | 20-Jul-00 | Pending |
| US | METHOD AND APPARATUS FOR COMMUNICATING COMPUTER DATA FROM ONE POINT TO ANOTHER OVER A COMMUNICATIONS MEDIUM | 09/620373 | 20-Jul-00 | Pending |
| US | QUEUE CIRCUIT AND METHOD FOR MEMORY ARBITRATION EMPLOYING SAME | 09/909704 | 20-Jul-01 | Pending |
| US | SYSTEM AND METHOD FOR REMOVING DATA FROM PROCESSOR CACHES IN A DISTRIBUTED MULTIPROCESSOR COMPUTER SYSTEM | 09/909700 | 20-Jul-01 | Pending |
| WO | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | US01/48111 | 10-Dec-01 | Pending |
| KR | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 2003-7007593 | 05-Jun-03 | Pending |
| JP | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 2002-548993 | 10-Dec-01 | Pending |
| EP | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 1990159.4 | 19-May-03 | Pending |
| US | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | | 07-Feb-05 | Pending |
| US | METHOD AND SYSTEM FOR MINIMIZING AN AMOUNT OF DATA NEEDED TO COMMUNICATE TILE INFORMATION IN SPATIALLY COMPOSITED DIGITAL VIDEO | 09/689784 | 13-Oct-00 | Pending |
| US | METHOD AND SYSTEM FOR SPATIALLY COMPOSITING DIGITAL VIDEO IMAGES WITH COARSE TILES | 09/689786 | 13-Oct-00 | Pending |
| US | FLEXIBLE FAILOVER POLICIES IN HIGH AVAILABILITY COMPUTING SYSTEMS | 09/997404 | 29-Nov-01 | Pending |
| US | APPARATUS AND METHOD FOR CONTROLLING THE FLOW AND ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS | 09/910587 | 21-Jul-01 | Pending |
| US | METHOD AND SYSTEM FOR PRESENTING THREE-DIMENSIONAL COMPUTER GRAPHICS USING MULTIPLE GRAPHICS PROCESSING UNITS | 09/888438 | 26-Jun-01 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| US | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REAL TIME TRANSPARENCY-BASED COMPOSITING | 10/145110 | 15-May-02 | Pending |
| US | SYSTEM FOR SYNCHRONIZING DISPLAY OF IMAGES IN A MULTI-DISPLAY COMPUTER SYSTEM | 10/695779 | 30-Oct-03 | Pending |
| US | TRANSPARENT DISTRIBUTION AND EXECUTION OF DATA IN A MULTIPROCESSOR ENVIRONMENT | 09/934443 | 20-Aug-01 | Pending |
| US | SNAPSHOT COPY OF DATA VOLUME DURING DATA ACCESS | 10/682841 | 10-Oct-03 | Pending |
| US | RELOCATION OF METADATA SERVER WITH OUTSTANDING DMAPI REQUESTS | 10/620387 | 17-Jul-03 | Pending |
| US | RECOVERY AND RELOCATION OF A DISTRIBUTED NAME SERVICE IN A CLUSTERED FILE SYSTEM | 10/345357 | 16-Jan-03 | Pending |
| US | FAILURE HIERARCHY IN A CLUSTER FILESYSTEM | 10/345371 | 16-Jan-03 | Pending |
| US | MESSAGING BETWEEN HETEROGENEOUS CLIENTS OF A STORAGE AREA NETWORK | 10/414245 | 16-Apr-03 | Pending |
| US | FAILSAFE OPERATION OF STORAGE AREA NETWORK | 10/414238 | 16-Apr-03 | Pending |
| US | CLUSTERED FILESYSTEM FOR MIX OF TRUSTED AND UNTRUSTED NODES | 10/414239 | 16-Apr-03 | Pending |
| US | MULTI-CLASS HETEROGENEOUS CLIENTS IN A CLUSTERED FILESYSTEM | 10/414236 | 16-Apr-03 | Pending |
| US | SYSTEM AND METHOD FOR COMMUNICATING IMAGE DATA USING ERROR CORRECTION CODING | 10/137026 | 30-Apr-02 | Pending |
| US | DEVICES FOR MONITORING DIGITAL VIDEO SIGNALS AND ASSOCIATED METHODS AND SYSTEMS | 10/429257 | 05-May-03 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING INTERACTIVE IMAGES | 10/112430 | 29-Mar-02 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING COLLABORATION OF A GRAPHICS SESSION | 10/112366 | 29-Mar-02 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING INTERFRAME COMPRESSION IN A GRAPHICS SESSION | 10/109835 | 29-Mar-02 | Pending |
| US | SYSTEM AND METHOD FOR DISCARDING FRAMES OF AN IMAGE DURING TRANSPORT ACROSS A NETWORK LINK | 10/112392 | 29-Mar-02 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING DYNAMIC CONTROL OF A GRAPHICS SESSION | 10/112345 | 29-Mar-02 | Pending |
| US | METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR BLENDING TEXTURES IN A TEXTURE PAGING SCHEME | 10/425735 | 30-Apr-03 | Pending |
| US | SYSTEM AND METHOD FOR MANAGING GRAPHICS APPLICATIONS | 10/208123 | 29-Jul-02 | Allowed |
| US | AN OPERATING SYSTEM SECURE SCHEDULAR | 11/079409 | 15-Mar-05 | Pending |
| US | SYSTEM AND METHOD FOR MANAGING GRAPHICS APPLICATIONS | 10/207940 | 29-Jul-02 | Pending |
| WO | METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR | US02/05779 | 28-Feb-02 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| JP | METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR | 2003-573550 | 28-Feb-02 | Pending |
| EP | METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR | 2721164.8 | 28-Feb-02 | Pending |
| US | SYNCHRONIZATION CIRCUITS FOR THE DISTRIBUTION OF UNIQUE DATA TO SCATTERED LOCATIONS | 10/356236 | 31-Jan-03 | Pending |
| US | MULTIPROCESSOR NETWORK MULTICASTING AND GATHERING | 10/607163 | 26-Jun-03 | Pending |
| JP | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | | 26-Jun-03 | Pending |
| KR | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | | 26-Jun-03 | Pending |
| TW | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | | 26-Jun-03 | Pending |
| WO | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | US03/20311 | 26-Jun-03 | Pending |
| EP | SYSTEM AND METHOD FOR SELF-CALIBRATING SENSE AMPLIFIER STROBE | 3742265.6 | 26-Jun-03 | Pending |
| US | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR APPLYING DIFFERENT TRANSPORT MECHANISMS FOR USER INTERFACE AND IMAGE PORTIONS OF A REMOTELY RENDERED IMAGE | 10/426003 | 30-Apr-03 | Pending |
| US | SYSTEM AND METHOD FOR CONVEYING INFORMATION | 10/310237 | 04-Dec-02 | Pending |
| US | SYSTEM AND METHOD FOR ALLOCATING COMPUTING RESOURCES | 10/174718 | 18-Jun-02 | Allowed |
| WO | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR NEAR-REAL TIME LOAD BALANCING ACROSS MULTIPLE RENDERING PIPELINES | US03/040253 | 18-Dec-03 | Pending |
| EP | REAL-TIME STORAGE AREA NETWORK | | 09-May-03 | Pending |
| JP | REAL-TIME STORAGE AREA NETWORK | | 09-May-03 | Pending |
| WO | REAL-TIME STORAGE AREA NETWORK | US03/14637 | 09-May-03 | Pending |
| US | REAL-TIME STORAGE AREA NETWORK | 10/434340 | 09-May-03 | Pending |
| US | EMI CABLE BACKSHELL ASSEMBLY FOR HIGH-DENSITY INTERCONNECT | 10/235221 | 05-Sep-02 | Pending |
| US | SYSTEM AND METHOD FOR CONVEYING INFORMATION | 10/310400 | 04-Dec-02 | Pending |
| US | SYSTEM AND METHOD FOR IMAGE-BASED RENDERING WITH OBJECT PROXIES | 10/197845 | 19-Jul-02 | Pending |
| US | GLOBAL POINTERS FOR SCALABLE PARALLEL APPLICATIONS | 10/365658 | 13-Feb-03 | Pending |
| US | DETECTION AND CONTROL OF RESOURCE CONGESTION BY A NUMBER OF PROCESSORS | 10/631988 | 31-Jul-03 | Pending |
| US | NETWORK FILESYSTEM ASYNCHRONOUS I/O SCHEDULING | 10/620797 | 11-Jul-03 | Pending |
| US | METHOD FOR EQUITABLE RESOURCE SHARING BETWEEN LOCAL AND NETWORK FILESYSTEMS | 10/620835 | 17-Jul-03 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| US | SYSTEM AND METHOD FOR NETWORKED COMPUTER GRAPHICS | 10/899316 | 27-Jul-04 | Pending |
| US | A METHOD AND APPARATUS FOR MAINTAINING COHERENCE INFORMATION IN MULTI-CACHE SYSTEMS | 10/785575 | 24-Feb-04 | Pending |
| US | MEMORY ACCESS MANAGEMENT IN A SHARED MEMORY MULTIPROCESSOR SYSTEM | 10/687196 | 16-Oct-03 | Allowed |
| US | METHOD FOR PERFORMING CACHE COHERENCY IN A COMPUTER SYSTEM | 10/837057 | 30-Apr-04 | Pending |
| WO | SYSTEM AND METHOD FOR PERFORMING ADDRESS TRANSLATION IN A COMPUTER SYSTEM | US2004/013485 | 30-Apr-04 | Pending |
| US | SYSTEM AND METHOD FOR PERFORMING ADDRESS TRANSLATION IN A COMPUTER SYSTEM | 10/835855 | 30-Apr-04 | Pending |
| US | SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS IN A COMPUTING SYSTEM | 10/836932 | 30-Apr-04 | Pending |
| US | HOT PLUG-INS IN A PCI SYSTEM BUS | 11/235493 | 26-Sept.-2005 | Pending |
| US | FAULT TOLERANT MEMORY SYSTEM | 11/136260 | 24-May-05 | Pending |
| US | SYSTEM AND METHOD FOR GRAPHICS CULLING | 11/043038 | 27-Jan-05 | Pending |
| US | METHOD AND SYSTEM FOR CONTROLLING UTILISATION OF A FILE SYSTEM | 10/912722 | 06-Aug-04 | Pending |
| US | GENERATING SUBDIVISION SURFACES ON A GRAPHICS HARDWARE WITH FLOATING-POINT FRAGMENT SHADERS | 11/182900 | 02-Feb-06 | Pending |
| US | SYSTEM AND METHOD FOR PROVIDING DYNAMIC COMPRESSION CONTROL OF A GRAPHICS SESSION | 11/049111 | 2-Feb.-2005 | Pending |
| US | METHOD AND APPARATUS FOR PROCESSING PRIMITIVE DATA FOR POTENTIAL DISPLAY ON A DISPLAY DEVICE | 10/715882 | 18-Nov-03 | Pending |
| WO | PRIMITIVE CULLING APPARATUS AND METHOD | US2004/37655 | 10-Nov-04 | Pending |
| US | DISTRIBUTED GRAPHICS PROCESSING APPARATUS AND METHOD | 11/027752 | 30-Dec-04 | Pending |
| US | A METHOD OF DATA PACKET TRANSMISSION | 10/982149 | 05-Nov-04 | Pending |
| US | SYSTEM AND METHOD FOR SYNCHRONIZING DISTRIBUTION OF TRANSACTION OPERATIONS IN A COMPUTER SYSTEM | 10/976531 | 29-Oct-04 | Pending |
| US | COMPOSITING IMAGES USING LOGICALLY DIVIDED OBJECT SPACE | 11/091237 | 28-Mar-05 | Pending |
| US | NODE SYNCHRONIZATION FOR MULTI-PROCESSOR COMPUTER SYSTEMS | 11/113805 | 25-Apr-05 | Pending |
| US | SYSTEM AND METHOD FOR REDUCING BACK FLOW | | 31-Jan-05 | Pending |
| US | ANTICIPATORY PROGRAMMABLE INTERFACE PRE-DRIVER | 11/116734 | 28-Apr-05 | Pending |
| US | LIQUID DIMM COOLER | 11/121975 | 04-May-05 | Pending |
| US | PREDICTIVE PREFAULTING IN THE PAGE FAULT HANDLER | 11/218868 | 2-Sept.-2005 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| JP | APPARATUS FOR CALCULATING DELAY WHEN EXECUTING VECTOR TAILGATING INSTRUCTIONS AND USING DELAY TO FACILITATE SIMULTANEOUS READING OF OPERANDS FROM AND WRITING OF RESULTS TO SAME VECTOR REGISTER | 2000-055714 | 31-Mar-00 | Pending |
| US | A SCALABLE PARALLEL VECTOR COMPUTER SYSTEM | 523540 | 05-Sep-95 | Pending |
| JP | SOLID STATE STORAGE DEVICE | 6-500733 | 26-May-93 | Pending |
| JP | METHOD & APPARATUS FOR A SPECIAL PURPOSE BOOLEAN UNIT | 515589/91 | 10-Jun-91 | Pending |
| DE | METHOD FOR EFFICIENT NON-VIRTUAL MAIN MEMORY MANAGEMENT | 91911776.2 | 10-Jun-91 | Pending |
| DE | SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL | 95905963.5 | 09-Dec-94 | Pending |
| EP | SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL | 95905963.5 | 09-Dec-94 | Pending |
| FR | SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL | 95905963.5 | 09-Dec-94 | Pending |
| GB | SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL | 95905963.5 | 09-Dec-94 | Pending |
| US | SPATIAL DERIVATIVE BUS ENCODER AND DECODER | 10/171095 | 13-Jun-02 | Allowed |
| JP | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 2003-356594 | 23-Sep-96 | Pending |
| JP | VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL | 517327/1997 | 23-Sep-96 | Allowed |
| DE | MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE | 98961737.8 | 17-Nov-98 | Pending |
| EP | MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE | 98961737.8 | 17-Nov-98 | Pending |
| FR | MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE | 98961737.8 | 17-Nov-98 | Pending |

## Schedule A

| Country | Title | App. No. | File Date | Status |
|---|---|---|---|---|
| GB | MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE | 98961737.8 | 17-Nov-98 | Pending |
| US | HYBRID HYPERCUBE/TORUS ARCHITECTURE | 192955 | 17-Nov-98 | Pending |
| US | NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM | 11/295,676 | 12/06/2005 | Pending |
| US | METHOD AND SYSTEM FOR MAINTAINING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM | | 01/03/2006 | Pending |
| PCT | PRIMITIVE CULLING APPARATUS AND METHOD | PCT/US2005/39012 | 10/26/2005 | Pending |
| US | SYSTEM AND METHOD FOR SYNCHRONIZING DISTRIBUTION OF TRANSACTION OPERATIONS IN A COMPUTER SYSTEM | | 10/31/2005 | Pending |
| US | FULL DUPLEX TELE-IMMERSION INCLUDING DESTOP PSEUDO-IMMERSIVE USER INTERFACE | 11/255,920 | 10/24/2005 | Pending |
| US | MEDIAFUSION | 60/735,962 | 11/14/2005 | Pending |
| US | SYSTEM FOR INSERTION AND EXTRACTION OF AN ELECTRONIC MODULE | 11/261,045 | 10/28/2005 | Pending |
| US | NEW SCALABLE DIRECTORY SCHEME FOR VERY LARGE SHARED MEMORY COMPUTER SYSTEMS. | 11/268,493 | 11/07/2005 | Pending |
| US | FAIL-SOFT CAPABILITY FOR IRIX CPU SETS | 11/334,526 | 01/19/2006 | Pending |
| US | INSTANTANEOUS CHECKPOINTS BY TLB | 11/340,486 | 01/27/2006 | Pending |
| US | SYSTEM LEVEL FLAW TABLES FOR MEMORY FOR INCREASED FAULT-TOLERANCE WHILE REDUCING SERVICE REQUIREMENTS | 12/30/2005 | Not yet assigned | Pending |
| US | MECHANISM FOR MAINTAINING ACCURATE GLOBAL REAL TIME CLOCK IN ANY ARBITRARY DISTRIBUTED SYSTEM WITH DYNAMIC PARTITIONS AND UNRELIABLE NETWORKS | | | Pending |
| US | USE OF RAY-TRACING FOR GENERATING IMAGES FOR AUTO-STEREO DISPLAYS | 12/29/2005 | Not yet assigned | Pending |
| US | SYSTEM FOR GENERATING SYNCHRONIZED EVENTS AND IMAGES | 11/340,579 | 27-Jan-06 | Pending |
| US | SYSTEM AND METHOD FOR MANAGING GRAPHICS APPLICATIONS | 11/324,684 | 03-Jan-06 | Pending |
| US | FLEXISCAPE | 11/368,452 | 07-Mar-06 | Pending |
| US | MEDIAFUSION | 11/368,625 | 07-Mar-06 | Pending |
| US | APPLICATION FUSION | 11/368,451 | 07-Mar-06 | Pending |
| US | SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL DATA SIGNALS RELATIVE TO A CLOCK | 11/405,387 | 17-Apr-06 | Pending |
| US | SYSTEM AND METHOD FOR REDUCING BACK FLOW | 11/343,968 | 31-Jan-06 | Pending |
| US | PREFETCHING HINTS | 11/365,280 | 28-Feb-06 | Pending |
| US | | 11/464,148 | 11-Aug-06 | Pending |
| US | PRIMITIVE CULLING APPARATUS AND METHOD | 11/490,505 | 06-00-06 | Pending |

**Schedule A**

| Country | Title | Issue Date | Patent | Status |
|---|---|---|---|---|
| US | BRACKET FOR CPU DAUGHTER CARD | 11/14/1995 | 5465934 | Expired |
| | | | | |

| Country | Title | App No. | File Date | Status |
|---|---|---|---|---|
| US | COMPACT FLAT PANEL COLOR CALIBRATION SYSTEM | 11/426469 | 26-June-06 | Pending |
| | | | | |