PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.	09/25/2007

RECEIVING PARTY DATA

Name:	MARVELL INTERNATIONAL TECHNOLOGY LTD.
Street Address:	Canon's Court, 22 Victoria Street
City:	Hamilton
State/Country:	BERMUDA
Postal Code:	Hm12

PROPERTY NUMBERS Total: 15

Property Type	Number
Application Number:	09917972
Application Number:	10327173
Application Number:	10788074
Application Number:	10696811
Application Number:	10903560
Application Number:	10826886
Application Number:	10994011
Application Number:	10995987
Application Number:	10938098
Application Number:	10945735
Application Number:	10941859
Application Number:	11377108
Application Number:	11416840
Application Number:	11352167
Application Number:	11391625

CH $600.00 09917972

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	115753
NAME OF SUBMITTER:	Kevin T. LeMond

Total Attachments: 5
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EXHIBIT A

AVAGOTECH ASSIGNMENT

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD., (Company Registration No. 200512430D) a company incorporated under the laws of Singapore ("Assignor") hereby sells, assigns, conveys and transfers to MARVELL INTERNATIONAL TECHNOLOGY LTD., a corporation organized under the laws of Bermuda having its registered office at Canon's Court, 22 Victoria Street, Hamilton HM 12, Bermuda ("Assignee"), its successors, and assigns, all of Assignor's right, title and interest in and to the inventions and improvements which are the subject of the patent and applications listed in Attachment A ("AvagoTech Patents"), including any patents issuing from or based upon all patent applications thereon, or any continuations, continuations-in-part, divisionals, reissues, re-examinations or extensions of the AvagoTech Patents, the same to be held by Assignee for Assignee's own use and enjoyment, and for the use and enjoyment of Assignee's successors, assigns and other legal representatives, to the full end term for which patents are granted, as fully and entirely as the same would have been held and enjoyed by Assignor if this Assignment had not been made, and all claims for damages and other remedies for past, present and future infringement of the AvagoTech Patents, along with the right to sue for and collect such damages and other remedies for the use and benefit of Assignee and its successors, assigns and other legal representatives.

DATE: 9/25/07

ASSIGNOR

AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.

By: _____

Name: Floyd E. Anderson

Title: Chief Patent Counsel

DATE: _____

ASSIGNEE

MARVELL INTERNATIONAL TECHNOLOGY LTD.

By: _____

Name: CAROL FEATHERS

Title: GENERAL MANAGER.

REVIEWED

MARVELL SEMICONDUCTOR, INC.

ATTACHMENT A

AVAGO PATENTS

CaseNumber	SubCase	AppTitle	AppNumber	FilDate	Pub#	PubDate	Country
10010393	07	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit					DE
10010393	03	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	02003915.2	15-Apr-02	1282041	22-Oct-03	EP
10010393	08	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit					FR
10010393	09	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit					GB
10010393	02	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	P2002-214658	24-Jul-02	2003-11426	18-Apr-03	JP
10010393	04	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	2002-0044561	29-Jul-02			KR
10010393	05	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	200201116-1	28-Feb-02	0094870	18-Mar-03	SG

10010393	06	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	91103450	26-Feb-02			TW
10010393	01	Built-In Self-Test Using Embedded Memory And Processor In An Application Specific Integrated Circuit	09/917972	30-Jul-01	0023914	30-Jan-03	US
10021148	03	A Method Of Field Upgradeable Boot Code	10348328.4	17-Oct-03	10348328	15-Jul-04	DE
10021148	04	A Method Of Field Upgradeable Boot Code	0325607.0	03-Nov-03	2396452	23-Jun-04	GB
10021148	02	A Method Of Field Upgradeable Boot Code	P2003-422115	19-Dec-03	2004206715	22-Jul-04	JP
10021148	01	A Method Of Field Upgradeable Boot Code	10/327173	20-Dec-02	0123089	24-Jun-04	US
10030806	03	Parallel Video Processing Architecture	102004051390.2	21-Oct-04	102004051390	22-Sep-05	DE
10030806	02	Parallel Video Processing Architecture	P2005-045382	22-Feb-05	2005243022	08-Sep-05	JP
10030806	01	Parallel Video Processing Architecture	10/788074	25-Feb-04	0185221	25-Aug-05	US
10030825	03	Fixed Frequency Clock Output Having A Variable High Frequency Input Clock And An Unrelated Fixed Frequency Reference Signal	102004033105.7	08-Jul-04	102004033105	09-Jun-05	DE
10030825	02	Fixed Frequency Clock Output Having A Variable High Frequency Input Clock And An Unrelated Fixed Frequency Reference Signal	P2004-318340	01-Nov-04	2005167994	23-Jun-05	JP
10030825	01	Fixed Frequency Clock Output Having A Variable High Frequency Input Clock And An Unrelated Fixed Frequency Reference Signal	10/696811	30-Oct-03	0093583	05-May-05	US

10030831	03	A Modulated Video Waveform Generator	102005011858.5	15-Mar-05			DE
10030831	02	A Modulated Video Waveform Generator	P2005-215634	26-Jul-05			JP
10030831	01	A Modulated Video Waveform Generator	10/903560	29-Jul-04	0023250	02-Feb-06	US
10031196	03	A Programmable I/O Interface	1002005004420.4	31-Jan-05	102005004420	10-Nov-05	DE
10031196	02	A Programmable I/O Interface	P2005-108430	05-Apr-05			JP
10031196	01	A Programmable I/O Interface	10/826886	15-Apr-04	0235096	20-Oct-05	US
10040804	01	Method And Apparatus For DMA-Generated Memory Write-Back	10/994011	19-Nov-04			US
10040805	01	Method And Apparatus For Intervaled DMA Transfer Access	10/995987	19-Nov-04	2006-0123158-A1	08-Jun-06	US
10040840	01	Method And Apparatus For Image Processing	10/938098	10-Sep-04	0056725	16-Mar-06	US
10040841	01	Method And Apparatus For Image Processing	10/945735	20-Sep-04	0061827	23-Mar-06	US
10040842	01	An Image Processing Method And Device	10/941859	16-Sep-04	0056738	16-Mar-06	US
10050684	01	Small Circuit For Complex IP On-Chip Functional Verification, Testing And Demonstration	11/377108	15-Mar-06			US
10051034	01	System And Method For Routing Signals Between Side-By-Side Die In Lead Frame Type System In A Package (SIP) Devices	11/416840	03-May-06			US
10051066	01	System And Method For Routing Supply Voltages Or Other Signals Between Side-By-Side Die And A Lead Frame	11/352167	10-Feb-06			US

		For System In A Package (SIP) Devices					
10051164	01	On-Die Bond Wires Enhance Routability Of One-Layer RDL	11/391625	27-Mar-06			US
10060108		Programmable Scan Data Capture And Output					