

PATENT ASSIGNMENT

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| Name | Execution Date |
| Ramtron International Corporation and Enhanced Memory Systems, Inc. | 04/13/2004 |
| RECEIVING PARTY DATA | |
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| PROPERTY NUMBERS Total: 2 | |
| Property Type | Number |
| Application Number: | 11238182 |
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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **Ramtron International Corporation** and **Enhanced Memory Systems, Inc.**, each having offices at 1850 Ramtron Drive, Colorado Springs, Colorado 80921 (*together, "Assignor"*), do hereby sell, assign, transfer and convey unto **Purple Mountain Server LLC**, a Delaware limited liability company, having an office at 171 Main Street, #271, Los Altos, California 94022 (*"Assignee"*) or its designees, all of Assignor's right, title and interest in and to: the patent applications and patents listed below, any patents, registrations, or certificates of invention issuing on any patent applications listed below, the inventions disclosed in any of the foregoing, any and all counterpart United States, international and foreign patents, applications and certificates of invention based upon or covering any portion of the foregoing, and all reissues, re-examinations, divisionals, renewals, extensions, provisionals, continuations and continuations-in-part of any of the foregoing (collectively "*Patent Rights*"):

| <u>Patent or Application No.</u> | <u>Country</u> | <u>Filing Date</u> | <u>Assignor</u> | <u>Title Inventor(s)</u> |
|----------------------------------|----------------|--------------------|-----------------|---|
| Pat. 5,104,822 (RAM 317) | U.S. | 07/30/1990 | RAM | Method For Creating Self-Aligned, Non-Patterned Contact Areas And Stacked Capacitors Using The Method Butler |
| Pat. 5,162,890 (RAM 317 DIV) | U.S. | 04/05/1991 | RAM | Stacked Capacitor With Sidewall Insulation Butler |
| Pat. 2673615 (RAM 317 JPN) | Japan | 07/30/1991 | RAM | Method For Creating Self-Aligned, Non-Patterned Contact Areas And Stacked Capacitors Using The Method Butler |
| Pat. 5,170,242 (RAM 319 CON) | U.S. | 05/10/1991 | RAM | Reaction Barrier For A Multilayer Structure In An Integrated Circuit Stevens, Maekawa |
| Pat. 2075540 (RAM 319 JPN) | Japan | 07/13/1990 | RAM | Reaction Barrier For A Multilayer Structure In An Integrated Circuit Stevens, Maekawa |
| Pat. 5,075,817 (RAM 320) | U.S. | 6/22/1990 | RAM | Trench Capacitor For Large Scale Integrated Memory Butler |
| Pat. 2089169 (RAM 320 JPN) | Japan | 06/21/1991 | RAM | Trench Capacitor For Large Scale Integrated Memory Butler |

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|---------------------------------|---------|------------|-----|---|
| Pat. 5,610,099 (RAM 321) | U.S. | 06/28/1994 | RAM | Process For Fabricating Transistors Using Composite Nitride Structure Stevens, Bailey, Taylor |
| Pat. 5,043,790 (RAM 322) | U.S. | 04/05/1990 | RAM | Sealed Self Aligned Contacts Using Two Nitrides Process Butler |
| Pat. 5,216,281 (RAM 322 CIP) | U.S. | 08/26/1991 | RAM | Sealed Self Aligned Contact Incorporating A Dopant Source Butler |
| Pat. 2005865 (RAM 322 JPN) | Japan | 04/05/1991 | RAM | Sealed Self Aligned Contacts Using Two Nitrides Process Butler |
| Pat. 5,134,310 (RAM 324) | U.S. | 01/23/1991 | RAM | Current Supply Circuit For Driving High Capacitance Load In An Integrated Circuit Mobley, Eaton |
| Pat. 2932122 (RAM 324 JPN) | Japan | 01/23/1992 | RAM | Current Supply Circuit For Driving High Capacitance Load In An Integrated Circuit Mobley, Eaton |
| Pat. 5,117,177 (RAM 325) | U.S. | 01/23/1991 | RAM | Reference Generator For An Integrated Circuit Eaton |
| Pat. 3106216 (RAM 325 JPN) | Japan | 01/23/1992 | RAM | Reference Generator For An Integrated Circuit Eaton |
| Pat. 5,255,222 (RAM 326) | U.S. | 01/23/1991 | RAM | Output Control Circuit Having Continuously Variable Drive Current Eaton |
| Pat. 3136424 (RAM 326 JPN) | Japan | 01/22/1992 | RAM | Output Control Circuit Having Continuously Variable Drive Current Eaton |
| Pat. 5,699,317 (RAM 343 CIP) | U.S. | 10/06/1994 | EMS | Enhanced Dram With All Reads From On-Chip Cache And All Writes To Memory Array Mobley, Sartore, Carrigan, Jones |
| Pat. 5,721,862 (RAM 343 CON) | U.S. | 06/02/1995 | EMS | Enhanced Dram With Single Row SRAM Cache For All Device Read Operations Mobley, Sartore, Carrigan, Jones |
| Pat. 69324508.5 (RAM 343 DE) | Germany | 01/14/1993 | EMS | Edram With Embedded Registers Mobley, Sartore, Carrigan, Jones |

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| Pat. 5,887,272 (RAM 343 DIV) | U.S. | 07/03/1997 | EMS | Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones |
| Pat. 6,347,357 (RAM 343 DIV/CON) | U.S. | 10/30/1998 | EMS | Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones |
| App. 09/962,287 (RAM 343 DIV/CN2) | U.S. | 09/24/2001 | EMS | Enhanced Dram With Embedded Registers Mobley, Sartore, Carrigan, Jones |
| Pat. 2851503 (RAM 343 JPN) | Japan | 01/21/1993 | EMS | EDRAM Having A Dynamically-Sized Cache Memory And Associated Method Mobley, Sartore, Carrigan, Jones |
| Pat. 5,566,318 (RAM 381) | U.S. | 08/02/1994 | RAM | Circuit With A Single Address Register That Augments A Memory Controller By Enabling Cache Reads And Page-Mode Writes Joseph |
| Pat. 5,835,442 (RAM 393) | U.S. | 03/22/1996 | EMS | EDRAM With Integrated Generation And Control Of Write Enable And Column Latch Signals And Method For Making Same Joseph, D.N. Heisler, D.J. Heisler |
| Pat. 5,991,851 (RAM 417) | U.S. | 05/02/1997 | EMS | Enhanced Signal Processing Random Access Memory Device Utilizing A Dram Memory Array Integrated With An Associated SRAM Cache And Internal Refresh Control Alwais, Mobley |
| Pat. 5,901,100 (RAM 418) | U.S. | 04/01/1997 | RAM | First-In, First-Out Integrated Circuit Memory Device Utilizing A Dynamic Random Access Memory Array For Data Storage Implemented In Conjunction With An Associated Static Random Access Memory Cache Taylor |
| Pat. 6,072,741 (RAM 418 CIP) | U.S. | 03/11/1999 | RAM | First-In, First-Out Integrated Circuit Memory Device Utilizing A Dynamic Random Access Memory Array For Data Storage Implemented In Conjunction With An Associated Static Random Access Memory Cache Taylor |
| Pat. 6,172,927 (RAM 418 CIP2) | U.S. | 03/24/2000 | RAM | First-In, First-Out Integrated Circuit Memory Device Incorporating A Retransmit Function Taylor |

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| Pat. 6,141,281 (RAM 429) | U.S. | 04/29/1998 | EMS | Technique For Reducing Element Disable Fuse Pitch Requirements In An Integrated Circuit Device Incorporating Replaceable Circuit Elements Mobley, Ash |
| Pat. 6,055,192 (RAM 430) | U.S. | 09/03/1998 | EMS | Dynamic Random Access Memory Word Line Boost Technique Employing A Boost-On-Writes Policy Mobley |
| Pat. 6,064,620 (RAM 432) | U.S. | 07/08/1998 | EMS | Multi-Array Memory Device, And Associated Method, Having Shared Decoder Circuitry Mobley |
| Pat. 6,278,646 (RAM 432 CIP) | U.S. | 03/23/2000 | EMS | Multi-Array Memory Device And Associated Method Having Shared Decoder Circuitry Mobley |
| Pat. 5,963,481 (RAM 447) | U.S. | 06/30/1998 | EMS | Embedded Enhanced DRAM And Associated Method Alwais, Peters |
| App. 99302956.0 (RAM 447 EPO) | Europe | 04/16/1999 | EMS | Embedded Enhanced DRAM And Associated Method Alwais, Peters |
| Pat. 6,249,840 (RAM 448) | U.S. | 10/23/1998 | EMS | Multi-Bank Esdram With Cross-Coupled SRAM Cache Registers Peters |
| Pat. 6,330,636 (RAM 450) | U.S. | 01/25/1999 | EMS | Double Data Rate Synchronous Dynamic Random Access Memory Device Incorporating A Static RAM Cache Per Memory Bank Bondurant, Peters, Mobley |
| Pat. 6,151,236 (RAM 460) | U.S. | 02/29/2000 | EMS | Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Grieshaber, Mobley, Peters |
| Pat. 6,301,183 (RAM 460 CON) | U.S. | 07/27/2000 | EMS | Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Grieshaber, Mobley, Peters |
| App. 2001-052888 (RAM 460 JPN) | Japan | 02/27/2001 | EMS | Enhanced Bus Turnaround Integrated Circuit Dynamic Random Access Memory Device Bondurant, Fisch, Grieshaber, Mobley, Peters |

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| Pat. 6,392,441 (RAM 461) | U.S. | 06/13/2000 | EMS | Fast Response Circuit Moscaluk |
| Pat. 6,373,751 (RAM 463) | U.S. | 05/15/2000 | EMS | Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant |
| Pat. 6,549,472 (RAM 463 CON) | U.S. | 02/21/2002 | EMS | Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant |
| Pat. 6,646,928 (RAM 463 DIV) | U.S. | 01/16/2003 | EMS | Packet-Based Integrated Circuit Dynamic Random Access Memory Device Incorporating An On-Chip Row Register Cache To Reduce Data Access Latencies Bondurant |
| Pat. 6,501,698 (RAM 464) | U.S. | 11/01/2000 | EMS | Structure And Method For Hiding DRAM Cycle Time Behind A Burst Access Mobley |
| App. 09/828,283 (RAM 465) | U.S. | 04/05/2001 | EMS | Method For Hiding A Refresh In A Pseudo-Static Memory Mobley |
| Pat. 6,538,928 (RAM 468) | U.S. | 10/11/2000 | EMS | Method For Reducing The Width Of A Global Data Bus In A Memory Architecture Mobley |
| App. 09/828,488 (RAM 487) | U.S. | 04/05/2001 | EMS | Method And Circuit For Increasing The Memory Access Speed Of An Enhanced Synchronous SDRAM Peters |
| App. 10/782,386 (RAM 487 CON) | U.S. | 02/18/2004 | EMS | Method And Circuit For Increasing The Memory Access Speed Of An Enhanced Synchronous SDRAM Peters |
| App. 10/178,072 (RAM 491) | U.S. | 06/20/2002 | RAM | Method And Circuit For Increasing The Memory Access Speed Of An Enhanced Synchronous SDRAM Mobley, Peters, Schuette |

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| Pat. 5,787,457 | U.S. | 10/18/1996 | EMS | Cached Synchronous DRAM Architecture Allowing Concurrent DRAM Operations Miller, Rogers, Tomashot, Bondurant, Jones, Jr., Mobley |
| Pat. 6,289,413 | U.S. | 10/15/1999 | EMS | Cached Synchronous DRAM Architecture Having A Mode Register Programmable Cache Policy Rogers, Tomashot, Bondurant, Jones, Jr., Mobley |

Subject to the exceptions described on Exhibit C to the Patent Purchase Agreement by and between the parties dated as of April 13, 2004, Assignor represents, warrants and covenants that: (i) it is the sole owner, assignee and holder of record title to the Patent Rights identified above, (ii) it has obtained and submitted for recordation previously executed assignments for all patent applications and patents identified above as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction, and (iii) it has full power and authority to make the present assignment.

Assignor further agrees to and hereby does sell, assign, transfer and convey unto Assignee all of its rights: (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past and future infringement of the Patent Rights, and (ii) to apply in any or all countries of the world for patents, certificates of invention or other governmental grants for the Patent Rights, including without limitation under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding. Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and at Assignee's sole expense do all things necessary, proper, or advisable, including without limitation the execution, acknowledgment and recordation of specific assignments, oaths, declarations and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. Such assistance shall include providing, and obtaining from the respective inventors, prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, powers of attorney, specifications, declarations or other papers and other assistance reasonably necessary for filing patent applications, complying with any duty of disclosure, and conducting prosecution, reexamination, reissue, interference or other priority proceedings, opposition proceedings, cancellation proceedings, public use proceedings, infringement or other court actions and the like with respect to the Patent Rights.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Ramtron
on April 13, 2004.

RAMTRON INTERNATIONAL CORPORATION

By: 

Name: GREG JONES

Title: PRESIDENT, TECH GRP

(Signature MUST be notarized)

STATE OF COLORADO)
) ss.
COUNTY OF EL PASO)

The foregoing instrument was acknowledged before me on this 13 of April, 2004, by
Greg Jones as President of Ramtron International Corporation, a
Delaware corporation.


Notary Public

My commission expires: 10-30-07

[SEAL]

ENHANCED MEMORY SYSTEMS, INC.

By: 

Name: GREG JONES

Title: DIRECTOR

(Signature MUST be notarized)

STATE OF COLORADO)
) ss.
COUNTY OF EL PASO)

The foregoing instrument was acknowledged before me on this 13 of April, 2004, by
Greg Jones as President of Enhanced Memory Systems, Inc., a
Delaware corporation.


Notary Public

My commission expires: 10-30-07

[SEAL]

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